The World’s Leading High Performance RISC-V & Chiplet Company

Powering Next Generation Data Center and Automotive Architectures

June 2023
Balaji Baktha  
*Founder and CEO*

**Pioneer in Data Center semiconductors: 30+ years experience**
- World’s first 64-bit ARM with Veloce (Acquired by AppliedMicro)
- Led Marvell BU delivering Data Center class Networking, Communications, Compute, Storage and Wireless infrastructure products

Greg Favor  
*Co-founder and Chief Architect*

**One of the world’s leading CPU architects: 35+ years experience**
- Architected K6 processor at startup NexGen, acquired by AMD
- Chief Architect at Siara Systems, acquired by RedBack
- Architected first successful 64-bit ARM CPU

Founded in 2019 by industry veterans with a proven track record of delivering Data Center class processors
Veyron V1: World’s First Data Center Class RISC-V Processor

**Highest Performance RISC-V CPU**

3.6GHz in 5nm process technology

<table>
<thead>
<tr>
<th>Processor</th>
<th>SPECint2017 per socket</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xeon® Ice Lake 8380</td>
<td></td>
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<tr>
<td>EPYC™ Milan 7763</td>
<td></td>
</tr>
<tr>
<td>AWS G3 Neoverse V1</td>
<td></td>
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<tr>
<td>Veyron V1-128C</td>
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</tbody>
</table>

**ASSP Based on High Performance Chiplet Architecture**

Significant reduction in development Time and Cost compared to prevailing monolithic SoC model

Disruptive ROI: Highest Single Socket Performance at Compelling Perf/Watt/$
The Semiconductor Innovator’s Dilemma

• Semiconductors are the foundation of the modern economy
• Unrelenting massive semiconductor consolidation since 2008
• Led to monopoly in each of the semi markets
• Average lifecycle of products is extended from 18 months to 3 years due to the lack competition
• No room for innovation and differentiation
  o OEMs are forced to use silicon from limited sources
• OEMs cannot build their own SoCs
  o Very high development cost: $100-200M per project
  o Incumbent ISAs don’t allow them to innovate
• How do you break the cycle?
Dilemma to Opportunity!

Monolithic SoC

- TTM: 3+ years
- Development cost: $100M+
- Leading edge process node
- Fixed performance
- Large die/high unit cost
- Risk of incorrect definition by time it comes to market

Chiplet-based SoC

- TTM: ~1 year
- Development cost: < $25M
- Each chiplet in optimal process node
- Scalable Compute, Accelerator and I/O performance
- Cost optimized solution
- Chiplets introduce the concept of late binding and scalability

Open Hardware Innovation Led by RISC-V and Open Chiplet Architecture
• Zonal architectures are a compelling opportunity to innovate and differentiate with Veyron Chiplets and Cores in ADAS, Infotainment (IVI), and Telemetry
• Sovereign Data Centers with Security & User Privacy
• Explosive use cases of Generative AI at the Edge
RISC-V and Composability Enable Next Generation Workload Efficiency

- Hardware-Software co-design and Domain Specific Acceleration using RISC-V’s Extensibility
- Composability: Right-sized Compute, Memory, & IO
- Late-binding: CSSP vs ASSP
- Maximize Socket performance and Perf/W/$$
- Supply chain diversification and resilience

Example: Custom Solution for 5G Base Station

X86 + FPGA

Integrated Accelerator

Discrete FGPA

x86 Processor

10x Performance/W/$$

Open Hardware Innovation Leveraging RISC-V and Chiplets
Ventana Veyron: Server Class RISC-V IP + Chiplets

Veyron High Performance RISC-V CPU IP

- Up to 16 cores
- Veyron V1 Core
  - 512 KB L1 D-cache
  - 64 KB L1 I-cache
  - 512 KB L2 D-cache
  - 512 KB I-cache
  - 48MB Shared L3 (sliced per core)
- Coherent Bus
- AMBA® CHI (Coherent Interconnect)
- D2D Interface

Veyron Chiplet Solutions

- Veyron compute chiplets
  - In latest process node technology
  - Scalable CPU performance/count
- IO Hub
  - Implemented in process node of choice
  - Customized for application requirements
- Custom Domain Specific Acceleration
  - Low-cost process node

- Eight wide, aggressive out-of-order instruction pipeline
- High core count multi-cluster scalability (Up to 192 cores)
- Advanced side channel attack mitigations
- Comprehensive RAS features
- IOMMU & Advanced Interrupt Architecture (AIA) system IP
Scalable Architecture for Server-class Compute

- **Entry level server**: 2 chiplets (32 cores)
- **Mid level server**: 4 chiplets (64 cores)
- **High end server**: 8-12 chiplets (128-192 cores)
Realizing Efficient Chiplet D2D PHY

Requirements

- Power efficient
- Small area overhead
- High data rates

Parallel D2D interconnects such as UCIe or BoW offer much lower power, area, and complexity overhead compared to serial/SERDES based solutions like PCIe

D2D Refinement Required for Automotive

- Failure predictability through monitoring
- Detection & reporting of failures

<table>
<thead>
<tr>
<th></th>
<th>PCIe Gen5</th>
<th>BoW-Fast</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Efficiency pJ/bit</td>
<td>7</td>
<td>0.55</td>
</tr>
<tr>
<td>Area Density Tbps/mm²</td>
<td>0.1</td>
<td>0.69</td>
</tr>
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Example Parallel D2D Interconnect: BoW Minimal Bidirectional Reference Link
Pioneering Efficient Chiplet Interconnect Controller

Requirements
- Low D2D latency
- Predictable memory performance
- Standard SoC buses and networks must map easily to D2D transport
  - CHI, AXI, ...
- HW memory coherency for efficient support of accelerators

Ventana has developed a low latency controller IP which maps standard, coherent SoC buses to D2D PHY

< 7ns latency vs 100ns+ for PCIe
Automotive Following Server Architecture

Today: Domain Architecture

- Dedicated, lower performance controllers
- Increasing hardware varieties
- Fragment code development environments
- Not easily upgraded or scaled

Future: Zonal Architecture

- Centralized high-performance compute
- Unified software environment
- Efficient development
- Scalable and easy to develop hardware

Same RISC-V + Chiplets concept applies
RISC-V and Chiplets Driving Innovation in Automotive

- Automotive can benefit from same cost efficient chiplet architectures to create differentiated platforms
- Ventana ASIL certified chiplets and IP
- Partners create automotive Hub
- Accelerators can be integrated in Hub or scaled up in chiplets
Ventana: Leadership in Action

1. Performance Leadership

2. Contribution to the RISC-V International Community

<table>
<thead>
<tr>
<th>Role</th>
<th>Name</th>
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<tbody>
<tr>
<td>Member of Board of Directors</td>
<td>Balaji Baktha</td>
</tr>
<tr>
<td>Vice-Chair of Technical Steering Committee</td>
<td>Greg Favor</td>
</tr>
<tr>
<td>Chair of Privileged Architecture Standing Committee</td>
<td>Greg Favor</td>
</tr>
<tr>
<td>Chair of Platforms Horizontal Sub-Committee</td>
<td>Kumar Sankaran</td>
</tr>
<tr>
<td>Chair of CacheOps Task Group</td>
<td>David Kruckemyer</td>
</tr>
<tr>
<td>Chair of Marketing Events Committee</td>
<td>Omar Hassen</td>
</tr>
<tr>
<td>Vice-Chair of Debug Task Group</td>
<td>Paul Donahue</td>
</tr>
<tr>
<td>Co-author of Advanced Interrupt Architecture</td>
<td>Greg Favor</td>
</tr>
<tr>
<td>Chair of Hypervisor SIG</td>
<td>Anup Patel</td>
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Greg Favor
‘21 RVI BoD Technical Leadership Award
‘20 RVI BoD Technical Contributor Award

Anup Patel
‘22 RVI BoD Technical Leadership Award

3. Driving the RISC-V Software Ecosystem…
Founding Member of RISE to Ensure RISC-V Software Readiness

Mission

• Accelerate the development of open source software for RISC-V
• Raise the quality of RISC-V Platform software implementations
• Push the RISC-V Software ecosystem forward and align partners’ efforts
• Ensure RISC-V is a tier 1 platform for all tools and libraries
• Accelerate RISC-V adoption for Client and above segments
In Closing …

• RISC-V, Chiplets, and Open Standards are the way forward for the next generation of semiconductor innovation

• Ventana leads the market with the Veyron CPU cores and chiplets

• Ventana is uniquely positioned to help revitalize the European semiconductor industry
Thank You