RISC-V customization, HW/SW co-optimization, and Custom Compute

RISC-V Summit Europe

Brett Cline

June 6, 2023
Traditional approach to hardware design

Flexible but slow..?

Choose a general-purpose core and optimize software.

...or fast but hard coded?

Implement fixed-function hardware circuits.
You don’t have to chose any longer.
A new disruptive force

- Open ISA
- Growing ecosystem
- No restrictions
- Customization allowed, and encouraged

- Counters end of scaling laws
- Best ISA for Custom Compute
Custom instructions for unique workloads

- **Adding custom instructions**
- **Adding RISC-V extensions**

**Performance**
(for a given set of applications)

**Optimization space**

- **Processors with custom instructions**
- **Processors with RISC-V extensions**
→ Hardware/software co-optimization

Shift left
Custom Compute is not new…

it is highly rewarded today
Custom Compute + benefits of a custom SoC
Our fundamental beliefs

- RISC-V will gain share
- HW & SW collaboration
- Co-optimization
- Custom Compute
- Processor selection
- Processor ownership
- OEMs doing more chips

Big winners

Big losers
But there is a talent challenge

- Many processor architects
- Many processor architectures

30 years ago

- Processor design
- Processor selection

15 years ago

Scarcity of skills

Now
Question:
How has the industry coped with complexity and limited design skills in the past 50 years?

Answer:
Automation → EDA tools
Processor design tools

Codasip RISC-V customizable IP
In CodAL high-level language

Codasip Studio

Profiling/analysis
IA model
CA model
Generator

SDK
HDK
→ Safety and security driving RISC-V forward

A combined approach to create dependable products for all markets
A fundamental security problem
What if you could... customize a security processor based on a starting production core?

...and be protected.
• Unique implementation of protection

CENSORED BY CODASIP MARKETING

Come on Brett, you know you can't show this yet 😇

(seriously, these commercial guys...)
→ Innovation through customization

No more “free improvements” with end of Moore’s law

Need to optimize processing to the application
→ Custom Compute

IP and tools to support a hardware / software co-optimization methodology
Architect your ambition

Zdenek Prikryl, CTO
RISC-V as an enabler of heterogeneous compute
Demo theatre - Wednesday 10.55

Tariq Kurd, Lead IP Architect
RISC-V code-size reduction with Zc extensions and dictionary compression custom instruction
Technical talk - Thursday 15:00

Come by our booth for a demo!