RISC-V Is Firing On All Cylinders

Charlie Su, Ph.D.
CTO and President

2023/06/06
Andes Technology Corporation

Andes and RISC-V International (RVI)

- Founding & Premier Member from 2016
- Board of Directors
- Technical Steering Committee
- Chairs/Co-Chairs of Task Groups
- Ambassador

Quick Facts

- 18 Years
  - Pureplay CPU vendor
  - Licensing AndesCore™

- 300+ Customers

- 80K+ Users
  - AndeSight IDE

- 12Bn+ SoC
  - Total Customer Shipment

<table>
<thead>
<tr>
<th>AX60 Series</th>
<th>AX65</th>
<th>AX67</th>
<th>AX60-SE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Categories</td>
<td>Power-efficient</td>
<td>Mid-range</td>
<td>Extended</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>45 Series</th>
<th>N45, NX45</th>
<th>NX45V D45</th>
<th>AX45MPV A45(MP), AX45(MP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>27 Series</td>
<td>NX27V</td>
<td>A27(L2), AX27(L2)</td>
<td></td>
</tr>
<tr>
<td>Compact Series</td>
<td>N225</td>
<td>D23</td>
<td>Linux AP</td>
</tr>
</tbody>
</table>

Note: AX45MPV configured as one core

References:
- A72~A78, N1/V1/X1
- A53/55, R52/R82, M7
- A5/7/35
- A5/7/35, R4/5, M4/33
- M0/0+/3/33/4
Andes Powering RISC-V Applications Everywhere


Mobile
- N25F, N45
- Performance, code size

MPU/MCU/AIoT
- D25F, D45, AX25MP, AX45MP

Cloud AI
- NX27V, AX25, AX27, AX45MP, AX45MPV
- Accelerate, accelerate, accelerate

Space
- Secure, control, compute, communicate, position
- N25F

Storage
- PHISON
- Performance, bandwidth, real-time

5G Networks
- N25F, A25, A45MP, AX45MP

Internet Company
- SK telecom

Confidential
Taking RISC-V Mainstream
Renesas Voice-Control ASSP Solution
- **R9A06G150** 32-bit 100MHz ASSP with Andes DSP-capable D25F, which speeds up the application by over 50%.
- **Cyberon**, an expert in voice recognition technology
- **Orbstar**, a system integrator specializing in embedded solutions
- **SEGGER**, supporting the ASSP with Embedded Studio and J-Link

ASUS IoT Tinker V Single-Board Computer:
- Based on Renesas RZ/Five 1GHz SoC with Andes AX45MP
- Supporting Linux Debian and Yocto distro with rich connectivity
- Ideal for Industrial IoT and gateway applications

Powered by Andes D25F/AX45MP
5G Small Cell SoC for Open-RAN

Picocom PC80x uses RISC-V Clusters and Linux core

- **Low power**
- **Flexible control for**
  - Task scheduling
  - Memory management
  - Event handling
- **Computation assistance for**
  - DFE (Digital Frontend)
  - DPD (Digital Pre-Distortion)
- **Support protocol/interface upgrades**
  - CPRI (common public radio interface)
  - eCPRI (enhanced CPRI)
- **Friendly development environment:**
  - Zephyr and Linux for application development

Powered by Andes N25F/A27
Compute-in-Memory (CIM) SoC

- Houmo H30 CIM SoC
- CIM Macro provides 256 TOPs (int8) in an H30
- RISC-V Vector processor: Flexibility to tackle Long Tail
  - Each NX27V provides 128 GOPS thru versatile RVV
  - ACE tools greatly simplify custom extensions

**SoC**

- IPU Cluster
  - IPU
  - Pre/Post Process
  - Tile Array
  - LDST
  - Bus Node

**Tile**

- NX27V CPU
  - SFU
  - TE
  - Macro Array

**Vector Unit**

- Andes Streaming Port™ (ASP)

**SRAM-CIM Macro**

- Powered by Andes NX27V
RISC-V Is Driving Innovations

– with Industry’s 1st RISC-V ISO 26262 Fully Compliant Core, Andes N25F-SE
– Isn’t possible without partners for compilers, tools and RTOS/AutoSAR
AndesCore™ AX65 OOO Application Processor

- 13-stage 4-way 64-bit OOO processor
- RVA22 profile
- Multicore cluster up to 8 cores
- 8 Execution Pipes: 4 ALU, 2 LD/ST, 2 FP
- 2-Level BTB with TAGE-L Branch Predictor
- Caches:
  - Private I/D caches: 64 KB, 4-way, 4-bank
  - Shared cache: up to 8 MB, 16-way
- 256-bit AXI4, MMIO and IOCP Buses
- Performance:
  - 2.4 GHz* @7nm without overdrive
  - Specint2006: 8.25/GHz
  - Specfp2006: 10.2/GHz
- AX67:
  - Further performance boost
  - RVA23 (or RVA24)

**Best spec2k6 with 2-level caches**
AX45MPV: 1024-bit Vector Processor

**RISC-V Vector Extension (RVV v1.0)**
- Data format: int8~64, fp16~64; int4, bf16
- VLEN/DLEN: 128~1024 bits, 1:1 or 2:1 ratio
- Up to 6 DLEN results per cycle

**Efficient support needed for tight coupling with HWE**
1. Data exchange performance (from/to shared memory in HWE)
2. Efficient control to the HWE

**2 solutions offered in AX45MPV:**
- Andes Streaming Port™ (ASP) thru ACE
  - Data bus: data transfer btw VR and HWE
  - Command bus: to control/synchronize HWE operations
- HVM: High-speed Vector Memory
  - CPU side: DLEN-wide load/store interface with dynamic wait cycles
  - HVM module: accepting multiple accesses to multi-bank SRAM’s
Matrix Multiplication Extension

■ To speed up MatMult

■ Some common goals:
  ● High compute-to-memory ratio
    – Leading to high MAC utilization
  ● Input/output registers: existing VRF and/or new (matrix) registers
  ● Scalability: VLEN-agnostic at the binary or source level

■ Less-addressed issues:
  – Matrix register file: more usage to be explored if used
  – Boundary-case handling: several instructions needed to compute 2D mask
  – Solutions to enable both inner-product or outer-product based computation sequence to defer the cost/performance tradeoff (from IP to IC)
RISC-V Continues to **RISE** Rapidly

- **RISE**: RISC-V Software Ecosystem, a project under LF Europe
- To accelerate the development of RISC-V open source SW
- Led by industry leaders
- **Areas to focus over time:**
  - Compilers & Toolchains
  - Language Runtimes
  - System Libraries
  - Debug & Profiling Tools
  - Simulator/Emulators
  - Kernel and Virtualization
  - Linus Distro Integration
  - System Firmware
- More at [https://riseproject.dev](https://riseproject.dev)
Thank You!