RISC-V : An opportunity for Bosch Automotive Electronics product range

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RISC-V – Bosch AE

Agenda

Section 1
• Bosch Mobility Electronics (introducing Bosch as Tier-1 and Tier-2/Tier-3 supplier)
• Automotive product map

Section 2
• Performance required and typical processing needs per module
• Focus on Automotive Electronics (Bosch Tier 2) needs, market perspective
• Range of cores required by Automotive Electronics needs

Section 3
• Expectations/Key points from the RISC-V introduction in Automotive Electronics products
• Focus key parameters (from ISA to PPA)
• HW eco system
• SW eco system
• Functional Safety & Security attributes

Section 4
• Conclusion and perspectives
Electric & Electronic Architecture
Integration of software and I/O parts from fixed-location ECU (e.g., window control, ...)

Integration of dedicated hardware functionalities (e.g., body, climate, ...)

I/O connection of simple sensors and actuators (e.g., seat, window, ...)

Sensors & actuators

I/O connection of high-data-rate sensors (e.g., camera streams, ...)

Zone controllers

Vehicle computers

High-performance SW features that define vehicle-level functions (e.g., ADAS, ...)

SW Updates
Hardware dependency
Safety and homologation relevance

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Demanding needs for Assistance and Automated drive

OEMs have need for HW compute...
Key trends in automotive industry drive the demand for compute HW, e.g.:

- Autonomous Driving (Assist.)
- Software-defined vehicle + x- Domain Integration

in a market w/ limited volume...

- Vehicle produced (M Units)
- Year

and increasing cost...

- Computer Performance (TOPS)
- SAE

- Total Dev. Costs (M$)
- Node (nm)

How to rearchitect for....

- Affordability
- Scalability
- Complexity
- Flexibility
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New Trend-Chiplet

Monolithic System-on-Chip

Requires development of entire new monolithic SoC

- Is current standard in SoC development
- Ensures high performance for use-cases
- High development & fabrication cost, esp. with larger die sizes and lower node sizes

Chiplet-based Systems

- Allows for smaller individual die sizes and combination of varying node sizes
- Simplifies reuse of already existing chiplets in varying configs.
- Cost efficiency of packaging tech unclear

Available from e.g., consumer electronics

Serializer/Deserializer
ML/AI
Comms
CPU
Memory
I/O
GPU

 Serializer/Deserializer
3-7nm
ML/AI
3-5nm
CPU
3-7nm
Memory
14-16nm
GPU
3-7nm
I/O

Leverage existing chips (savings in R&D & EoS)

Automotive Chiplet System (ACS)

- New ACS architecture to derive various configurations
- Disintegration of value chain, allowing for new entrants in compute
- Enabling OEM involvement in design choices & tailoring towards own req's
- Easier upgradeability and re-usability of individual Chiplets within system

1. Economies of scale, i.e., because chip can be used in gaming and automotive

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Combined ADAS/IVI performance needs

Take away
• 64b processor, ~10 DMIPS/MHz
• Large multi-core, cache-coherent architecture, heavy multi-thread capability
• 3-5GHz, CMOS technology <5 nm
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IP, Sensors, Gatewayd

- Engine Management
- Brake Control
- Airbag & Safety Restraints
- ADAS Sensors
  - RADAR, USS
- PMICs / Power Safety Communication
- E-Drive Control
- In Vehicle Networks
- HW accelerators
  - Computer Vision
  - EDE, GTM
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Focus on IP, Edge and Gateway needs

32 bit variant
Excellent **real-time** capability, 2 to 3 DMIPS/MHz
Some SIMD capability, FPU optional
Extension to tightly attached coprocessors (+more loosely attached ones)
100 MHz-1GHz, 65..16nm, down to below 10nm for Zone/Domain controller
Mostly single core till 1kDMIPS, dual or quad core capability above
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Bosch Automotive Electronics : key points for Risc V

- Vendor independence
- Geographic independence (Control export rules)
- Reduced cost of ownership including options to work with some open-source IP
- Full range / scalability

- Opportunity to customize ISA to specific needs
- Extensibility to Data handling (SIMD operations)
- Interoperable IP and tools served by numerous companies, good dynamics in ecosystem
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Bosch involvement in RISC-V ecosystem

• Bosch AE is involved in RISC-V ecosystem
  • in cooperative projects such as Scale4Edge (Ge), EU-funded project Tristan
  • Special focus on RISC-V Use in functional safety relevant applications
  • CVA-6 extension (FuSa, AI tightly attached coprocessor) with the support of OpenHW Group
  • CVA-6 verification contribution in the OpenHW Group umbrella
  • Modeling with EU partners

• Bosch is in discussion with several RISC-V suppliers matching automotive needs
  • At both Automotive Electronics level and at Tier-1 level

• Bosch Automotive Electronics is in assessment phase for the time being
  • Target: Decision about product introduction based upon RISC-V for Start of Production 2028+
RISC-V Ecosystem
Bosch Automotive Electronics view

HW development
- Models / Platform Integration ready
- VHDL/Verilog ready to integrate into IC & FPGA
- IDE for SW HW codesign
- HW Safety Package

SW Stack
- RTOS porting
- Optimized Libraries for custom operations on SIMD acc.

Subsystem IP Blocks
- Core IP Extension
- RISC-V Core Engine
- Automotive and Functional Safety
  - Hypervisor
  - 1st level IRQ
  - Generic Tightly attached copro (FPU)
  - Custom Tightly attached copro (..)
  - 2nd level IRQ
  - Scratch Pad Memory
  - Multi-core capability
  - Core IP Trace
  - Standard NoC i-f
  - L1$ Memory
  - Generic Loosely attached copro (SIMD)
  - L2$ Memory
  - Custom Loosely attached copro (AI)

SW Development
- ISS / Profiler and performance monitoring
- Debugger
- Tracer
- Compiler/Linker
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Key focus points

- ISA instructions (MAFDC capability)
  - Bit/Byte handling capability (L/S/ALU) – (Zbb/Zbs)
  - Code Compression extension – (Zc)
  - Superscalar capability (dual-issue primarily ALU/ALU and ALU/LS)
  - In-order execution, branch prediction
  - Optimized control/config of operations (Zicsr), dynamic load of program (Zifencei), semaphore (atomic)

- Other capability
  - Hypervisor
  - FPU 32b/64b and 16b operations
  - SIMD 4b/8b/16b/32 single cycle MAC (4x8b typically) + DSP specifics ("0" overhead loop, circular addressing)
  - Extension to dedicated coprocessor via CV-X-IF, optionally native RISC-V ISA Extension

- Performance, Power, Area
  - Linked to pipeline length (2-8)
  - Low power design (clock gating, granularity in cache management, transaction mgt with Interconnect, WFI)
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HW eco system key points

- **Automotive compliance** (pay attention to memory cuts, scan coverage, *don’t use* cells for hard macro)
- L1$ (Write Through and Write Back configuration), 0 ws Scratch-Pad Memory
- **Efficient IRQ management** (128 lines at least, >8 priority level including NMI, vectored mode support, low latency handling i.e. ~30 cycles, multi-core capability)
- Monitoring IP [PMP] supporting off and on-line performance measurement - +32b counter of HW evts
- Trace and Debug (JTAG compliance, HW break point, step-by-step instruction, Test Access Port, I&D)
- **Multi-core capability** (inc. coherent systems, L2$ (unified cache complying with AXI/ACE i-f)
- Advanced memory management (support of 16+ regions of variable size, cacheability attributes)
- **Standard Interconnect i-f** (AXI-4/AXI-5 compliance)
- DMA (memory to memory, memory to peripherals, safety and security attributes)
- **IDE to perform combined HW/SW codesign for coprocessor** tightly attached to core
  - Definition of requirements (DSL) to generate ISA extensions - ensure portability of custom extensions, agree upon an API to integrate RISC-V cores in SoC context and assess KPIs from a customer SW / Workload
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SW eco system key points

- Performing Compiler (C/C++, Rust) \(^1\)
- Optimized libraries (SIMD exploitation..)
- Model (integration-ready into platform creation Toolsuite, instruction accurate & cycle approximate)

- Debugger, Profiler, Tracing Toolsuite
- RTOS\(^2\) exploiting HW facility, Hypervisor

\(^1\) see also safety related constraints for qualification according to ASILD ISO-26262
\(^2\) RTOS is primarily RTK for AutoSar but QNX is of relevance

High Level OS can be seen as relevant extension for 64b variant though not a priority for Bosch Automotive Electronics now
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Functional safety attributes

- **FuSA ISO 26262**

- Functional Safety is **not just about HW technical measures** to cope with transient and permanent faults.

- Functional Safety has much to do with development process.
  - IP shall be developed according to a mature and ‘safe’ development plan in order to avoid systematic faults.

- Functional Safety calls for a safety package which requires safety analysis in depth to derive key documentation meant for correct integration of IP into SoC.

- Now, Functional safety also requires dedicated **HW facility to cope with transient and permanent/latent faults** such as dual-core lock step, error protection on memory buffer as well as on physical path (address, data), etc..

- Functional Safety is **not about HW work products** but also scopes **SW work products** (compiler/assembly).
Security attributes

- Security ISO 21434

  - Primarily a security analysis support (TARA) at module and IC level that will call for a need for a **security package** (integration guideline at the least)

  - Tough in general **more a subsystem or an IC level issue** calling for dedicated HW IP, protected bus to convey sensitive data, anti-tampering mechanisms such as shield/analog sensors, ...

  - Additional support at **Core level** can also be relevant such as Zbk, Zkn ISA extension or even some **tightly attached crypto coprocessor** (such as AES)
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Conclusion and Perspectives

▪ Our short term needs
  - ASIL-D capable IPs with all relevant goodies matching our full-range needs
  - ASIL-D approved and efficient C/C++ compilers
  - Eco-system is progressing on that matter with some vendors taking the request with full concern

▪ Our next target
  - Get Flexible IA & Cycle Approximate models that can be ‘easily’ integrated in order to create virtual platform at SoC and ECU-level
  - Make sure that trace and debug ecosystem is getting mature
  - Get a competitive PPA for Bosch Automotive Electronics entire range

▪ Our challenges
  - OpenHW Group : maturing ecosystem with lot of actors, expecting mature verification whilst working on FuSa
  - RISC-V : What about an extension of scope to GPU ?
THANK YOU
FOR
YOUR ATTENTION