TRISTAN

Together for **RISC-V** Technology and Applications

Patrick Pype
Director Strategic Partnerships
NXP Semiconductors

*RISC-V Summit Barcelona, June 7th, 2023*
Agenda

• How it all started...

• The TRISTAN consortium and project

• How TRISTAN contributes to the EU Roadmap on RISC-V and Open-Source

• Why TRISTAN needs ISOLDE ?

• Conclusions
Agenda

• How it all started...
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“Alibaba introduced first RISC-V based product (XT910) in July 2020”  
(Source: https://www.nextplatform.com/2020/08/21/alibaba-on-the-bleeding-edge-of-risc-v-with-xt910/)

“How it all started... Europe to urgently catch up with China

“The massive on-going adoption of open source in China, “... , with a strong support from both the central and regional authorities, is a very interesting trend in China’s strategy to catch up in semiconductors.”

“For China, open source is an industrial policy tool and important part of its push for technological autonomy”  
How it all started...
Why RISC-V in Europe?

**STRENGTHS**
- Easy access & low barrier for SoC design
- Ability to customize
- Accessible data for safety & security analysis (whitebox)
- Availability of SW ecosystem
- Lower export control restrictions
- Less vulnerable to geo-political risks
- Strong academic support; educational use
- Steers Innovation

**WEAKNESSES**
- Not Industrial Quality IP yet (HW/SW)
- Long-term guaranteed support to industrial users not yet established
- Risk of maintenance
- Lack of some IP (e.g. interconnect)

**OPPORTUNITIES**
- Customization opportunities
- Sharing development costs
- Sharing support costs
- New licensing models
- Support to SME’s
- New industrial leaders

**THREATS**
- Risk not to create enough critical mass in Europe
- US/China competitors are running fast, with large investments and acceptance by leading end-user companies

Europe must develop the RISC-V supply chain to support autonomy in critical market sectors and reduce its dependency on US & China

MAXIMISE
RESOLVE
How it all started...
European WG to create Recommendations & Roadmap

Recommendations and Roadmap for European Sovereignty in Open Source Hardware, Software, and RISC-V Technologies

Report from the
Open Source Hardware & Software Working Group

November 2021

Members of the Open Source HW/SW Working Group

Chair:
Patrick Pype
NXP Semiconductors

Participants:
Jan Andersson
Cobham Gaisler

Luca Benini
ETH Zürich / Univ. Bologna

Sven Beyer
Siemens

Holger Blasum
SYSGO GmbH

Sylvain Depierre
NanoXplore

Marc Duranton
CEA

Wolfgang Ecker
Infineon

Michael Gielda
Antmicro Ltd

Edwin Hakkennes
Technolution

Andreas Koch
Technische Universität Darmstadt

Loic Liétar
GreenWaves Technologies

Andreas Mauderer
Bosch

Jan-Hendrik Oetjens
Bosch

Jérôme Quévremont
Thales

John Round
NXP Semiconductors

Javier Serrano
CERN

Herbert Taucher
Siemens

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How it all started...
Defining a RISC-V Eco-System: IP to SoC Landscape

RISC-V is a modular ISA:
- Basic
- Standard extensions
- Custom extensions

Base Building Blocks
- High-end RISC-V core
- Mid-end RISC-V core
- Low-end RISC-V core
- Other SoC IPs (interconnect, peripherals...)

Software
(OS, tool chains, compilers, drivers, debuggers...)

Domain-specific features
(safety, security, acceleration, AI...)
- Custom RISC-V extensions
- Co-processors / accelerators

Customized solutions for various markets
- Automotive
- Industrial
- Communication
- Data
- Other sectors

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46 partners
Budget: 54 M€
Starting Date: 1 Dec 2022
Lead: NMP
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Overarching Aim of TRISTAN

Aim of the WP

Expand
Mature
Industrialize

the European RISC-V ecosystem in order to compete with existing commercial/proprietary alternatives

How ?

- leveraging the Open-Source community to gain in productivity and quality
- defining a European strategy for RISC-V based designs including the creation of a repository of industrial quality building blocks to be used for SoC designs in different application domains (e.g. automotive, industrial, etc.)
- applying a holistic approach, covering both electronic design automation tools (EDA) and the full software stack
- exposing a large number of engineers to RISC-V technology, which will further strengthen adoption.
### TRISTAN Objectives & Expected Impact

<table>
<thead>
<tr>
<th>Objectives</th>
<th>Expected Impact 3-5 years after project end</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor Development</td>
<td>At least 4 industrial RISC-V based SoC design starts per year</td>
</tr>
<tr>
<td>Eco-system of Industrial Quality SoC Building Blocks</td>
<td>At least 2 Building Blocks used in 4 industrial design-ins</td>
</tr>
<tr>
<td>SoC Development Infrastructure</td>
<td>Availability of SW stacks, development &amp; EDA-tools TRISTAN stack visible in at least 1 Open-Source project per year</td>
</tr>
<tr>
<td>Vendor Independence</td>
<td>At least 80% of TRISTAN HW IP’s simulates and synthesizes with at least 2 different vendors and Open-Source tools</td>
</tr>
<tr>
<td>Active EU Open-Source HW Community</td>
<td>At least 5 new requests outside TRISTAN consortium making use of TRISTAN results in the OpenHW Core-V CVA6 repository At least 10 references of TRISTAN are found in design-ins</td>
</tr>
<tr>
<td>Demonstration of Building Block Interoperability</td>
<td>At least 2 examples of Building Blocks interworking visible in design-ins</td>
</tr>
<tr>
<td>Pre-Certification &amp; Validation</td>
<td>Effort of certifying a product composed of TRISTAN items is reduced by 80%</td>
</tr>
</tbody>
</table>
How Open-Source SW penetration can evolve towards an Open-Source mixed HW/SW eco-system

**Massive penetration of Open Source Software**
- IoT (Arduino),
- Mobile (Android),
- Enterprise (Linux),
- HPC (Linux, OpenMP, etc.)

**Moore`s Law + Power = Specialization**
- More cost effective
- More performant
- Less Power

**New Open Source Hardware Momentum from IoT and the Edge to HPC**
- RISC-V
- OpenPOWER

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### TRISTAN’s 3 levels of operation

in order to encourage rapid industry adoption of an increasingly rich RISC-V eco-system

<table>
<thead>
<tr>
<th>DEVELOPMENT</th>
<th>VALIDATION</th>
<th>OUTREACH</th>
</tr>
</thead>
<tbody>
<tr>
<td>Extend RISC-V processor designs with new capabilities for industrial adoption</td>
<td>Clarify alignment with, and differentiation from other IS families</td>
<td>Introduce new engineers to RISC-V</td>
</tr>
<tr>
<td>Created supporting IP-blocks to industrial quality level, with simple and transparent licensing</td>
<td>Demonstrate that RISC-V addresses real-world problems as well, if not better, than existing proprietary solutions</td>
<td>Create a productive binding between Les, SMEs and RTOs working on RISC-V across Europe</td>
</tr>
<tr>
<td>Reduce EU dependence on ‘opaque IP’ blocks which cannot be independently verified</td>
<td>Demonstrate that developed toolchains are capable of rendering structured and full ASIC design by real tape-outs</td>
<td>Improve the relationship between the Open-Source and Industrial Communities</td>
</tr>
<tr>
<td>Create and solidify robust EDA tooling for microcontroller, SoC and CPU designs</td>
<td></td>
<td>Educate the industrial community in how to work constructively with Open-Source</td>
</tr>
<tr>
<td>Develop world class SW tooling to develop RISC-V applications</td>
<td></td>
<td>Encourage commercial organizations to become less fearful of Open-Source</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Build a reference repository for RISC-V compliant IP-blocks</td>
</tr>
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TRISTAN’s Scientific Methodology

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• Why TRISTAN needs ISOLDE ?

• Conclusions
How TRISTAN contributes to the EU Roadmap
RISC-V and Open-Source

<table>
<thead>
<tr>
<th>Roadmap Elements</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Repository of RISC-V based Processor Platforms</td>
<td></td>
</tr>
<tr>
<td>Domain-Specific Processor Features</td>
<td></td>
</tr>
<tr>
<td>Repository of Open Source HW Peripheral Blocks</td>
<td></td>
</tr>
<tr>
<td>Interconnect for Real-Time and Mixed Criticality</td>
<td></td>
</tr>
<tr>
<td>Interconnect for System Integration</td>
<td></td>
</tr>
<tr>
<td>Domain-Specific Accelerators</td>
<td></td>
</tr>
<tr>
<td>Software</td>
<td></td>
</tr>
<tr>
<td>Methodology and EDA Tools</td>
<td></td>
</tr>
<tr>
<td>Domain-Specific Demonstrators</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Timeframe</th>
<th></th>
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</thead>
<tbody>
<tr>
<td>Short Term</td>
<td>2-5 years</td>
</tr>
<tr>
<td>Mid-Term</td>
<td>5-10 years</td>
</tr>
<tr>
<td>Long Term</td>
<td>&gt; 10 years</td>
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Extract from TRISTAN positioning on EU Roadmap

<table>
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<tr>
<th>Positioning of TRISTAN developments in EU RISC-V &amp; Open-Source Roadmap</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Roadmap Elements</strong></td>
</tr>
<tr>
<td>High-end: Highly customizable Multi-core Out of Order 64-bit open source infrastructure with the associated memory hierarchies (caches/coherency, off-chip) and communication (fast cores to cores, cores to accelerators, cores/accelerators to system). This should be suitable for various instances of processor IP.</td>
</tr>
<tr>
<td>Highly customizable high-end domain-specific cores for high-performance embedded system and/or general-purpose application (link with EuroHPC call on HPC processors)</td>
</tr>
<tr>
<td><strong>Domain-Specific Processor Features</strong></td>
</tr>
<tr>
<td>Provide public artifacts for safety and security by architecture at an initial assurance level</td>
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<td></td>
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How TRISTAN contributes to the EU Roadmap
Vision in EU

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Positioning TRISTAN

How TRISTAN contributes to the EU Roadmap
Approach to European Success Story
From Niche to Certified Mass Deployment

- RISC-V based Open Source IP
- Use of RISC-V Open Source IP for Application Component Design

R&D | FID (First Industrial Deployment) | Exploitation

Start-ups Universities Design Wins

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Approach to European Success Story
From Niche to Certified Mass Deployment

RISC-V based Open Source IP

Use of RISC-V Open Source IP for Application Component Design

Industrialization of RISC-V Open Source IP

Strategic Fully supported IP Portfolio Design Wins

Start-ups Universities Design Wins

R&D

FID

(First Industrial Deployment)

Exploitation

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Why TRISTAN needs ISOLDE?
Move into another dimension...
ISOLDE Consortium

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41 partners
Budget: 42 M€
Starting Date: 1 May 2023
Lead: Infineon
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Goals of ISOLDE

- Foundation infrastructure: maintain and grow
- Validation/testing on future pilot lines
- Foundation infrastructure: maintain and grow
- Prefabication capabilities
- Concrete realizations
- SoC implementations + Chiplets (M-Cores)
- SoC implementations + Chiplets (32-bit)
- SoC implementations + Chiplets (64-bit)
- New packaging solutions
- RISC-V architecture
- 3 families of processors from base infrastructure
- Processors: 32-bit ("Open cores 32-bit")
- Processors: 64-bit ("High End application cores")
- Design for verticals
- Foundation infrastructure:
  - Basic Building Blocks, Domain-specific extensions
  - accelerators, co-processors, custom extensions)
  - Methodology & EDA tools (Open Source ASIC tools, chiplets, analog IPs), Software incl. already developed IP

- Validation/testing on future pilot lines
- Concrete realizations
- Foundation infrastructure: maintain and grow
- Design for verticals
- Foundation infrastructure:
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TRISTAN

ISOLDE Project
High Performance: 64bit, super-scalar, out-of-order
## TRISTAN and ISOLDE Project

**Synergise, Complement and Build a strong European Network**

<table>
<thead>
<tr>
<th>Item</th>
<th>Tristan</th>
<th>Isolde</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor Development</td>
<td>• Decent Performance</td>
<td>• High Performance</td>
<td>• To be proven in real designs</td>
</tr>
<tr>
<td></td>
<td>• CVA6 and Pulp</td>
<td>• CVA6, Noel-V</td>
<td>• Isolde strives for super scalar, out of order, 64 bit</td>
</tr>
<tr>
<td>Building Blocks for SoC/High Perf, Computing</td>
<td>• SoC Building Blocks</td>
<td>• High performance and/or low power accelerators</td>
<td>• In both cases (documentation, RTL, test-bench, drivers, other design artifacts)</td>
</tr>
<tr>
<td>SoC Development Infrastructure</td>
<td>• Focus on standard peripherals</td>
<td>• Focus on High performance accelerators</td>
<td>• Industry quality</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vendor Independence</td>
<td>• Validate with different colaterals</td>
<td></td>
<td>• Avoid locking of HW-IP and SW-stack/tools to specific vendor</td>
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## TRISTAN and ISOLDE Project

Synergise, Complement and Build a strong European Network

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<th>Isolde</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Safety/Security</td>
<td>• Especially multi-core • Preparation of certification</td>
<td>• Features enabling Safety and/or Security Certification for high-performance RISC-V Computing</td>
<td></td>
</tr>
<tr>
<td>Research</td>
<td>• High Performance Computing research</td>
<td>• ISOLDES’s focus is high performance compute, TRISTAN’s focus is SoC building</td>
<td></td>
</tr>
<tr>
<td>Open Source (OS)</td>
<td>• Active European OS Hardware Community</td>
<td>• High Quality OS Hardware and Software IP</td>
<td>• Both strive for deliverables given to open source</td>
</tr>
<tr>
<td>Demonstration of Building Block</td>
<td>• Mainly models and FPGAs • Interoperability between a high number of IPs</td>
<td>• Mainly FPGAs and ASICs • Make OS IPs de factor standard • Focus: Cores and Accelerators</td>
<td>• ASICs and FPGAs are targeted in both projects. Isolde strives for more ASIC demonstrators</td>
</tr>
<tr>
<td>Interoperability</td>
<td></td>
<td></td>
<td></td>
</tr>
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TRISTAN and ISOLDE Consortium

Synergise, Complement and Build a strong European Network
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Conclusion

• TRISTAN & ISOLDE are starting points for creating a **European Eco-System of RISC-V and Open-Source**

• Within 5 years RISC-V CPU’s are at no functional disadvantage to establish **competitive & competing architectures**

• TRISTAN & ISOLDE will form the impetus to create low-, mid- and high-end platforms for different **strategic application domains** in Europe...

Mobility  
Energy  
Digital Industry  
Health & Wellbeing  
Agrifood & Natural Resources  
Digital Society
The Future: Automotive Platforms based on RISC-V
Delivering on EU strategies in the automotive sector

EU CHIPS ACT

- Open SW-defined vehicle platform (CarOS + Middleware)
- Reduce costs and complexity by working together on non-differentiating features
- Ensure level playing field for automotive HW and data-driven cloud-edge applications

NEW INDUSTRIAL STRATEGY

- Reinforce EU position in strategic market of high-performance central automotive processors
- Leverage RISC-V developments to reduce dependencies on non-EU technologies & suppliers

Research and Innovation Policy

Data Strategy

European Green Deal

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From First Idea on TRISTAN to a European Success Story...

Two members of the consortium (Davide Schiavone – OpenHW Group & Adrian Evans – CEA) are giving a TRISTAN workshop on Friday morning:

Open-Source Hardware Basic Training: [https://riscv-europe.org/side-events.html](https://riscv-europe.org/side-events.html)