Software-driven evolution of
a uniquely modular ISA

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Delivering silicon that isn’t supported by software is a bug.

— Pat Gelsinger, CEO, Intel
Delivering silicon that fails to optimise for its workloads is a missed opportunity.
Foster adoption and innovation
Foster a workload-driven evolution of the RISC-V ISA
Enable the coexistence with vendor-specific extensions

Enable differentiation, manage fragmentation
Standardise the basic platforms
Enable vendors to gracefully transition from existing non-standard solutions

Deliver optimised software support
Foster Open-Source Projects, early-adopters, and academia
Guide the community towards optimisations for RISC-V
Extensability
RISC-V enables implementors to add their domain-specific “secret sauce” to designs.

Modularity
RISC-V allows implementors to leave off unneeded features from their designs to “scale-to-fit”.

How can we leverage a common software without holding everyone back?

How can we innovate and roll out adoption of new features?
Architectural improvements
Specialised instructions and new ISA extensions
Consumes opcode space
Increased maintenance burden and complexity for toolchains

Microarchitectural enhancements
Fusion patterns
Increased complexity for toolchains
Diminishing gains due to software interoperability requirements

Improvements to code generation
Increased maintenance burden and complexity for toolchains
Rooting new instructions in fact-based decisions

Evolutionary drivers
- Standard benchmarks
- Real-world workloads

Proposals for new instructions

Experimental toolchains

Emulation and instrumentation

Performance metrics
Zfa

- Derived from quantitative analysis of ‘imagick’
- Reduces the dynamic instruction count by 9 to 19% (depending on whether both floor and ceil are calculated before the first branch)
- “Load FP immediate” is based on analysis of SPEC FP

Zicond

- Designed to follow the RISC-V philosophy
- Based on extensive analysis to confirm that branchless sequences also reduce instruction counts (e.g. > 1% on some SPEC benchmarks)
- Quantitative analysis confirms that many branches turn compressible as an add-on benefit
Extensions originating from software applications tend to be small and lightweight.
Managed Runtimes SIG

Sstdso: Dynamic per-process switching of Zits fast-track proposal
User-mode memory management fast-track proposal

AI/ML SIG

Matrix operations extension

Graphics SIG

Android SIG

Palette memory (memory colouring) fast-track proposal

RVM-CSI SIG

RVM-CSI non-ISA specification
To successfully evolve the RISC-V we need everyone to drive the discussion based on workload-observations and quantitative data.
Thank you!

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