Implementation of an Edge-Computing RISC-V based architecture for RFID communication

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Abstract

RFID devices are today deployed in billions of pieces world-wide to facilitate most of the common daily-life activities. RFID powered devices are found in mobile payment, ticketing, and many other IoT applications. The main drawback of today's RFID architectures is that the modulation and demodulation of the signal is performed with custom analogue and digital circuitry, thus losing on functional flexibility of the end-product. The following paper presents the implementation of an edge-computing architecture based on a proprietary NXP RISC-V core to perform Digital Signal Processing operations, thus supporting the receiving chain of an RFID modem and improving flexibility of the end product. We will describe the main characteristics of said architecture, and how it is instantiated in an existing NXP RFID system. This paper also mention the results obtained by implementing a selected FW feature running on the proposed microprocessor.

Introduction

Radio Frequency Identification (RFID) is an ubiquitous technology with many applications ranging from identification to mobile payment, as well as wireless charging. A considerable amount of analogue and digital signal processing is required on all RFID integrated circuits to achieve high performance and reliable communication, while keeping engineering and manufacturing cost low.

Every modem unit of RFID controllers must be able to support multiple communication standards in different operative configurations and environmental conditions. This is achieved by means of an extensive use of custom digital signal processing (DSP) logic, which is tuned to meet the final product requirements at the expense of full functional flexibility. The resulting pre-silicon engineering and verification effort can be unacceptable from the business perspective and limit the end product evolution. Additional limitations of this approach are that the final chip is not adaptable to different communication standards [1], as well as its performance might be negatively impacted by unexpected silicon non-linearities.

One way to balance chip-resources with the growing need for flexibility is to consider the adoption of microprocessors that are able to perform DSP instructions. In contrast to a specialized signal processing realized with custom digital logic, a microprocessor provides the wanted flexibility at the cost of potentially higher resource usage (e.g. memory demand). Additionally, higher clock rates might be required to meet the end-application performance, which has an impact on the total power consumption.

This paper presents the implementation of an edge-computing microprocessor architecture based on a proprietary NXP RISC-V core to deal with the described problem statement. The developed core is able to execute real-time DSP operations, thus increasing the flexibility of the receiving chain of the final product at the cost of higher clock rate and silicon area requirements. The proposed solution is currently instantiated in an existing NXP RFID modem prototype, which might be deployed in the IoT global market.

This paper also presents the results obtained by implementing the following RFID application in FW running on the implemented microprocessor system:

- Real-time monitoring of an RF field shape for tag detection within the RF field generated by the reader.

Related Works

To the best of the authors' knowledge, no other similar work is currently published. However, the drawbacks of deploying analogue/digital custom logic to perform real-time DSP operations in wireless communication devices and the theoretical advantages of adopting a microprocessor based architecture as an alternative solution have been analysed in many published studies [1,2].

None of the cited work has proposed a functional alternative to the commonly used analogue/digital custom logic implementations, which renders the presented study a pioneering attempt of edge-computing innovation for RFID applications and potentially many other IoT use-cases.

Features

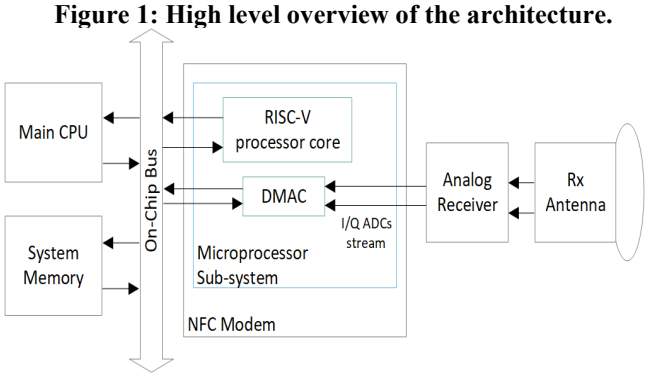
The presented microprocessor architecture is a general-purpose processing module based on a NXP proprietary RISC-V core. It implements the following features:

- Dedicated interface for connection to an existing RFID modem
- On-chip bus manager and subordinate connections
- Floating Point Unit (FPU) unit
- Direct Memory Access Control (DMAC) unit
- Interrupt controller and timers units
- Debugger unit
- Real-time processing of an input data stream

Architecture

The microprocessor based sub-system is connected to an existing NXP RFID modem through a dedicated interface which bundles and routes a selected sub-set of signals from the modem to the microprocessor. The selected signals are transferred to the system memory using a DMAC core via an On-Chip bus manager connection. The collected values are then processed by the RISC-V core to perform the selected operations on the input data. The microprocessor is configured by the main system CPU using an On-Chip bus subordinate connection [Figure 1].

Figure 1: High level overview of the architecture.



Integration proposal

The proposed microprocessor is instantiated right after the analogue front-end of an existing NXP RFID system, and it is able to communicate to the main CPU system through a dedicated On-Chip bus [Figure 1]. The input data that are elaborated by the microprocessor are mainly coming directly from the analogue circuitry after signal processing of the RF field at the receiving antenna (e.g. ADC signals). Since the microprocessor should operate in real-time, its clock should be higher than the RF field frequency to meet the performance requested by the RFID standard of choice. In the study case presented in this paper, the existing NXP RFID modem operates with High Frequency (HF) communication at 13.56MHz, thus the selected microprocessor clock is 54MHz.

Application example and results

The RISC-V based architecture presented in this paper, instantiated as described within an existing NXP system, was verified against an RFID application for tag detection developed in FW which executes the following steps:

1. Real-time observation of the RF field generated by the reader and decoded as I/Q ADCs stream.
2. Monitoring of the RF field signal once the field is turned off.
3. Comparison of the on-off transient shape with known shapes, and determination of the presence of a tag within the generated RF field.

The underlying FW executes a machine learning based recognition algorithm, with an execution time of ca. 200 µs with a 54MHz microprocessor clock.

Future work

This paper aims to set the foundation for a full-fledged implementation of a Software Defined Radio (SDR) for RFID communication, engineered around an open source OpenHW RISC-V core. The future ambition of this research work, which is performed in the context of the European founded TRISTAN project, is to propose a microprocessor architecture that can support most of the features currently implemented with custom digital logic in RFID modems for reception.

The underlying research has already started and the proposed microprocessor architecture is based on an OpenHW CV32E40X RISC-V core [3]. The mentioned core was selected for the presence of an eXtension InterFace (XIF) which eases the Instruction Set Architecture (ISA) extension to support dedicated DSP operation for performance enhancement. At the moment of writing, the CV32E40X RISC-V core is combined with a co-processor unit to perform high throughput filtering. The core is able to demodulate an ISO 14443-2 TypeA 106kBd card response [4], but it requires an unfeasible clock for IoT applications (ca. 500MHz). The next step is to improve the proposed architecture to support reception of an ISO 14443-2 TypeA 106kBd card response with feasible clock, power, area and performance constraints.

References

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