The TETRISC SoC - A resilient quad-core system based on Pulpissimo

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Abstract

Fault-tolerant systems are typically designed for worst-case scenarios and offer sub-optimal performance during normal operation. Configurable systems that adapt to changing circumstances can improve this situation. This paper presents a design that does just that. The TETRISC SoC is a multiprocessor system based on the Pulpissimo platform that uses various reliability sensors to operate its four cores in different performance and fault tolerance modes as needed. This adaptable solution provides optimal performance and reliability for use cases with high requirements, such as avionics or aerospace.

Introduction and Objective

Due to the steadily increasing demand for real-time data processing, multi- and manycore systems are becoming more and more important, especially in the fields of avionics and aerospace. Their inherent level of redundancy can be exploited to adapt performance and fault tolerance to specific situations. Fault tolerance, in particular, plays a major role in this respect, as for example in space, the radiation rate and thus the number of transient errors can quickly fluctuate by several orders of magnitude ([1]).

The development of such systems requires combining different studies from the fields of adaptive fault tolerance and radiation hardening for avionics and space systems across different system levels. The goal of the present research was to implement such a mixed approach on a single state-of-the-art system with open-source hardware. After thorough investigations on possible platforms, we decided to use the Pulpissimo SoC ([2]) as basis. PULPissimo represents the main System-on-Chip controller for all recent multi-core PULP chips, taking care of autonomous I/O, advanced data pre-processing, external interrupts, and more. The main core, called RI5CY, is an in-order, single-issue core with 4 pipeline stages.

The following section provides deeper insights into the architecture that we created and the different approaches that we used to extend Pulpissimo into a resilient and adaptive quad-core platform.

The TETRISC SoC

The resulting architecture has been named TETRISC (TETra Core System based on RISC-V) SoC and is shown in Figure 1. The gray blocks illustrate the original IPs adopted from the Pulpissimo Platform. The newly added components are shown in blue and orange.

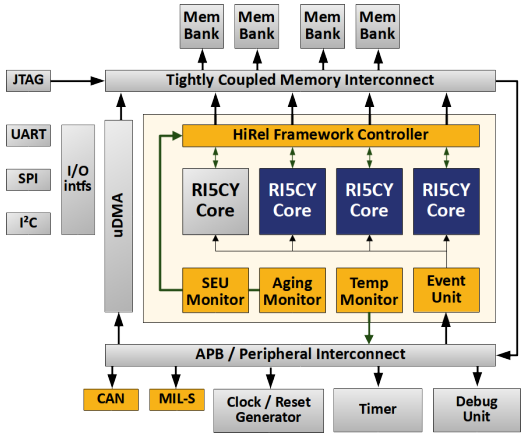

Figure 1: *The system architecture of the TETRISC SoC*

Pulpissimo as multicore

To obtain the necessary degree of redundancy for developing an adaptive and fault-tolerant system, we first extended the Pulpissimo to a quad-core processor structure (see fig. 1). Three additional RI5CY cores, shown in blue, were inserted into the system and connected to the correspondingly expanded interfaces. Above all, the memory interface was reworked and now offers the four cores equal memory access to the entire address space. The separation of the program and data memory of the four cores is done on the software side.

As with the original Pulpissimo platform, interrupts are handled by a (to the cores) external event / interrupt unit. For TETRISC, this was extended accordingly so all four processors can receive interrupts separately.

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