CORE-V™

OPENHW™

OpenHW Group

CORE-V: Open Source RISC-V Cores Commercial Adoption Lesson Learned

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GROUP OPENHW® PROVEN PROCESSOR IP

Outline

- OpenHW Group History
- OpenHW ~ 3 Years Later – Lessons Learned
  - Lesson 1 – Permissive Use
  - Lesson 2 – IP Quality
  - Lesson 3 – Roadmap & Ecosystem
- Summary

OpenHW Launch June 2019

- OpenHW Group Launch at ETH Zurich 11 June 2019
- 13 Initial Sponsors & 2 Projects
- https://riscv.org/proceedings/2019/06/risc-v-workshop-zurich-proceedings/

OpenHW Group Initial Sponsors

Alibaba Group 阿里巴巴集团 · bluespec · CMC MICROSYSTEMS · EMBECOSM® · ETH zürich · imperas · GREENWAVES TECHNOLOGIES · metrics · MYTHIC · NXP · SILICON LABS · onespin · THALES

CORE-V™ Family of RISC-V Cores

- Initial contribution of open source RISC-V cores from ETH Zurich PULP Platform
  - Very popular, industry adopted cores
- OpenHW Group becomes official committer for these repositories

PULP Parallel Ultra Low Power

Core	Bits/Stages	Description
RI5CY	32bit / 4-stage	A 4-stage core that implements, the RV32-IMC, has an optional 32-bit FPU supporting the F extension and instruction set extensions for DSP operations, including hardware loops, SIMD extensions, bit manipulation and post-increment instructions.
Ariane	64bit / 6-stage	A 6-stage, single issue, in-order CPU implementing RV64IMCD extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. It has configurable size, separate TLBs, a hardware PTW and branch-prediction (branch target buffer, branch history table and a return address stack).

- OpenHW Group is a not-for-profit, global organization registered in Canada and Europe. The OpenHW ecosystem is driven by members (corporate & academic) and individual contributors where HW and SW designers collaborate in developing open-source cores, related IP, tools and SW such as the CORE-V Family of open-source RISC-V processors
  - International footprint with developers in North America, Europe and Asia
  - Providing an infrastructure for hosting high quality open-source HW developments in line with industry best practices
  - Strong support from industry, academia and individual contributors worldwide

Industry Members

104+ Members & Partners

Academic Members

104+ Members & Partners

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

Universidade do Minho

Science and
Technology
Facilities Council

Partner Ecosystem

104+ Members & Partners

Accounting, Legal, Banking

Working Groups & Task Groups

- Board of Directors approves elected Chairs of Working Groups and has final approval of working group recommendations

- Technical Working Group
  - Cores Task Group
  - Verification Task Group
  - SW Task Group
  - HW Task Group
- Marketing Working Group
  - University Outreach Task Group

- OpenHW Asia Working Group
- OpenHW Europe Working Group

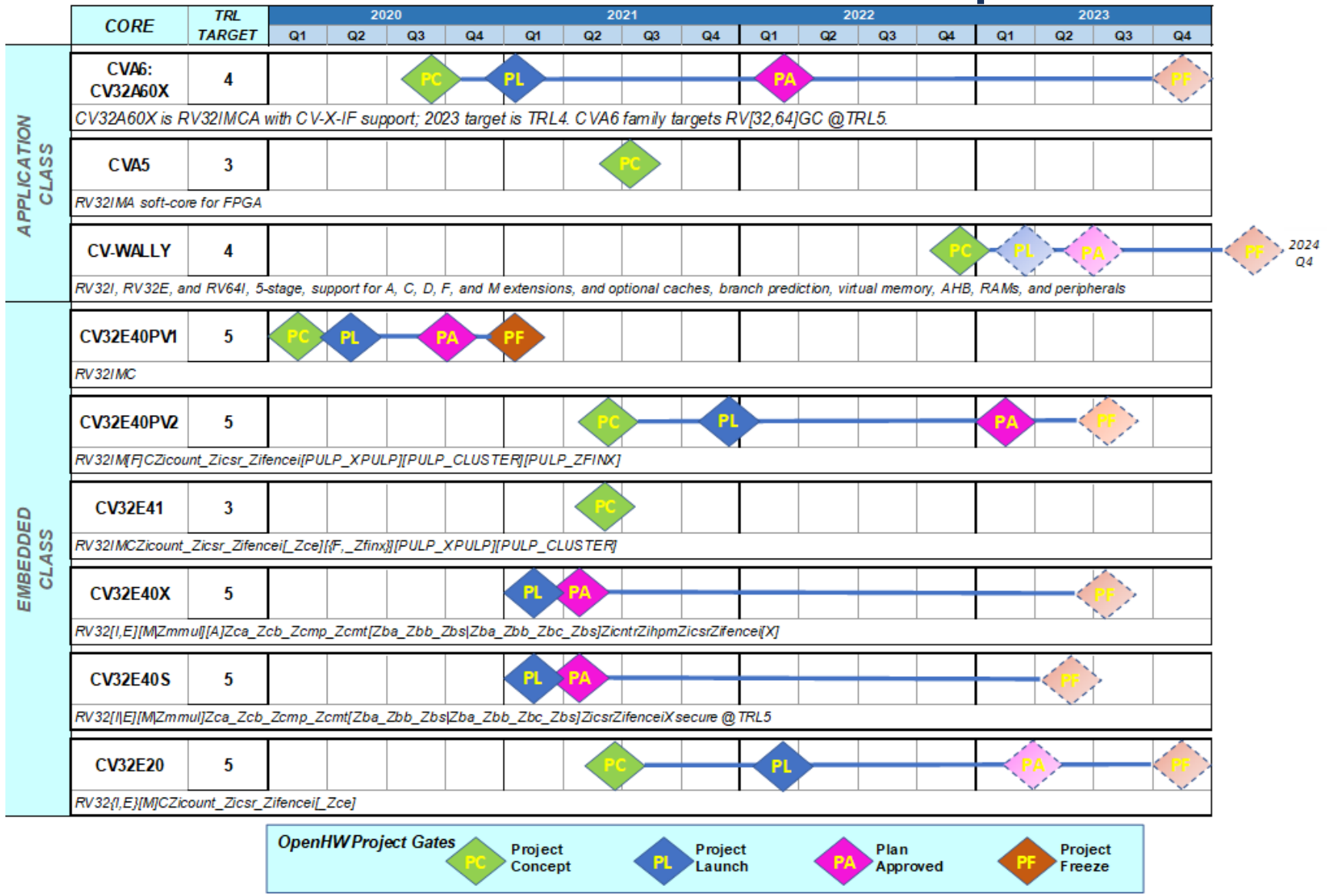
- Together with internal OpenHW Group engineering staff, member company development engineers (FTEs / ACs) establish and execute OpenHW Group projects
  - 20+ active projects across CORE-V RTL, Verification, GCC / LLVM, IDE, RTOS, FPGA, SoC, etc. with more projects in the pipeline

OpenHW Cores Task Group

- Chair: Arjan Bink, Silicon Laboratories
- Vice-Chair: Jérôme Quévremont, Thales Research & Technology
- develop feature and functionality roadmap and the open-source IP for the cores within the OpenHW Group such as the CORE-V Family of open-source RISC-V processors.
- Initial contribution of open-source RISC-V cores from ETH Zurich PULP Platform and the OpenHW Group is the official committer for these repositories

Core	Bits/Stage	Description
CVE4 (RI5CY)	32bit / 4-stage	A family of 4-stage cores that implement, RV32IMFCXpulp, optional 32-bit FPU, instruction set extensions for DSP operations including HW loops, SIMD extensions, bit manipulation and post-increment instructions.
CVA6 (Ariane)	32 & 64bit / 6-stage	A family of 6-stage, single issue, in-order CPU cores implementing RV64GC extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. The cores have configurable size, separate TLBs, a HW PTW and branch-prediction (branch target buffer, branch history table and a return address stack).

CORE-V® Cores Roadmap



OpenHW Collaboration Stats

CoderStats(openhwgroup)

GitHub user name | Get Stats

OpenHW Group

Joined GitHub 27 May 2019

openhwgroup
www.openhwgroup.org
Ottawa, Ontario, Canada

Repo types

Pushed to repos	Main languages	Total issues	Total forks	Total stars	Followers	Following
54	10	769	1627	4171	326	0

Summary

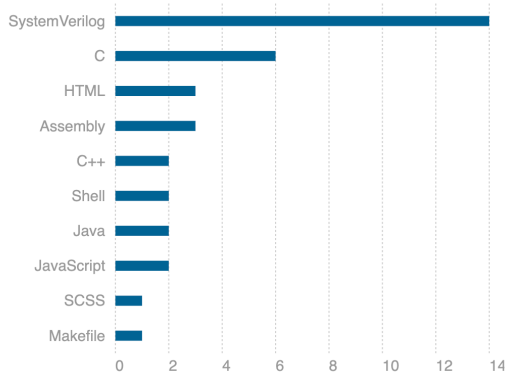
OpenHW Group has 55 repositories on GitHub, the latest 55 with user activity were loaded from GitHub's web service for this evaluation. OpenHW Group has pushed to **54** of these repositories. This is a high ratio congratulations!

10 different main languages were identified across all repos pushed to. The main language is the one with the largest amount of code in a given repository, as identified by GitHub's linguist. Assuming a basic level of proficiency in all these languages OpenHW Group can be considered hyperpolyglot in the world of computer languages. **SystemVerilog** occurs most frequently - 14 times - as the main repo language.

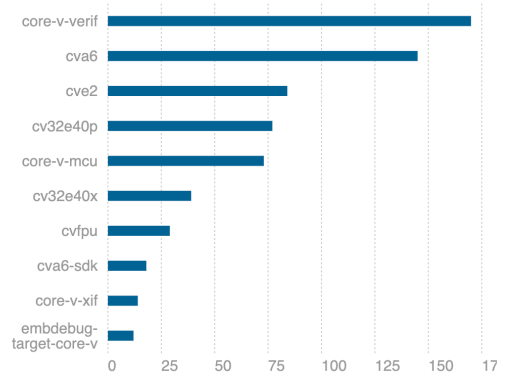
The total number of forks across all pushed to repositories indicates that the GitHub projects OpenHW Group contributes to are actually used by other people.

Rankings

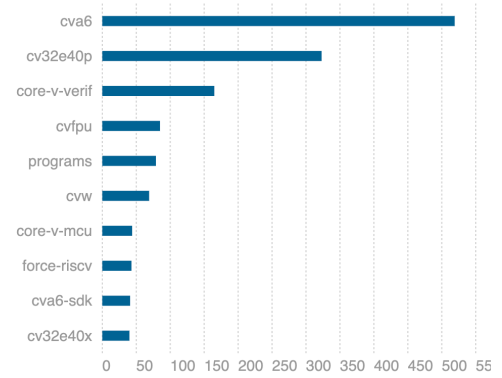
Languages



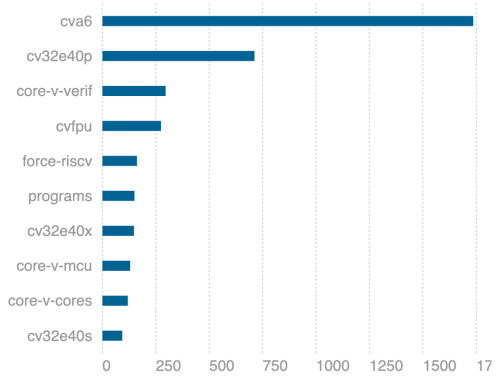
Issues



Forks



Stars



Silicon Labs OpenHW Leadership

"As a leader in secure, intelligent wireless technology for a more connected world, Silicon Labs products need efficient, low-cost, customizable processor cores to realize our customers' performance requirements.

The OpenHW CORE-V CVE4 family of open-source RISC-V cores satisfy these requirements, and Silicon Labs has taken a leadership position within the OpenHW ecosystem to help drive the execution of various CORE-V CVE4 projects.

A range of Silicon Labs SoC products have adopted various CVE4 cores and have launched into high-volume production," said Daniel Cooley, Silicon Labs CTO & Board Member, OpenHW Group.

Thales OpenHW Leadership

"In 2018, Thales joined the RISC-V Foundation to help design the RISC-V open instruction set and above all to rally manufacturers and academics around a subject that is crucial for our sovereignty.

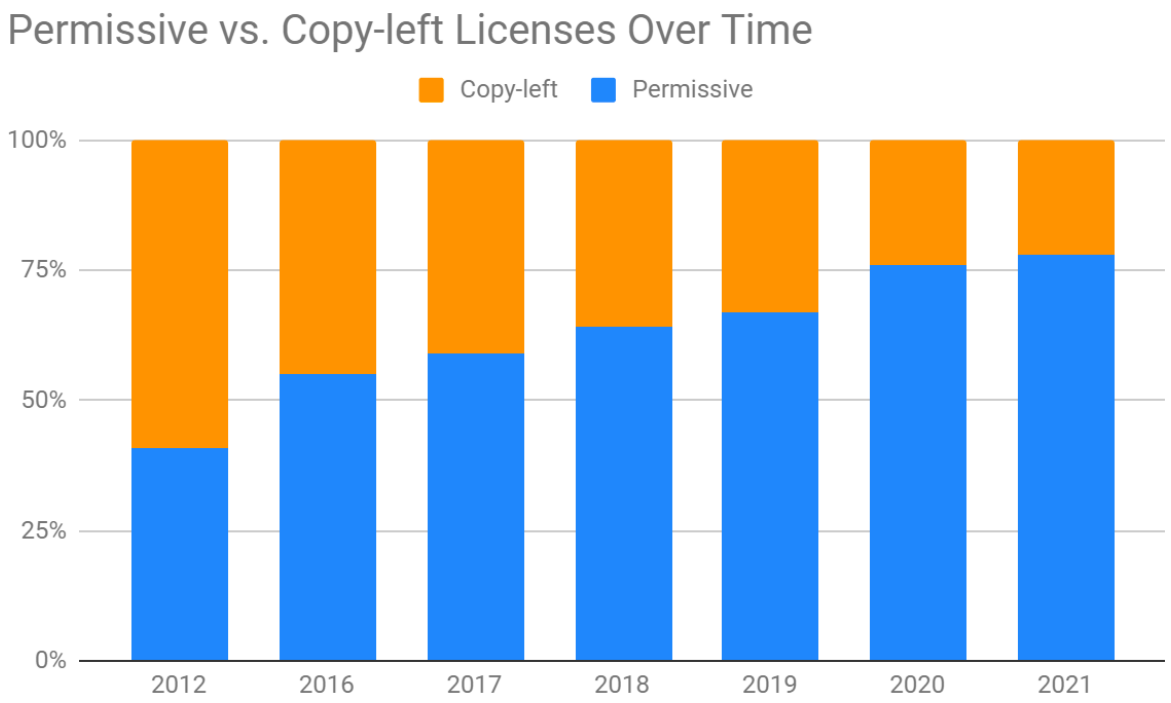
In 2019, Thales was a founding member of the OpenHW Group and has taken a leadership role within open-source hardware communities to design processors for critical embedded systems, particularly in the aerospace, defence and cybersecurity sectors with a particular focus on the OpenHW CORE-V CVA6 processor.

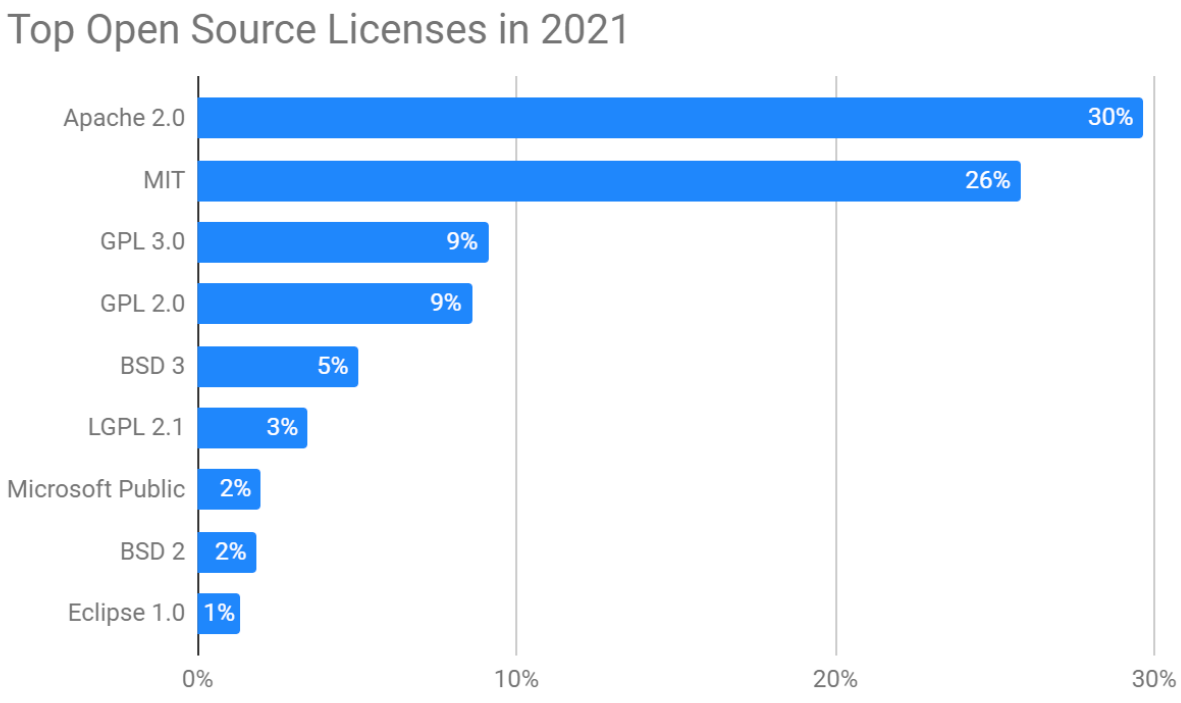
Open-source solutions for hardware as well as software are becoming more integral than ever to Thales's innovation strategy." said Daniel Glazman, VP Software Technologies at Thales.

Open Source HW Adoption Lessons

- Lesson 1 - Permissive use
  - permissive open-source licensing and processes to minimize business and legal risks
- Lesson 2 - IP quality
  - harness community best-in-class design and verification methods and contributions
- Lesson 3 - Roadmap & Ecosystem
  - ensure availability of IDE, RTOS / OS ports, physical design etc. and create a roadmap of cores covering a range of PPA metrics

Open Source License Usage





https://www.whitesourcesoftware.com/resources/blog/open-source-licenses-trends-and-predictions/

HW Companies & Open Source

- Large Systems & Semiconductor companies have very deep patent portfolios
- Copyleft / GPL style licenses are generally seen to pose a greater risk of unwanted patent exposure
- Companies need to see commercial benefit to ‘give back’ and not be forced to give back through license terms
- Apache provides permissive terms with both copyright and patent grants – also, most HW companies have already accepted Apache for SW projects
- But is Apache enough?

Solderpad Hardware License 2.1

- A permissive open hardware license
- Based on, and acts as an exception to, Apache-2.0
- SPDX-License-Identifier: Apache-2.0 WITH SHL-2.1
- Covers physical hardware as well as open silicon and gateware
- Modifies, clarifies and extends various Apache definitions, and the scope of rights to explicitly cover hardware
- Not specifically OSI approved, but we know it falls within the OSI definition of “open source” because any licensee can treat as plain Apache-2.0
- http://solderpad.org/licenses/SHL-2.1/

MOORCROFTS
CORPORATE LAW

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OpenHW Verification Task Group

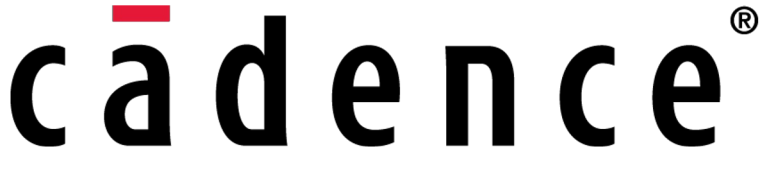
- Chair: Simon Davidmann, Imperas
- Vice-Chair: Jean-Roch Coulon, Thales Silicon Security

- Develop best in class verification test bench environments for the cores and IP blocks developed within the OpenHW Group.

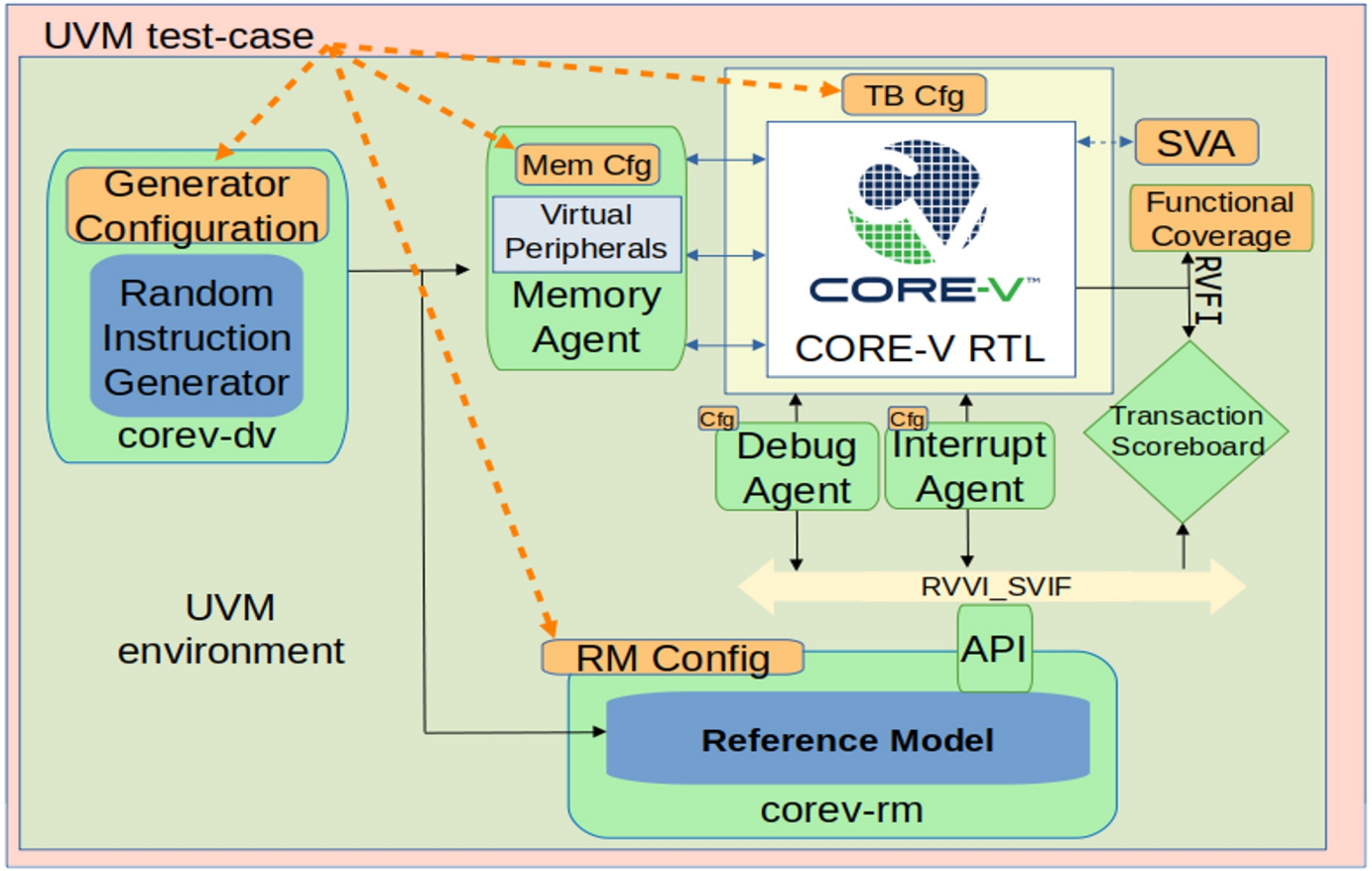
Industry Standard Tools

- Use industry standard languages and verification methods

- Open-Source projects need to fit easily into ecosystem companies' existing EDA tool flow. Leverage the best commercial tools for the job



Next Gen: universal UVM environment for CORE-V Verif



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SW Task Group

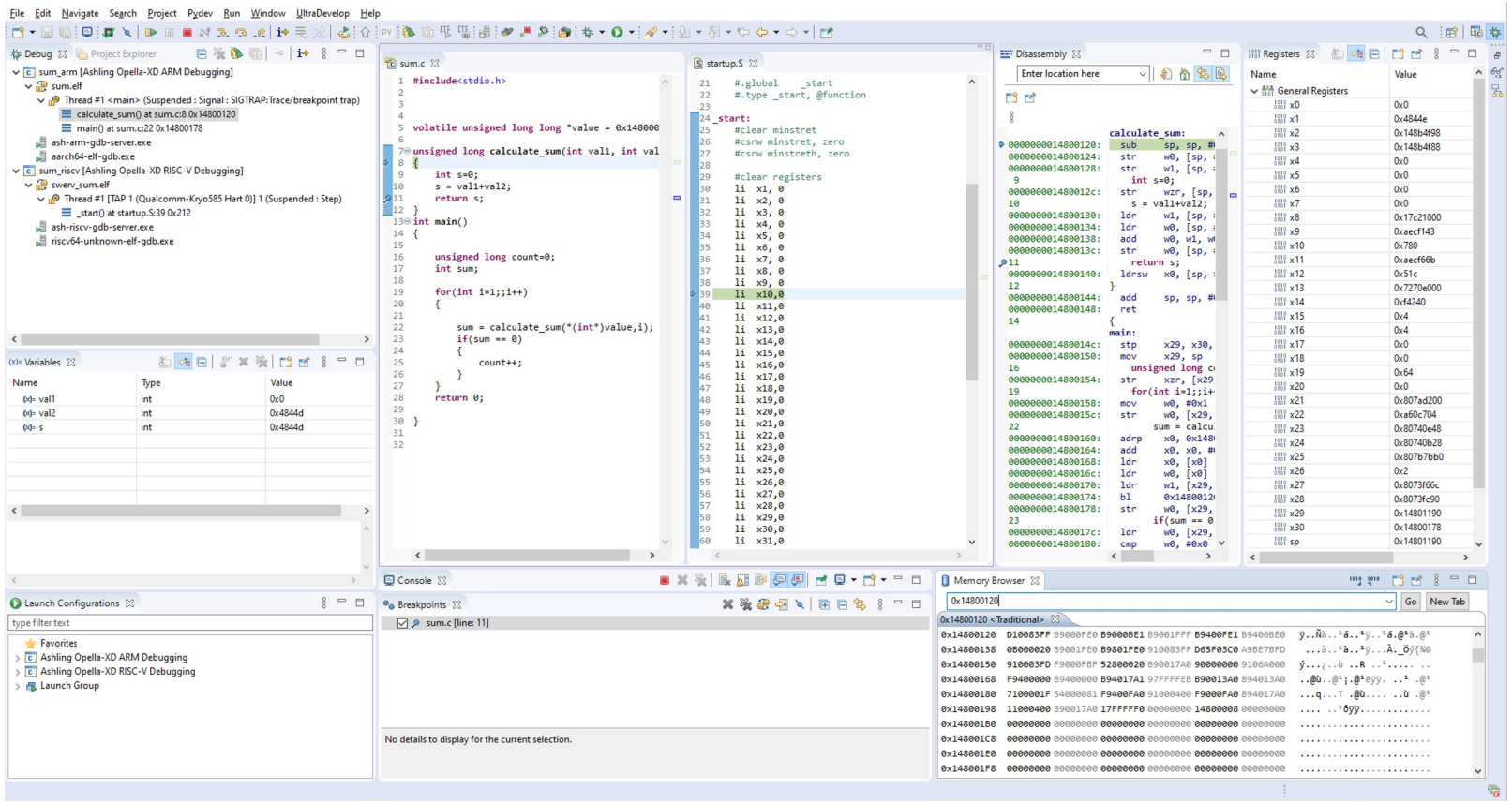
- Chair: Jeremy Bennett, Embecosm
- Vice-Chair: Yunhai Shang, Alibaba T-Head

- Define, develop and support SW tool chain, operating system ports and firmware for the cores and IP developed within the OpenHW Group

- SW TG active projects include: GCC / LLVM, IDEs, FreeRTOS, HAL, CORE-V MCU SDK, etc.

CORE-V® IDE

- CORE-V IDE is an open-source development under the SW TG at the OpenHW Group
- Eclipse based IDE for CORE-V development
- Includes the GCC Toolchain for CORE-V
- OpenOCD Debug Support
- “Ready-to-run” examples for Digilent FPGA boards
- Getting started guides

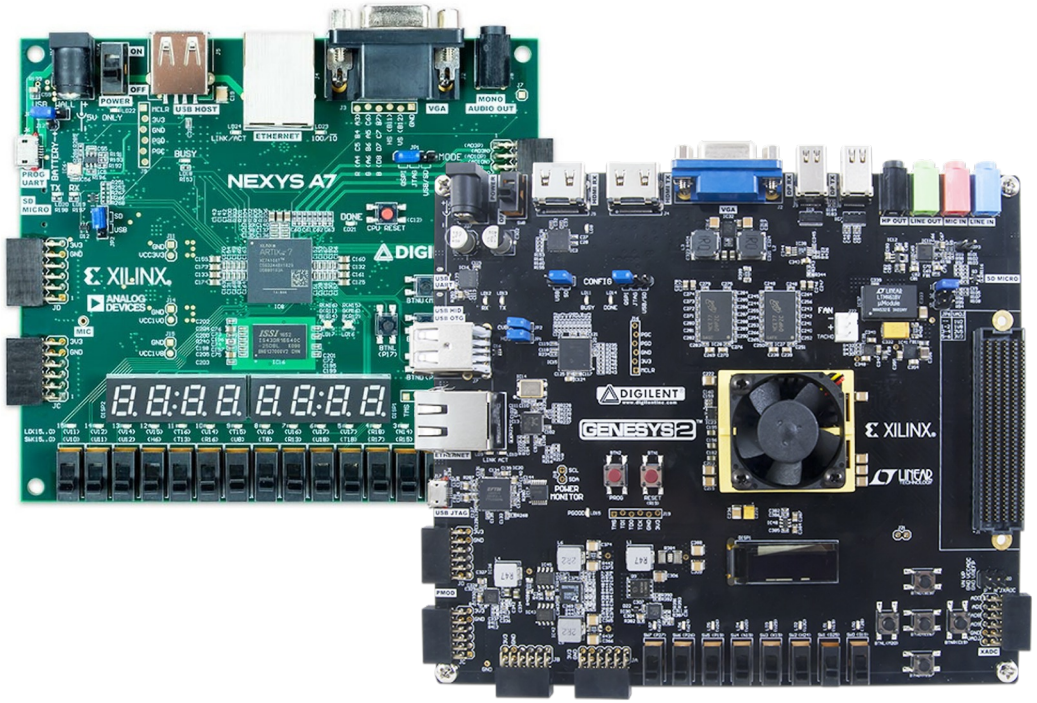


HW Task Group

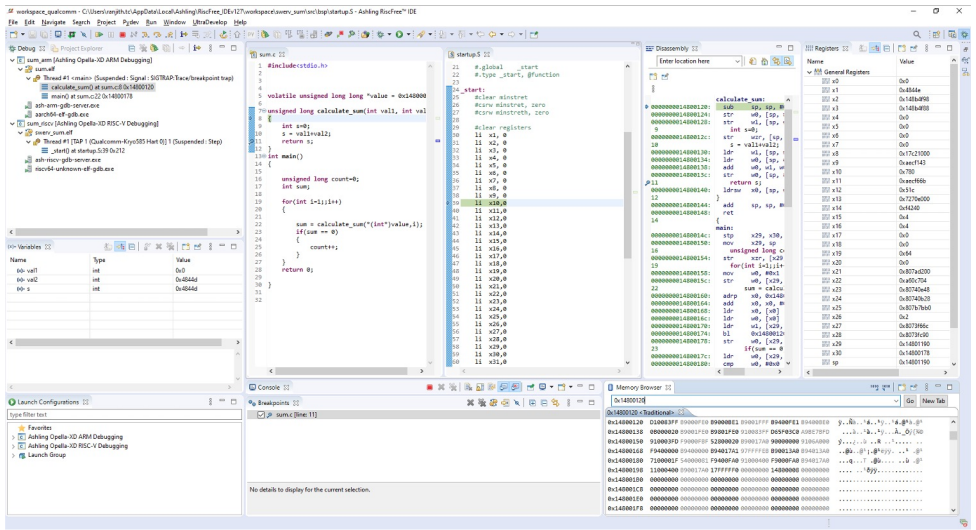
- Chair: Hugh Pollitt-Smith, CMC Microsystems
- Vice-Chair: Tim Saxe, QuickLogic
- define, develop and support SoC and FPGA based evaluation / development platforms for the cores and IP developed within the OpenHW Group.

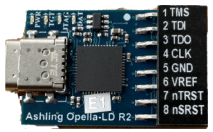
CORE-V® FPGA Emulation

- CORE-V projects leverage Digilent NexysA7 & Genesys2 FPGA boards for soft-core bring up for both CVE4 and CVA6 Families



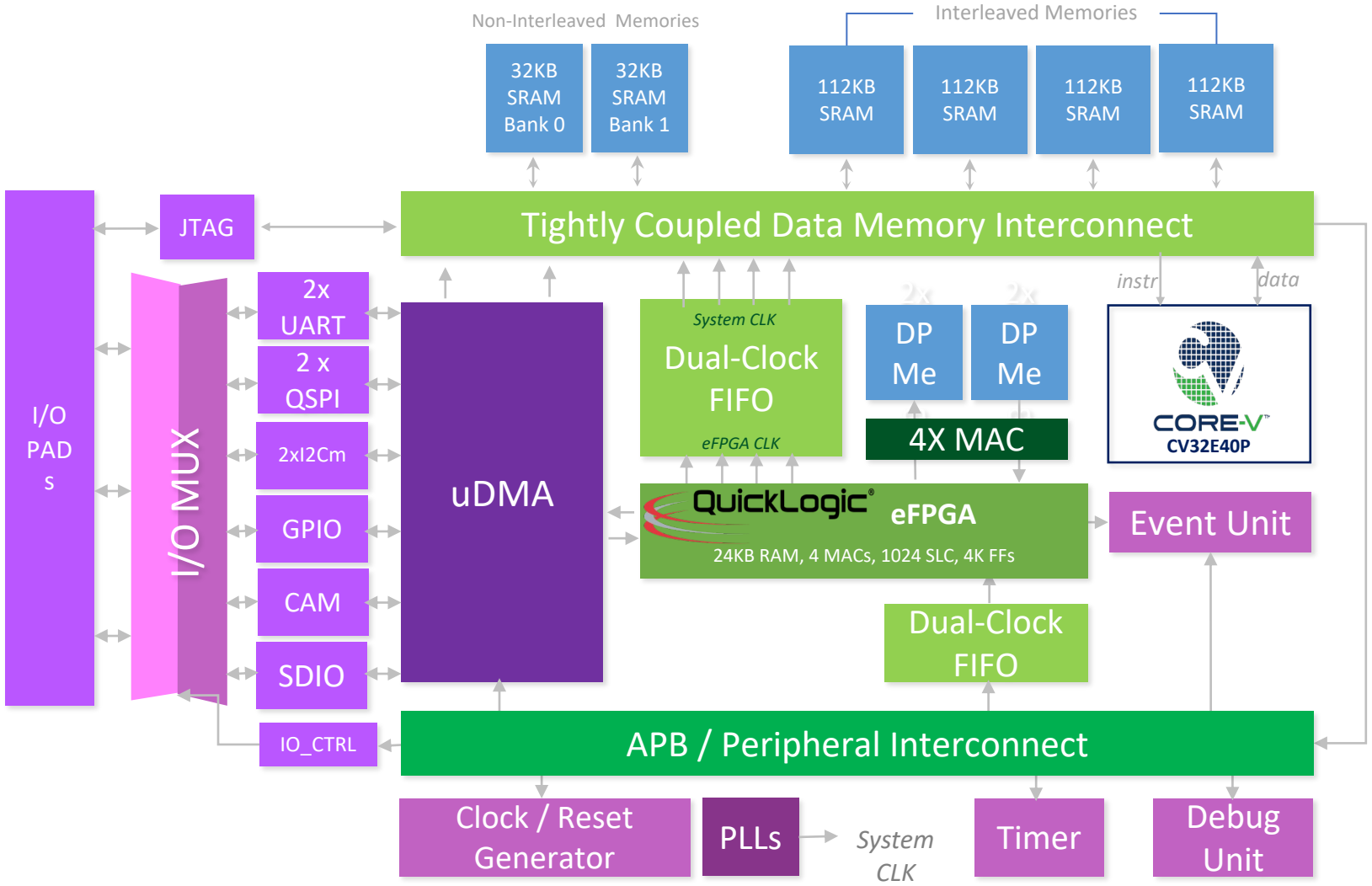
CORE-V™ IDE





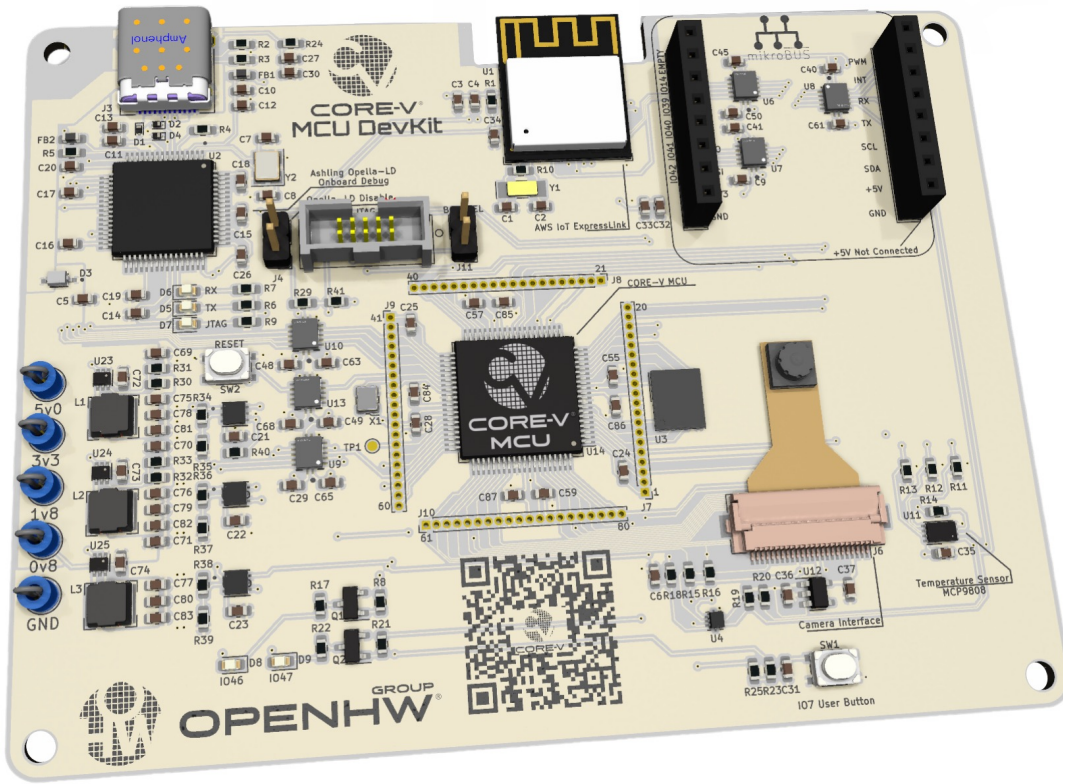
ASHLING Opella LD Debug Probe

CORE-V® MCU in fab now



- Real Time Operating System (e.g. FreeRTOS) capable ~300+MHz CV32E4 MCU
- Embedded FPGA fabric with hardware accelerators from QuickLogic
- Multiple low power peripheral interfaces (SPI, GPIO, I2C, HyperRAM, CAMIF, etc) for interfacing with sensors, displays, and connectivity modules
- Built in 22FDX with GF

CORE-V® MCU DevKit



[OpenHW CORE-V DevKits]

- CORE-V MCU SoC
  - CV32E40P processor core
  - Quicklogic ArticPro eFPGA
  - Global Foundries 22FDX
- Ashling Opella-LD onboard JTAG debug module
- USB-C for terminal and onboard debug access
- JTAG connector for external debug access
- Espressif AWS IoT ExpressLink Module for AWS IoT cloud interconnect
- mikroBUS onboard socket, allowing access to a vast range of mikroBUS modules
- 40 pin expansion header
- I2C temperature sensor
- Early Access CORE-V MCU DevKits can be reserved on the GroupGets campaign page (quantities are limited)

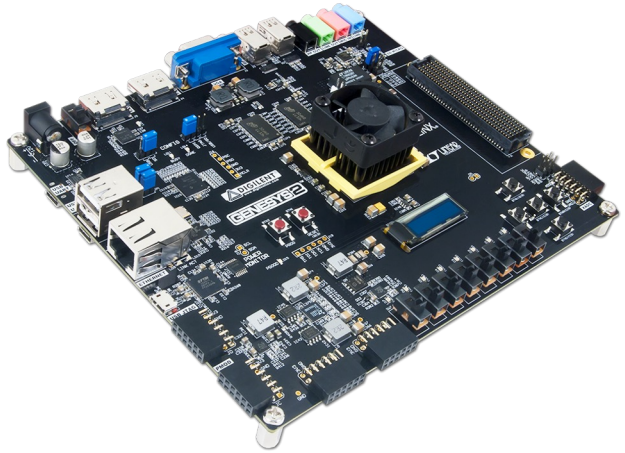
CVA6 – dual core SMP Linux on Genesys2

OPENHW®

OpenPiton

CORE-V®

CVA6-SDK



```
masgia@masgia-Inspiron-5579: ~
File  Edit  View  Search  Terminal  Help
[   12.580437] fff0c2c000.uart: ttyS0 at MMIO 0xfff0c2c000 (irq = 1, base_baud = 4166687) is a 16550
[   13.413954] printk: console [ttyS0] enabled
[   13.413954] printk: console [ttyS0] enabled
[   13.432853] piton_sd:v1.0 Apr 26, 2019
[   13.432853]
[   13.432853] piton_sd:v1.0 Apr 26, 2019
[   13.432853]
[   18.280307]  piton_sd: piton_sd1 piton_sd2
[   18.280307]  piton_sd: piton_sd1 piton_sd2
[   18.313435] libphy: Fixed MDIO Bus: probed
[   18.313435] libphy: Fixed MDIO Bus: probed
[   18.329267] xilinx_emaclite fff0d00000.ethernet: Device Tree Probing
[   18.329267] xilinx_emaclite fff0d00000.ethernet: Device Tree Probing
[   18.345813] libphy: Xilinx Emaclite MDIO: probed
[   18.345813] libphy: Xilinx Emaclite MDIO: probed
[   18.365367] xilinx_emaclite fff0d00000.ethernet: MAC address is now 00:18:3e:02:e3:e5
[   18.365367] xilinx_emaclite fff0d00000.ethernet: MAC address is now 00:18:3e:02:e3:e5
[   18.391571] xilinx_emaclite fff0d00000.ethernet: Xilinx EmacLite at 0x(____ptrval____) mapped to 0x(____ptrval____2
[   18.391571] xilinx_emaclite fff0d00000.ethernet: Xilinx EmacLite at 0x(____ptrval____) mapped to 0x(____ptrval____2
[   18.415544] ehci_hcd: USB 2.0 'Enhanced' Host Controller (EHCI) Driver
[   18.415544] ehci_hcd: USB 2.0 'Enhanced' Host Controller (EHCI) Driver
[   18.437508] usbcore: registered new interface driver usbhid
[   18.437508] usbcore: registered new interface driver usbhid
[   18.448971] usbhid: USB HID core driver
[   18.448971] usbhid: USB HID core driver
[   18.478182] NET: Registered protocol family 10
[   18.478182] NET: Registered protocol family 10
[   18.510941] Segment Routing with IPv6
[   18.510941] Segment Routing with IPv6
[   18.520527] sit: IPv6, IPv4 and MPLS over IPv4 tunneling driver
[   18.520527] sit: IPv6, IPv4 and MPLS over IPv4 tunneling driver
[   18.546628] NET: Registered protocol family 17
[   18.546628] NET: Registered protocol family 17
[   18.561907] Key type dns_resolver registered
[   18.561907] Key type dns_resolver registered
[   18.851667] Freeing unused kernel memory: 6724K
[   18.851667] Freeing unused kernel memory: 6724K
[   18.860994] This architecture does not have kernel memory protection.
[   18.860994] This architecture does not have kernel memory protection.
[   18.874036] Run /init as init process
[   18.874036] Run /init as init process
Starting logging: OK
Initializing random number generator... [   21.273658] random: dd: uninitialized urandom read (512 bytes read)
[   21.273658] random: dd: uninitialized urandom read (512 bytes read)
done.
Starting rpcbind: OK
[   22.539276] random: ssh-keygen: uninitialized urandom read (32 bytes read)
[   22.539276] random: ssh-keygen: uninitialized urandom read (32 bytes read)
Starting sshd: [   22.799293] random: sshd: uninitialized urandom read (32 bytes read)
[   22.799293] random: sshd: uninitialized urandom read (32 bytes read)
OK
NFS preparation skipped, OK

Welcome to Buildroot
buildroot login: root
#
CTRL-A Z for help | 115200 8N1 | NOR | Minicom 2.7.1 | VT102 | Offline | ttyUSB0
```

Open HW ~3 Years Later Lessons Learned

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- OpenHW Group & CORE-V Family of open-source RISC-V cores for use in high-volume production SoCs
  - Visit www.openhwgroup.org for community information
  - Visit OpenHW GitHub https://github.com/openhwgroup for projects
  - Learn more at OpenHW TV

- Follow us on Twitter @openhwgroup & LinkedIn OpenHW Group