VENTANA

The World's Leading High Performance RISC-V & Chiplet Company Powering Next Generation Data Center and Automotive Architectures

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Ventana: The Leading High-Performance RISC-V & Chiplet Company

Balaji Baktha
Founder and CEO

Greg Favor
Co-founder and Chief Architect

Pioneer in Data Center semiconductors: 30+ years experience

- World's first 64-bit ARM with Veloce (Acquired by AppliedMicro)
- Led Marvell BU delivering Data Center class Networking, Communications, Compute, Storage and Wireless infrastructure products

One of the world's leading CPU architects: 35+ years experience

- Architected K6 processor at startup NexGen, acquired by AMD
- Chief Architect at Siara Systems, acquired by RedBack
- Architected first successful 64-bit ARM CPU

THECHANNELCO. CRN CELEBRATING 40 YEARS

10 Hot Semiconductor Companies To Watch In 2023

BY DYLAN MARTIN ▸
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CRN breaks down 10 semiconductor companies that are driving the market with new innovations — or are on the verge of doing so — while navigating the tough economic environment.

DATA CENTER WORLD INNOVATION challenge WINNER

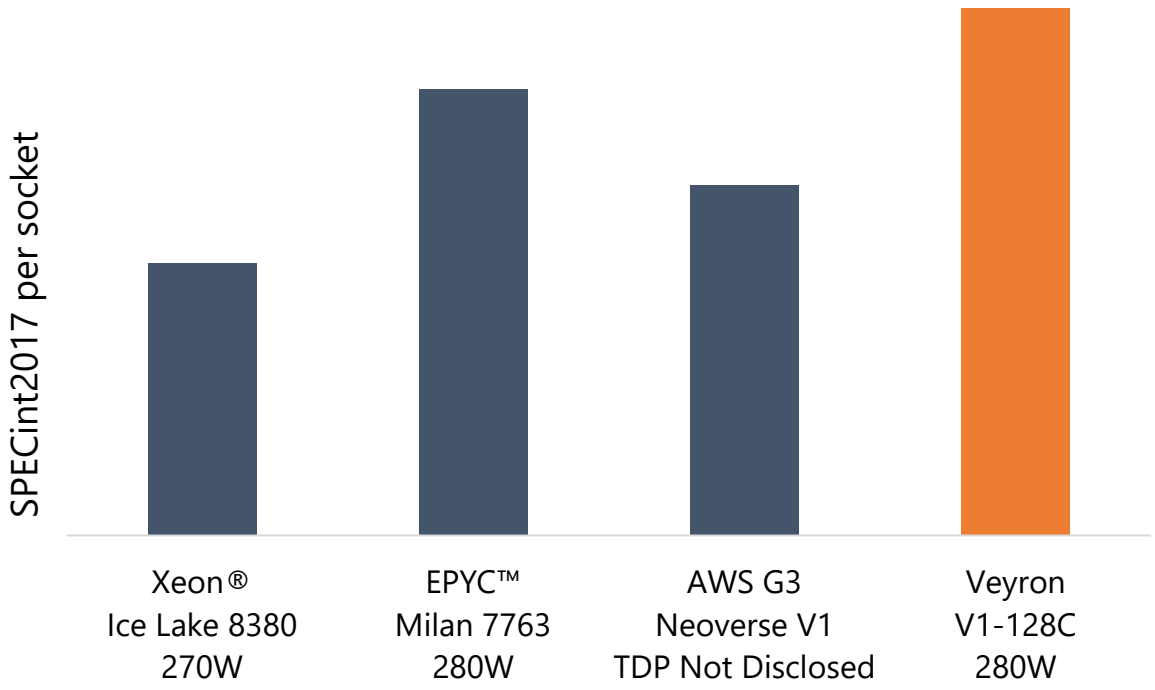
Most Influential Founding Team 2023

Founded in 2019 by industry veterans with a proven track record of delivering Data Center class processors

Veyron V1: World's First Data Center Class RISC-V Processor

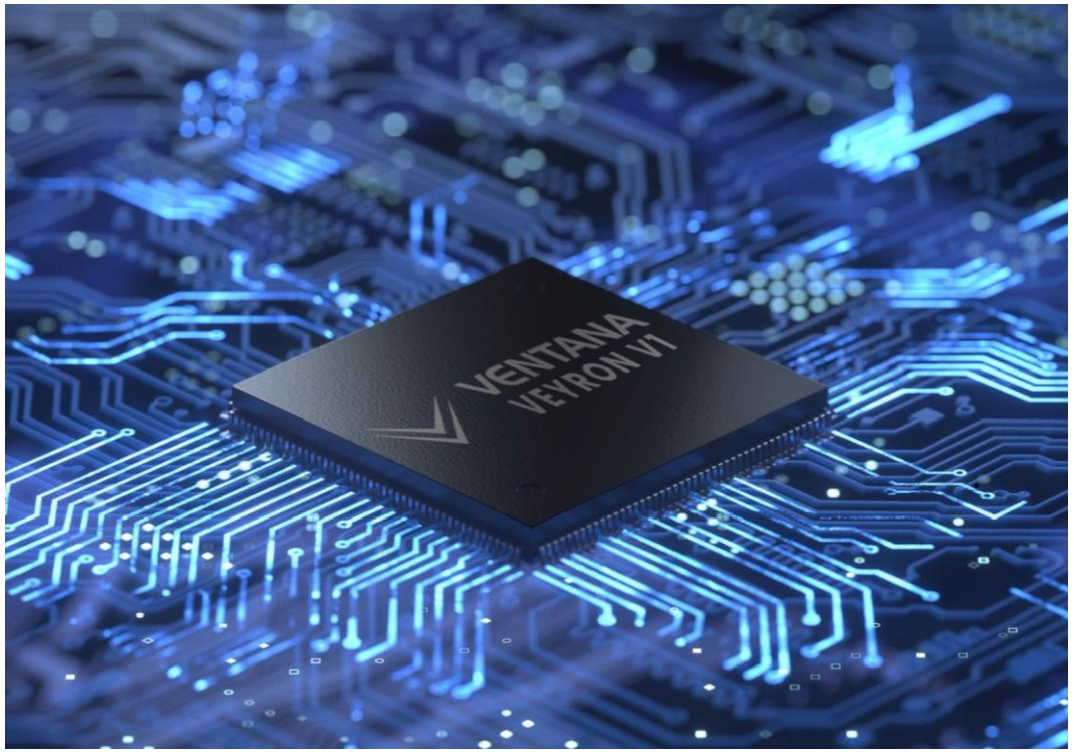
Highest Performance RISC-V CPU

3.6GHz in 5nm process technology



ASSP Based on High Performance Chiplet Architecture

Significant reduction in development Time and Cost compared to prevailing monolithic SoC model

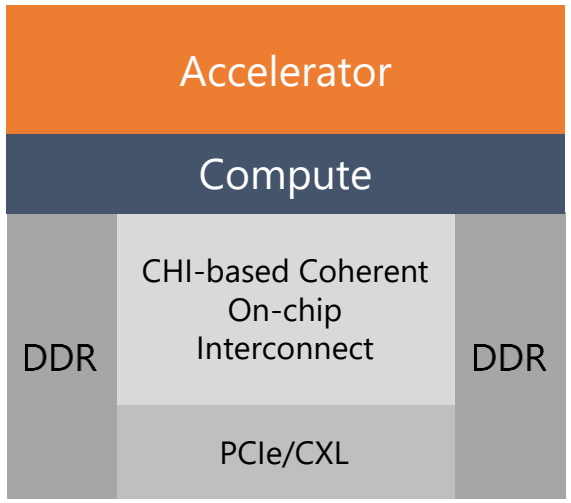


Disruptive ROI: Highest Single Socket Performance at Compelling Perf/Watt/$

The Semiconductor Innovator's Dilemma

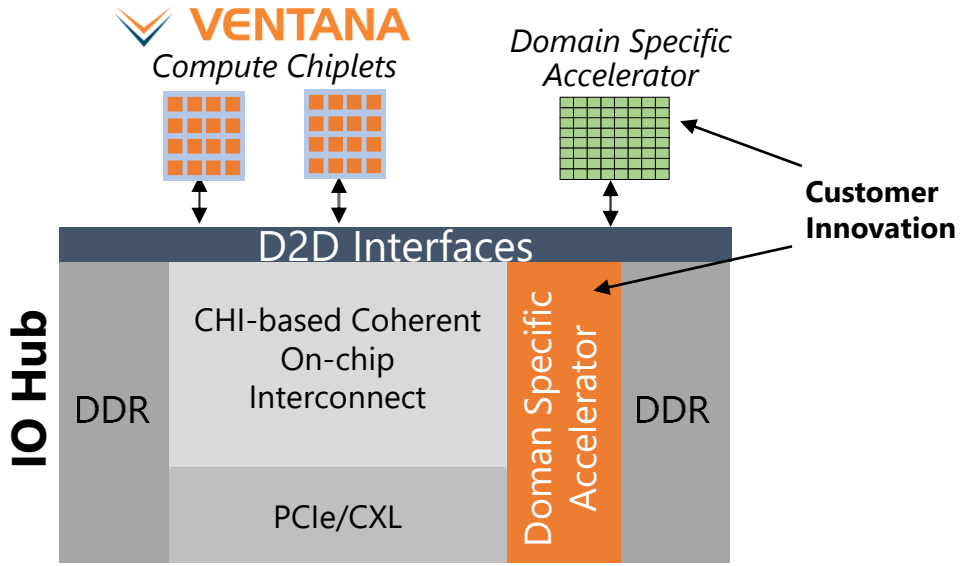
- Semiconductors are the foundation of the modern economy
- Unrelenting massive semiconductor consolidation since 2008
- Led to monopoly in each of the semi markets
- Average lifecycle of products is extended from 18 months to 3 years due to the lack competition
- No room for innovation and differentiation
  - OEMs are forced to use silicon from limited sources
- OEMs cannot build their own SoCs
  - Very high development cost: $100-200M per project
  - Incumbent ISAs don't allow them to innovate
- How do you break the cycle?

Dilemma to Opportunity!



Monolithic SoC

- **TTM: 3+ years**
- **Development cost: $100M+**
- Leading edge process node
- Fixed performance
- Large die/high unit cost
- Risk of incorrect definition by time it comes to market

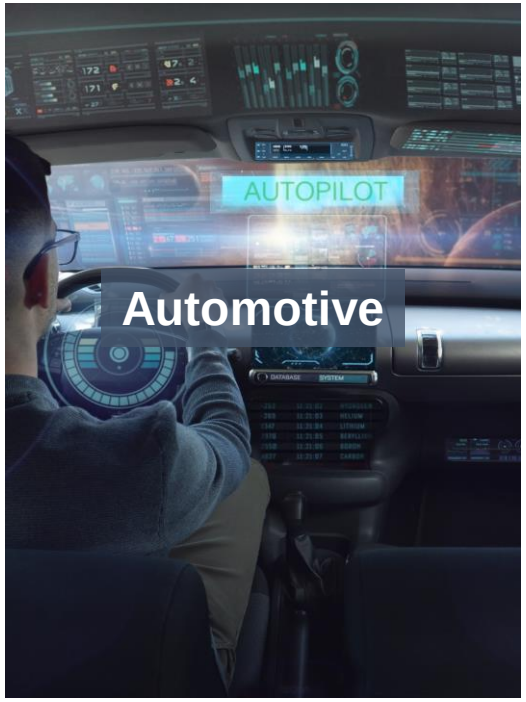


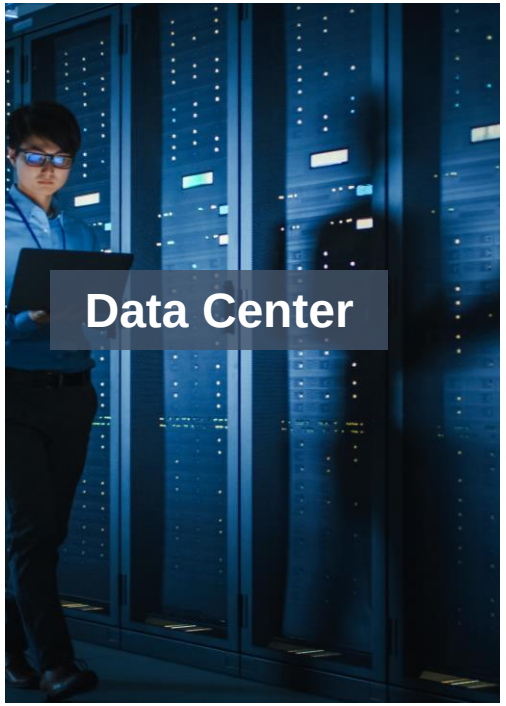
Chiplet-based SoC

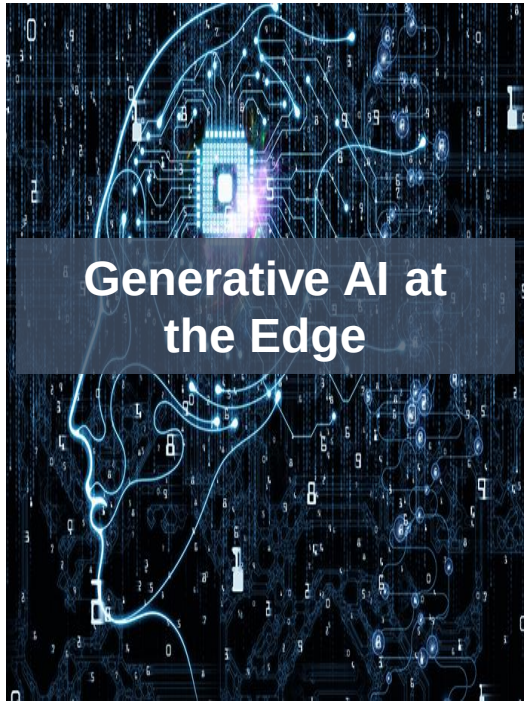
- **TTM: ~1 year**
- **Development cost: < $25M**
- Each chiplet in optimal process node
- Scalable Compute, Accelerator and I/O performance
- Cost optimized solution
- Chiplets introduce the concept of late binding and scalability

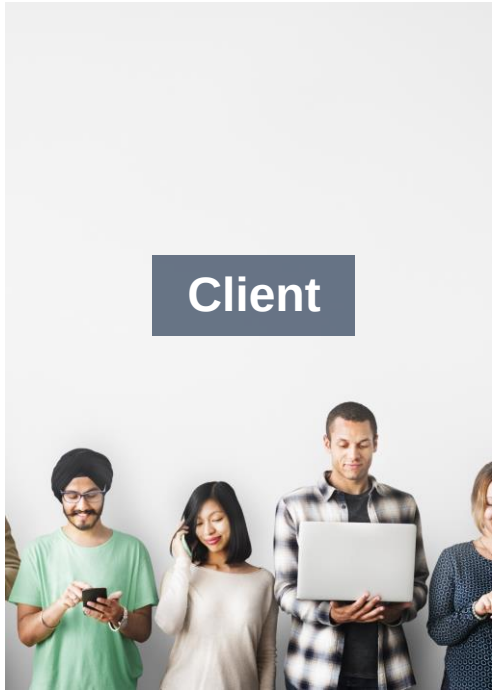
Open Hardware Innovation Led by RISC-V and Open Chiplet Architecture

European Semiconductor Renaissance with Ventana







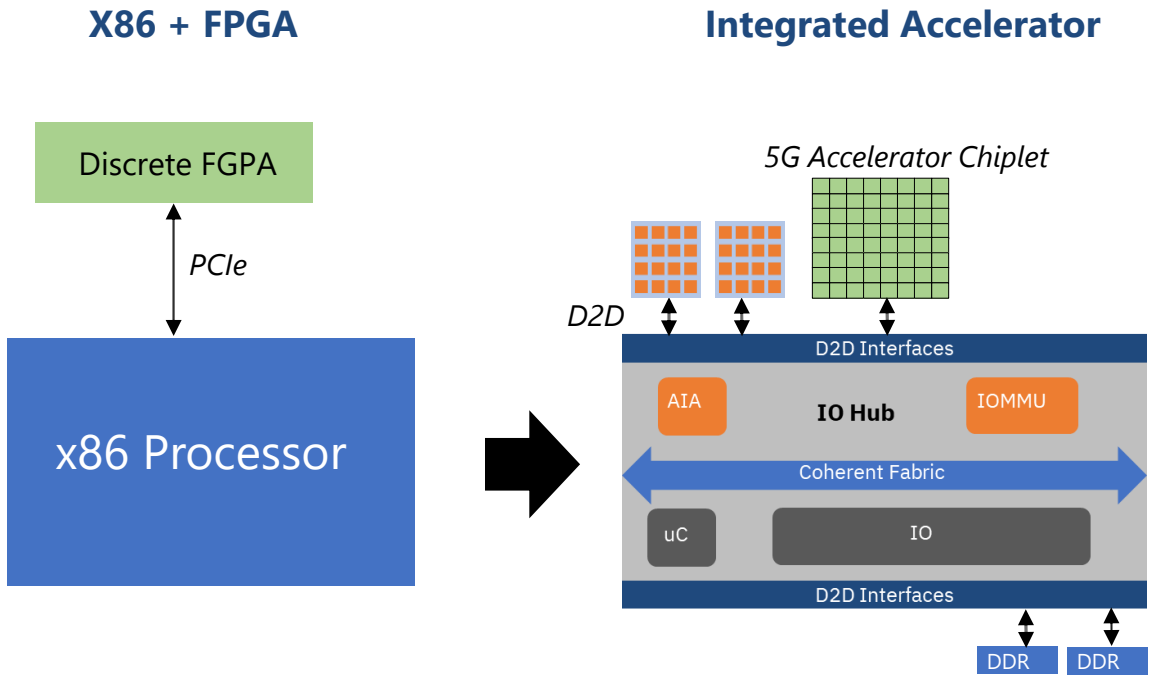


- Zonal architectures are a compelling opportunity to innovate and differentiate with Veyron Chiplets and Cores in ADAS, Infotainment (IVI), and Telemetry
- Sovereign Data Centers with Security & User Privacy
- Explosive use cases of Generative AI at the Edge

RISC-V and Composability Enable Next Generation Workload Efficiency

- Hardware-Software co-design and Domain Specific Acceleration using RISC-V's Extensibility
- Composability: Right-sized Compute, Memory, & IO
- Late-binding: CSSP vs ASSP
- Maximize Socket performance and Perf/W/$$
- Supply chain diversification and resilience

Example: Custom Solution for 5G Base Station

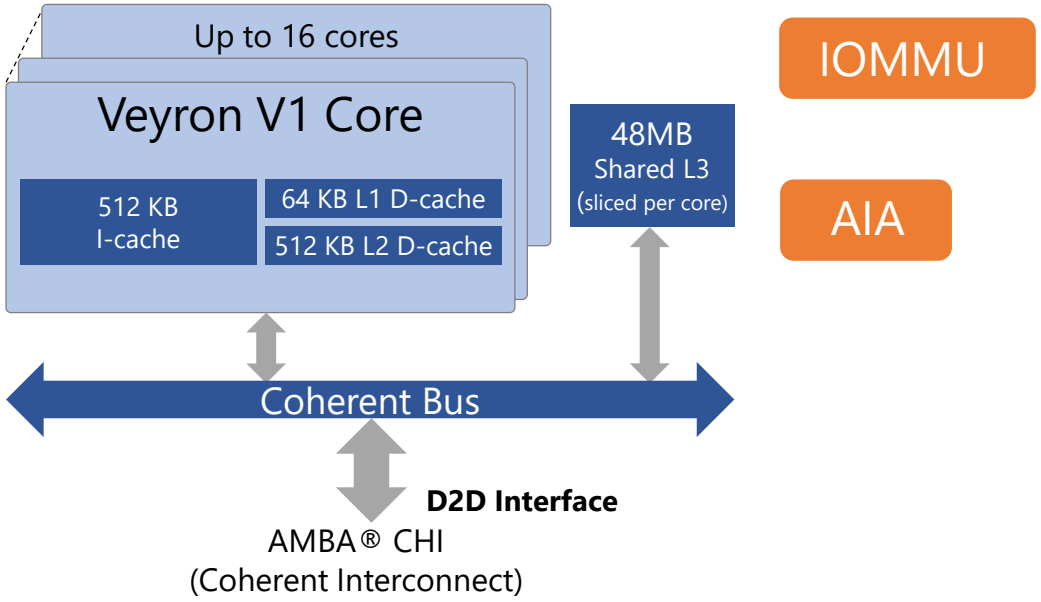


10x Performance/W/$

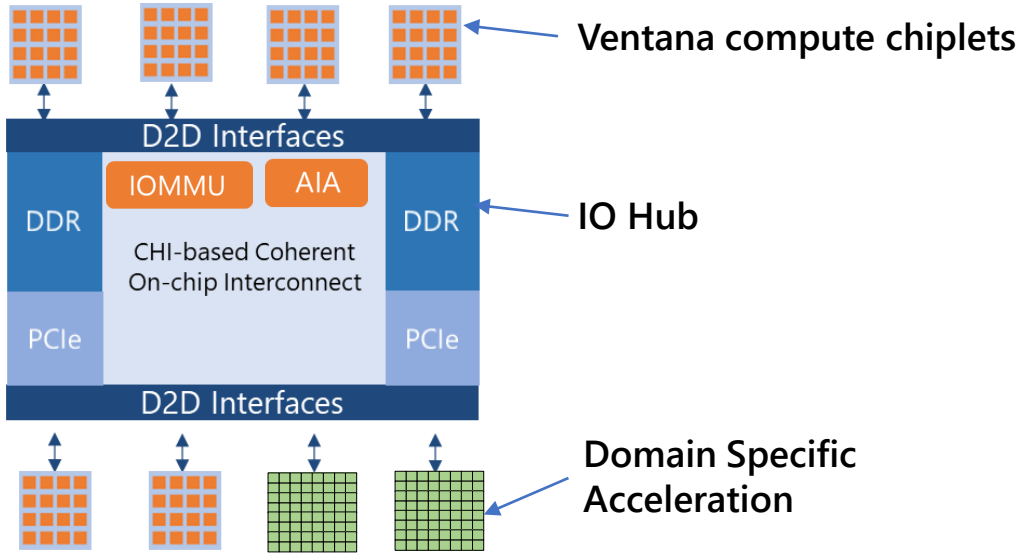
Open Hardware Innovation Leveraging RISC-V and Chiplets

Ventana Veyron: Server Class RISC-V IP + Chiplets

Veyron High Performance RISC-V CPU IP



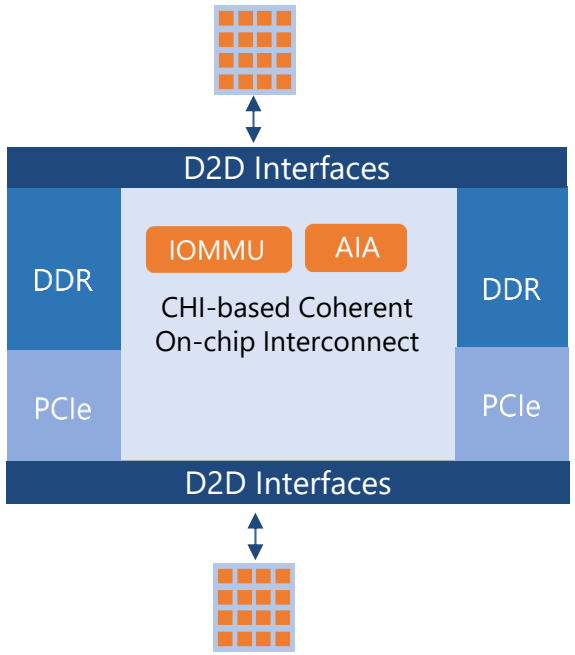
Veyron Chiplet Solutions



- Eight wide, aggressive out-of-order instruction pipeline
- High core count multi-cluster scalability (Up to 192 cores)
- Advanced side channel attack mitigations
- Comprehensive RAS features
- IOMMU & Advanced Interrupt Architecture (AIA) system IP

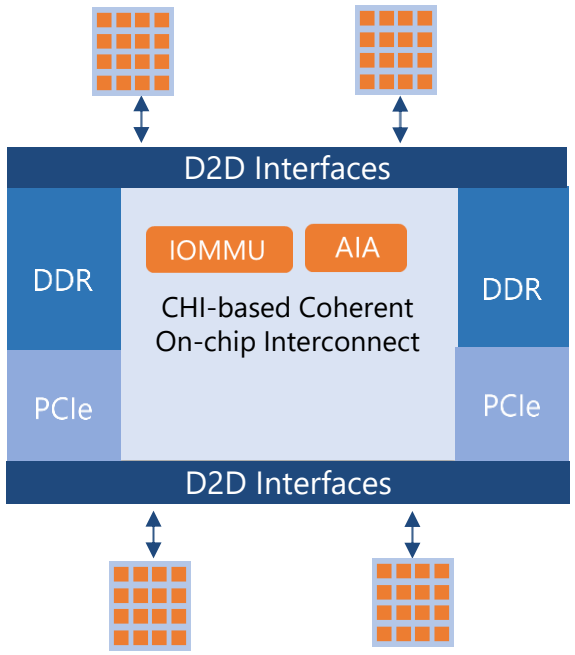
- Veyron compute chiplets
  - In latest process node technology
  - Scalable CPU performance/count
- IO Hub
  - Implemented in process node of choice
  - Customized for application requirements
- Custom Domain Specific Acceleration
  - Low-cost process node

Scalable Architecture for Server-class Compute



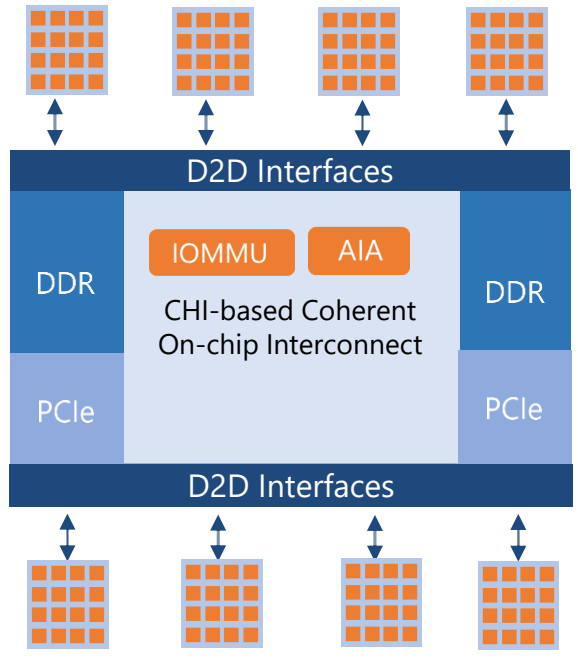
2 chiplets (32 cores)

Entry level server



4 chiplets (64 cores)

Mid level server



8-12 chiplets (128-192 cores)

High end server

Realizing Efficient Chiplet D2D PHY

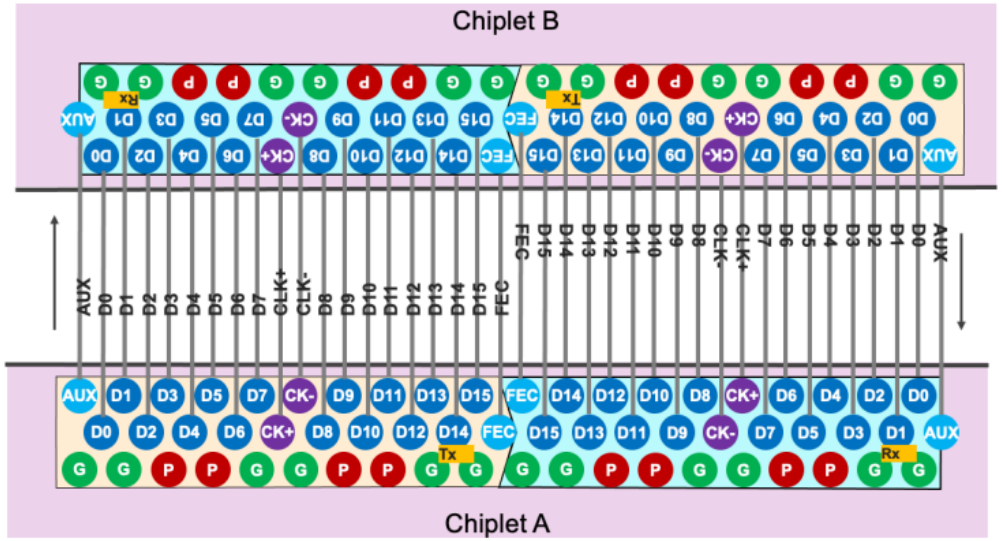
Requirements

- Power efficient
- Small area overhead
- High data rates

	PCIe Gen5	BoW-Fast
Power Efficiency pJ/bit	7	0.55
Area Density Tbps/mm2	0.1	0.69

Parallel D2D interconnects such as UCIe or BoW offer much lower power, area, and complexity overhead compared to serial/ SERDES based solutions like PCIe

Example Parallel D2D Interconnect:
BoW Minimal Bidirectional Refence Link



D2D Refinement Required for Automotive

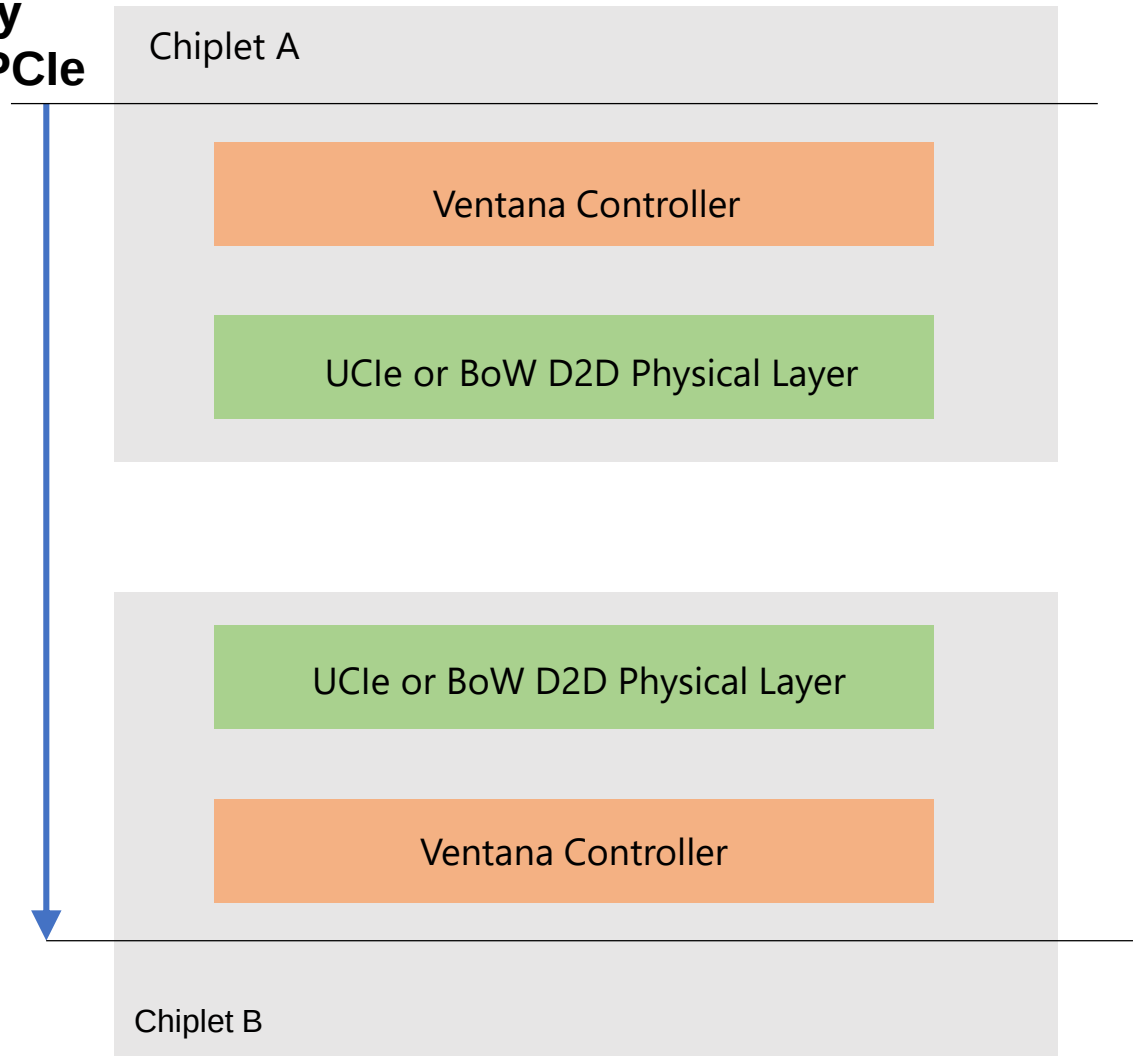
- Failure predictability through monitoring
- Detection & reporting of failures

Pioneering Efficient Chiplet Interconnect Controller

Requirements

- Low D2D latency
- Predictable memory performance
- Standard SoC buses and networks must map easily to D2D transport
  - CHI, AXI, …
- HW memory coherency for efficient support of accelerators

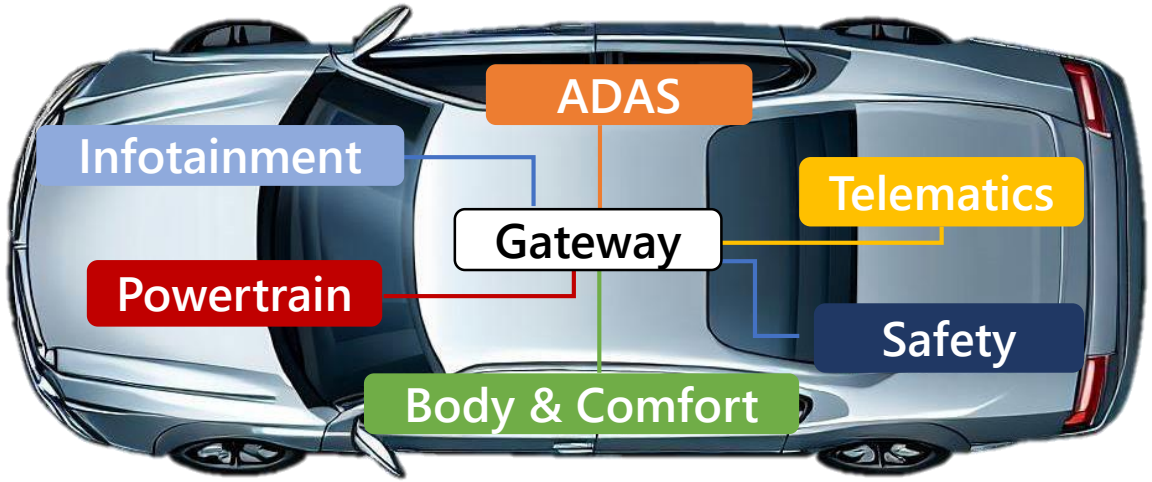
< 7ns latency
vs 100ns+ for PCIe



Ventana has developed a low latency controller IP which maps standard, coherent SoC buses to D2D PHY

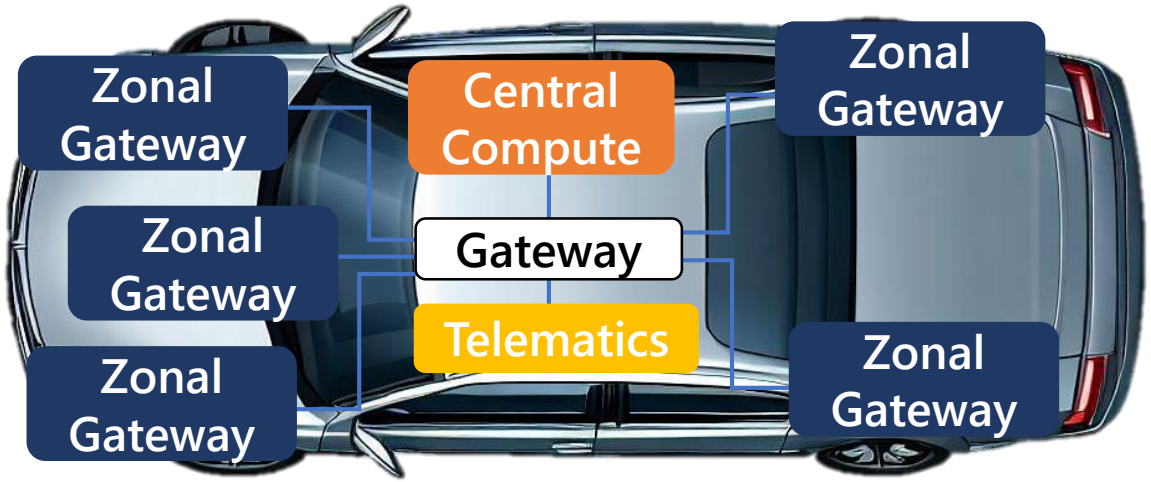
Automotive Following Server Architecture

Today: Domain Architecture



- Dedicated, lower performance controllers
- Increasing hardware varieties
- Fragment code development environments
- Not easily upgraded or scaled

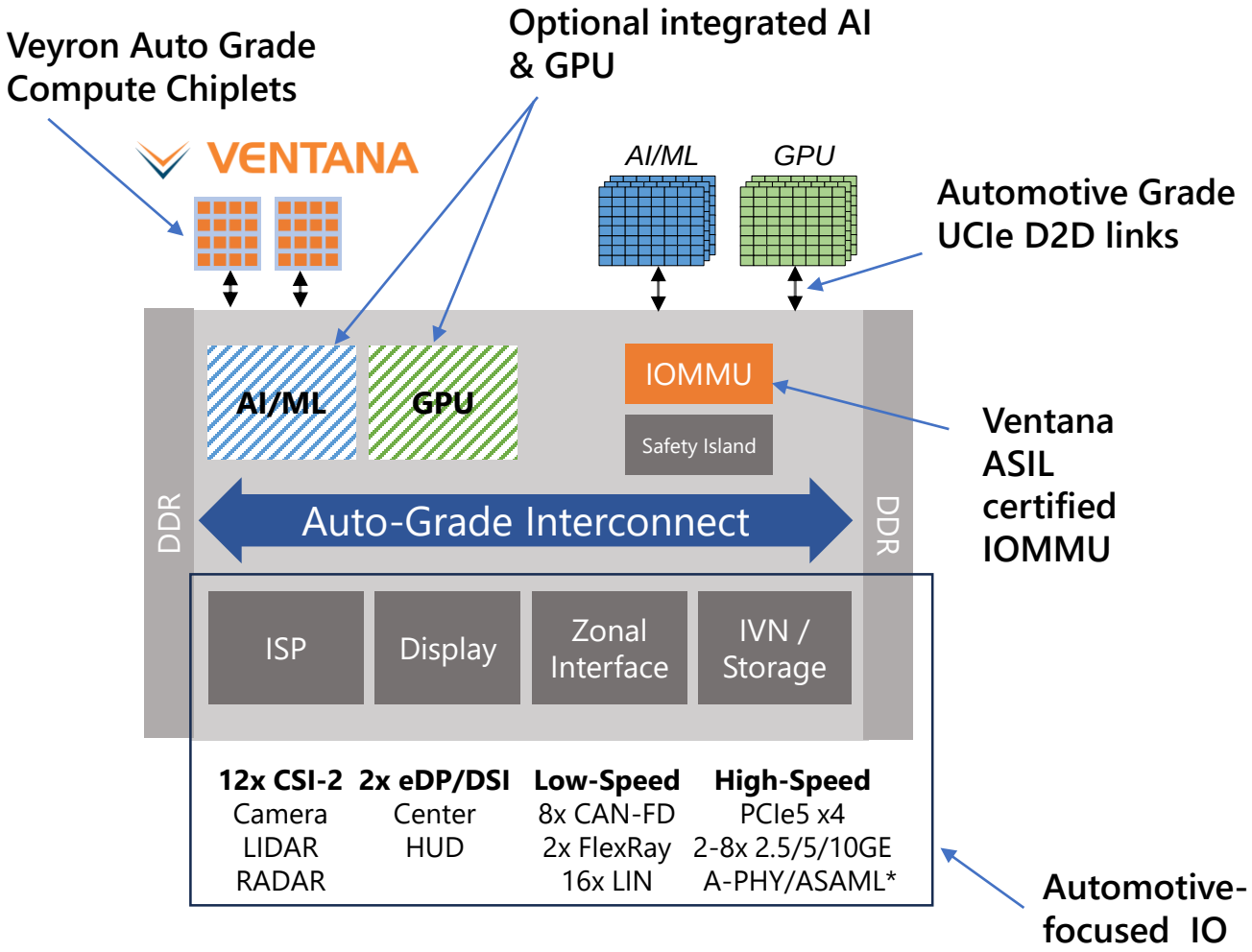
Future: Zonal Architecture



- Centralized high-performance compute
- Unified software environment
- Efficient development
- Scalable and easy to develop hardware

Same RISC-V + Chiplets concept applies

RISC-V and Chiplets Driving Innovation in Automotive



- Automotive can benefit from same cost efficient chiplet architectures to create differentiated platforms
- Ventana ASIL certified chiplets and IP
- Partners create automotive Hub
- Accelerators can be integrated in Hub or scaled up in chiplets

Ventana: Leadership in Action

1. Performance Leadership

2. Contribution to the RISC-V International Community

Member of Board of Directors	Balaji Baktha
Vice-Chair of Technical Steering Committee	Greg Favor
Chair of Privileged Architecture Standing Committee	Greg Favor
Chair of Platforms Horizontal Sub-Committee	Kumar Sankaran
Chair of CacheOps Task Group	David Kruckemyer
Chair of Marketing Events Committee	Omar Hassen
Vice-Chair of Debug Task Group	Paul Donahue
Co-author of Advanced Interrupt Architecture	Greg Favor
Chair of Hypervisor SIG	Anup Patel

Greg Favor

'21 RVI BoD Technical Leadership Award
'20 RVI BoD Technical Contributor Award

Anup Patel

'22 RVI BoD Technical Leadership Award

3. Driving the RISC-V Software Ecosystem…

Founding Member of RISE to Ensure RISC-V Software Readiness

Mission

- Accelerate the development of open source software for RISC-V
- Raise the quality of RISC-V Platform software implementations
- Push the RISC-V Software ecosystem forward and align partners' efforts
- Ensure RISC-V is a tier 1 platform for all tools and libraries
- Accelerate RISC-V adoption for Client and above segments

In Closing …

- RISC-V, Chiplets, and Open Standards are the way forward for the next generation of semiconductor innovation
- Ventana leads the market with the Veyron CPU cores and chiplets
- Ventana is uniquely positioned to help revitalize the European semiconductor industry

VENTANA

Thank You