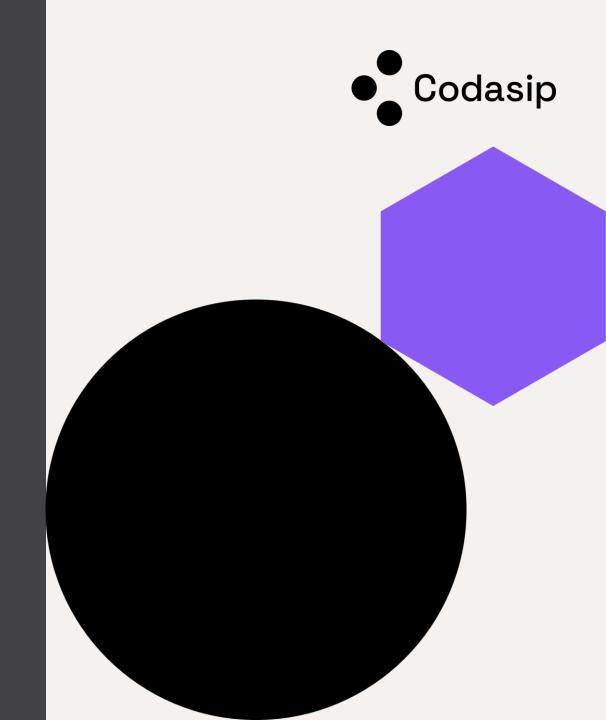


RISC-V customization, HW/SW co-optimization, and Custom Compute

RISC-V Summit Europe

Brett Cline

June 6, 2023



→ Traditional approach to hardware design



Flexible but slow..?

Choose a generalpurpose core and optimize software.

...or fast but hard coded?

Implement fixedfunction hardware circuits.



You don't have to chose any longer.

→ A new disruptive force



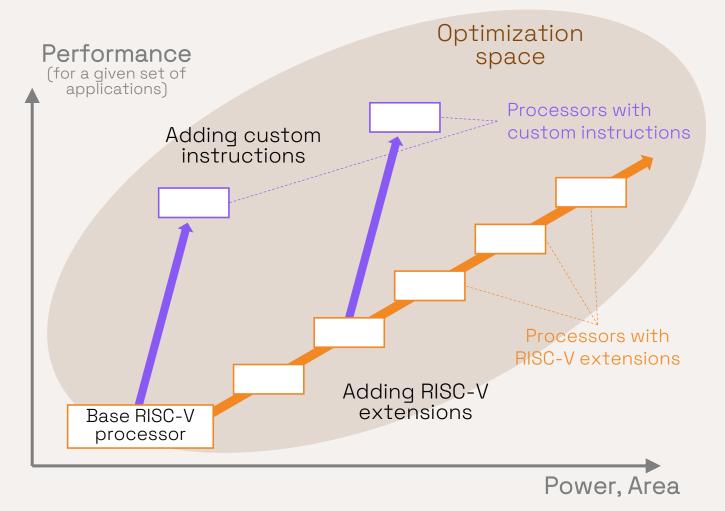


- Open ISA
- Growing ecosystem
- No restrictions
- Customization allowed, and encouraged
- → Counters end of scaling laws
- → Best ISA for Custom Compute

→ Custom instructions for unique workloads

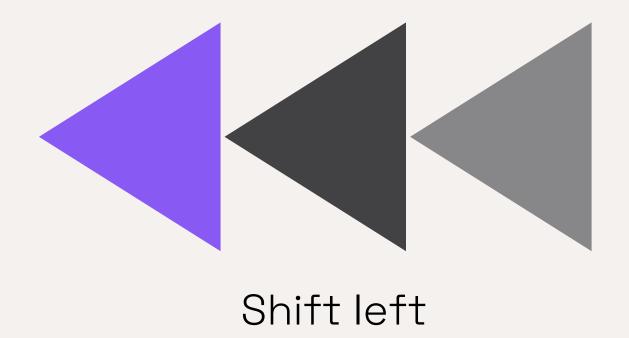


5



→ Hardware/software co-optimization









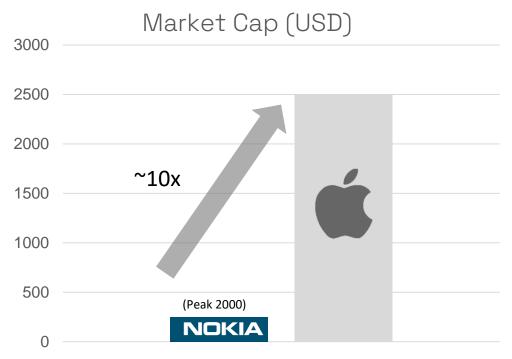
Codasip Custom Compute

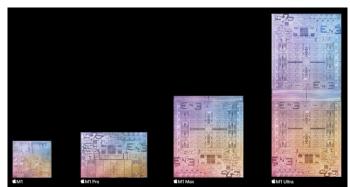


Custom Compute is not new...

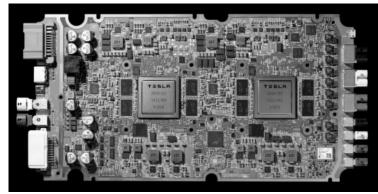
it is highly rewarded today











Custom Compute + benefits of a custom SoC

→ Our fundamental beliefs



RISC-V will gain share

HW & SW collaboration

Co-optimization Custom Compute

OEMs doing more chips



→ But there is a talent challenge



Many processor architects

Many processor architectures

30 years ago

15 years ago



Now



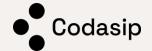
Question:

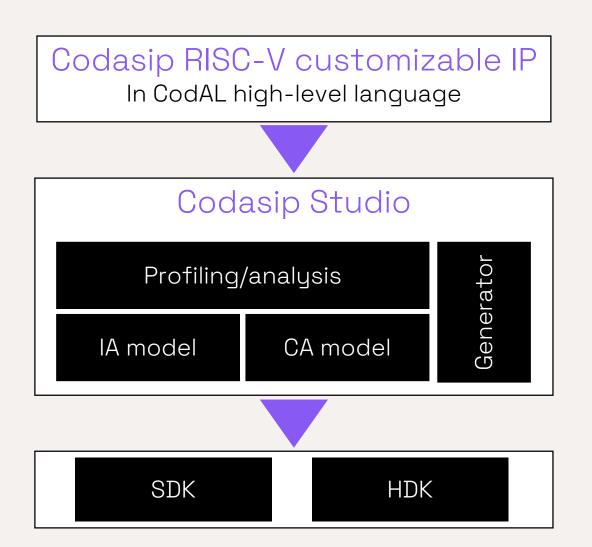
How has the industry coped with complexity and limited design skills in the past 50 years?

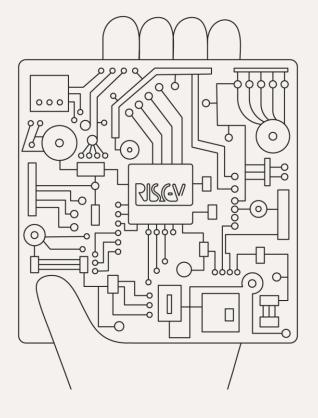
Answer:

Automation → EDA tools

→ Processor design tools







→ Safety and security driving RISC-V forward

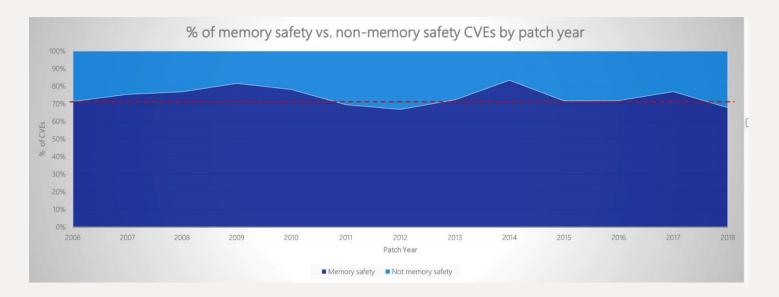




A combined approach to create dependable products for all markets

→ A fundamental security problem











What if you could... customize a security processor based on a starting production core?

...and be protected.

→ Coming soon



• Unique implementati

CENSORED BY CODASIP MARKETING

Come on Brett, you know you can't show this yet 🗟

(seriously, these commercial guys...)

protection

→ Innovation through customization





No more "free improvements" with end of Moore's law



Need to optimize processing to the application

→ Custom Compute



IP and tools to support a hardware / software co-optimization methodology

Architect your ambition



Zdenek Prikryl, CTO

RISC-V as an enabler of heterogeneous compute

Demo theatre - Wednesday 10.55

Tariq Kurd, Lead IP Architect

RISC-V code-size reduction with Zc extensions and dictionary compression custom instruction

Technical talk - Thursday 15:00

Come by our booth for a demo!