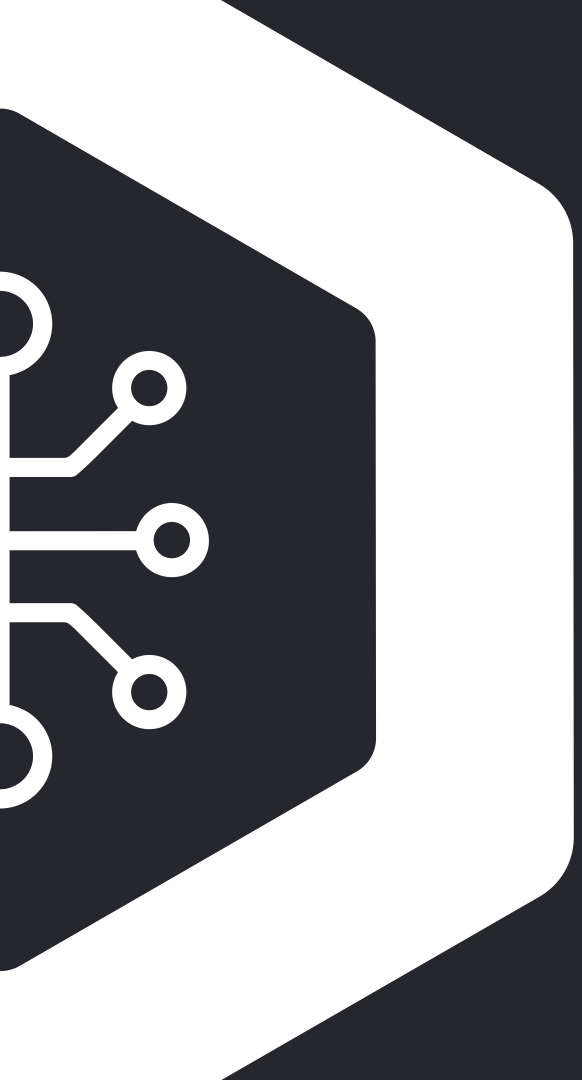

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RISC-V and Antmicro's Visual System Designer: Everything Everywhere all at Once

RISC-V Summit Europe, Barcelona, 2023-06-06

Michael Gielda, mgielda@antmicro.com

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RISC-V and Antmicro's Visual System Designer: Everything Everywhere all at Once

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RISC-V - options, options everywhere

open source hardware

RISC-V

RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once

Fragmentation? More like augmentation

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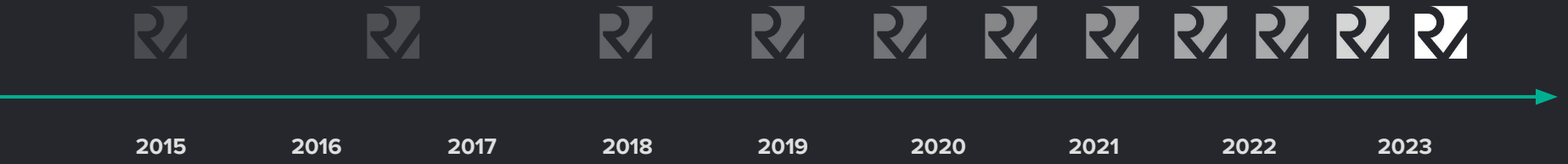
Helping customers adopt RISC-V since 2015



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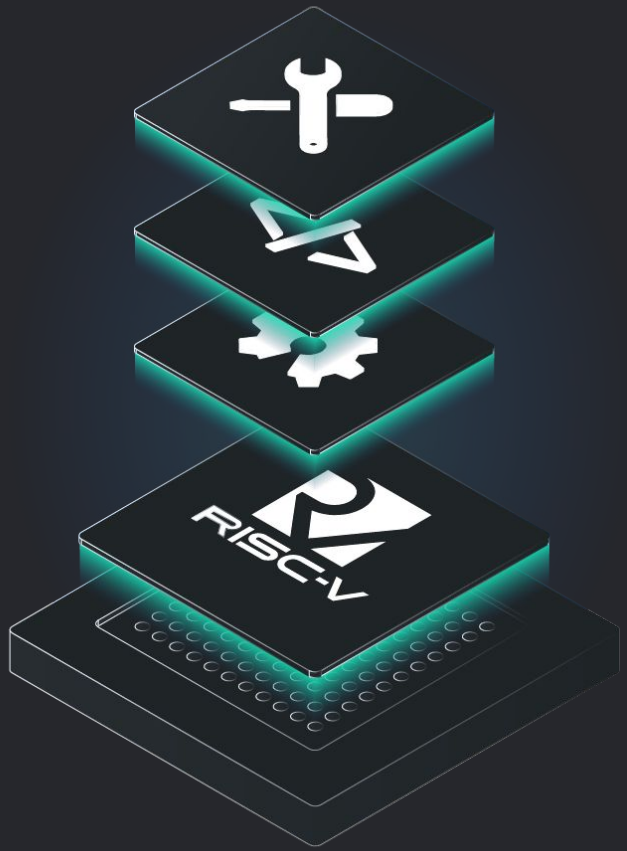

Crossing all levels of the tech stack, enabling vertical integration

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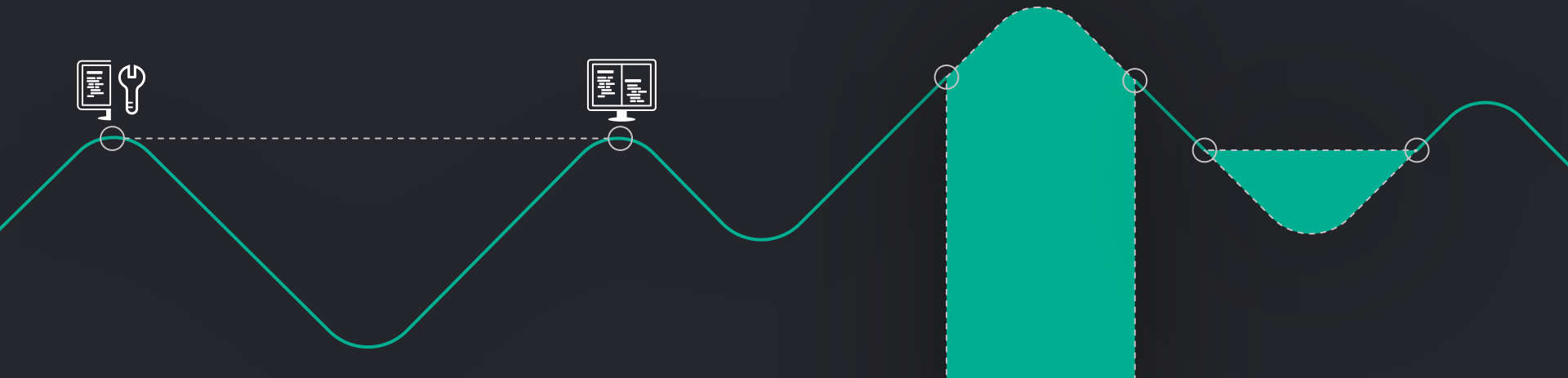
Always improving the open source landscape, connecting, documenting, filling the blanks



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RENODE™

common denominator, making all hardware virtual

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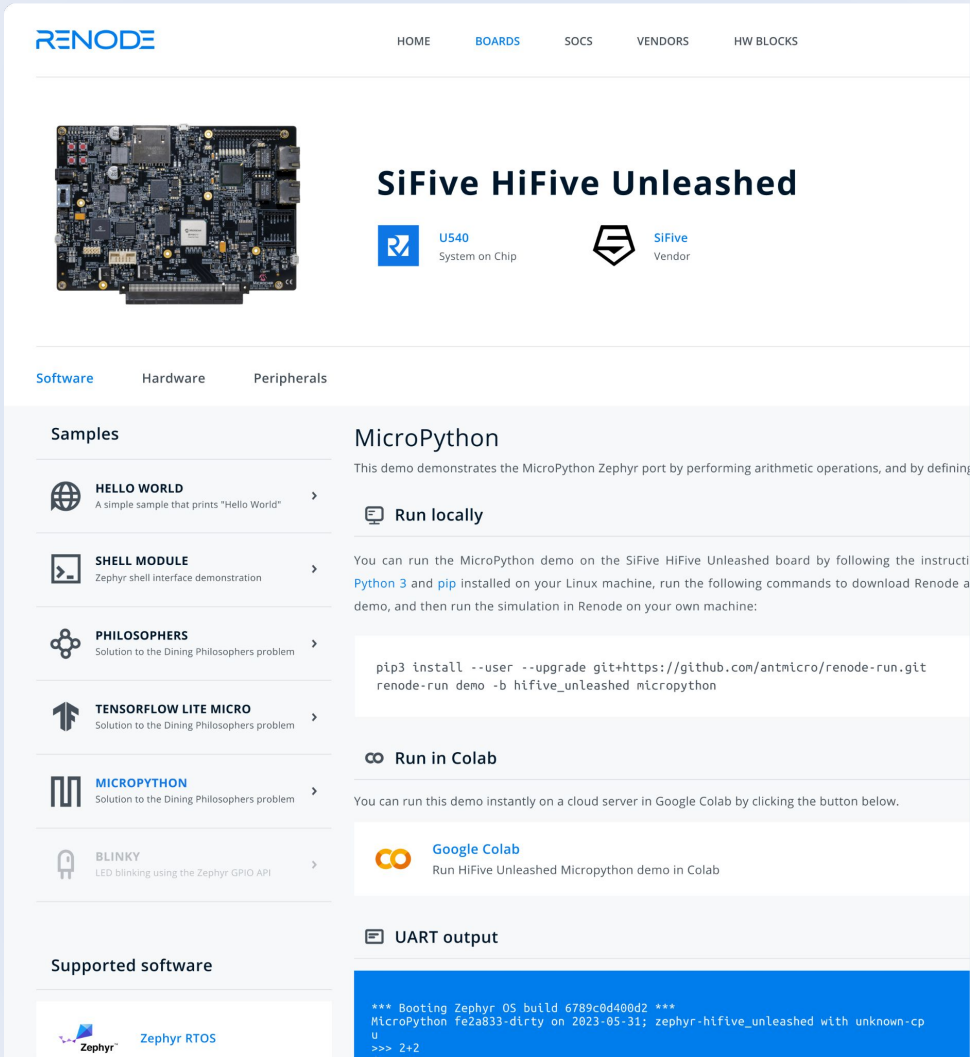
Zephyr™ U-Boot TensorFlow

Using SW data and structure to test software at scale

Search...

BOARD NAME	HELLO WORLD	PHILOSOPHERS	SHELL MODULE	TENSORFLOW LITE MICRO	MICROPYTHON	BLINKY
	273 PASSED	268 PASSED	260 PASSED	265 PASSED	249 PASSED	102 PASSED
LiteX SoC with VexRiscV softcore CPU	PASSED	PASSED	PASSED	PASSED	NOT BUILT	NOT BUILT
M5Stack STAMP-C3	BUILT	BUILT	BUILT	BUILT	BUILT	NOT BUILT
Microchip M2GL025 with MiV target	PASSED	PASSED	GENERATED	NOT BUILT	GENERATED	NOT BUILT
Microchip PolarFire ICICLE kit	PASSED	PASSED	PASSED	PASSED	GENERATED	GENERATED
NEORV32 Processor (SoC)	BUILT	BUILT	BUILT	NOT BUILT	NOT BUILT	BUILT
OpenTitan Earl Grey	PASSED	PASSED	PASSED	PASSED	NOT BUILT	NOT BUILT
RV32M1-VEGA (RI5CY)	BUILT	BUILT	BUILT	BUILT	BUILT	BUILT
RV32M1-VEGA (ZERO-RISCY)	BUILT	BUILT	BUILT	BUILT	BUILT	BUILT
SiFive HiFive Unleashed	PASSED	PASSED	PASSED	PASSED	PASSED	NOT BUILT
SiFive HiFive Unmatched	PASSED	PASSED	PASSED	PASSED	PASSED	NOT BUILT
SiFive HiFive1	PASSED	PASSED	PASSED	PASSED	PASSED	GENERATED
SiFive HiFive1 Rev B	PASSED	PASSED	PASSED	PASSED	PASSED	GENERATED

Take this to the next level: Renodepedia



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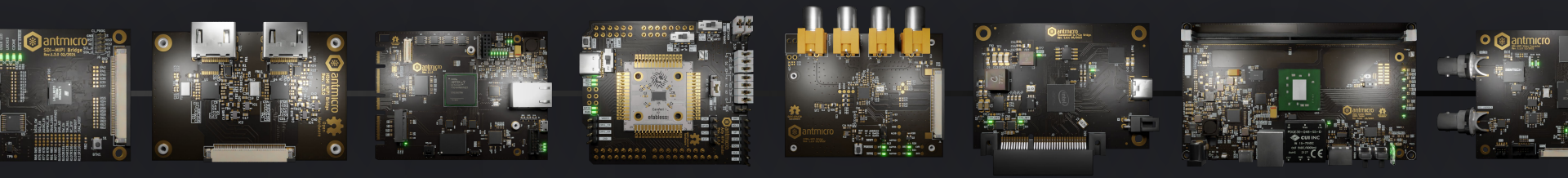
But software needs hardware...



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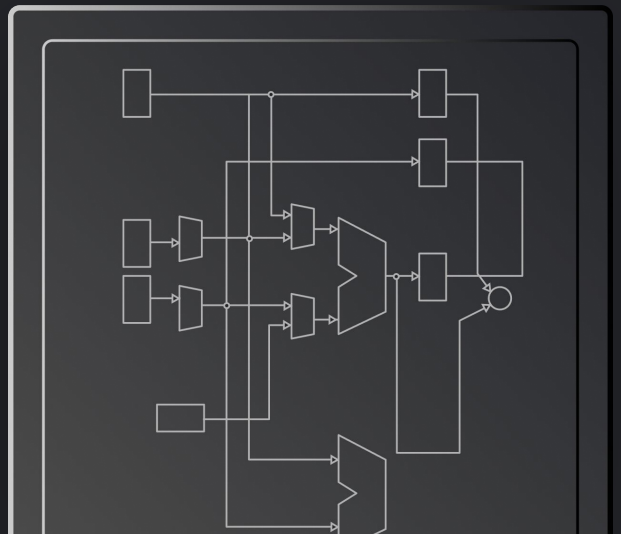
... and hardware is all about structure



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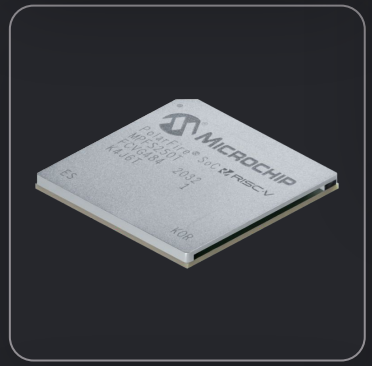
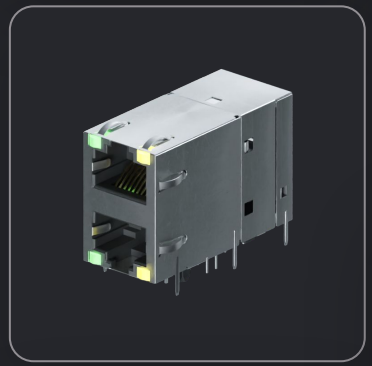
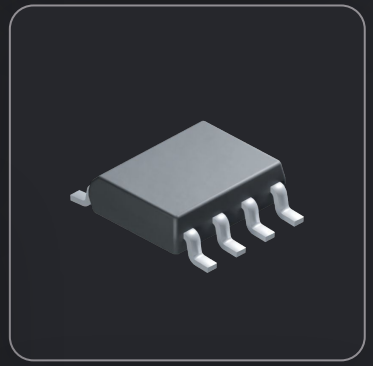
From the structure, the Open Hardware Portal was born

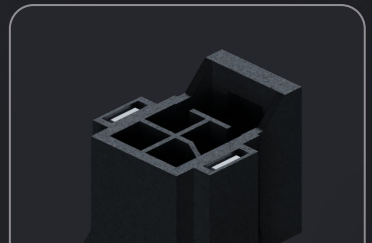
RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once

Open source components database with KiCad footprints and Blender models



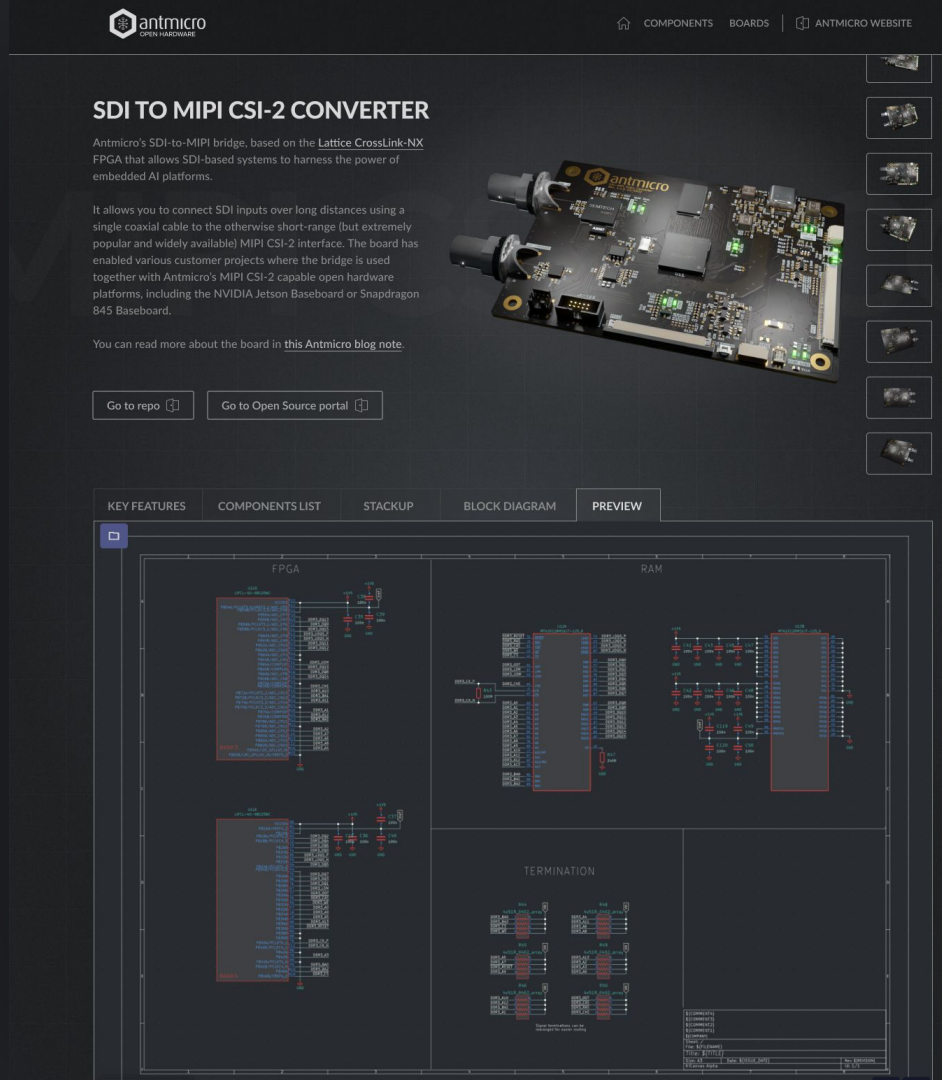






RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once

Interactive schematics viewer



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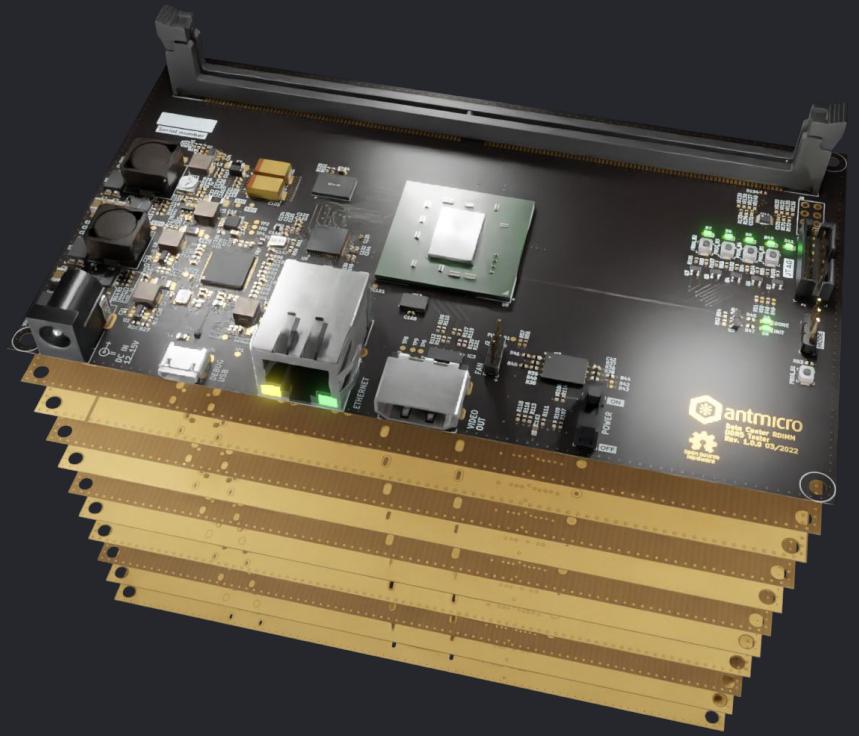
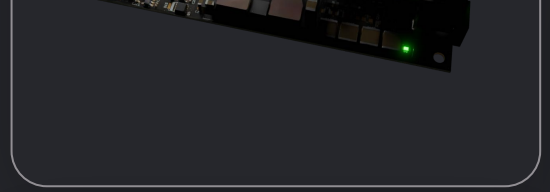
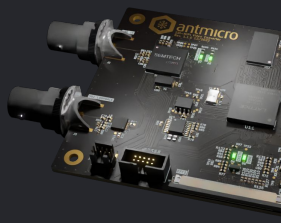
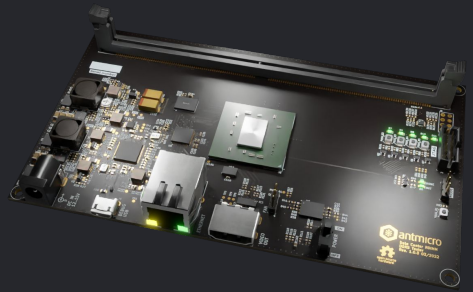


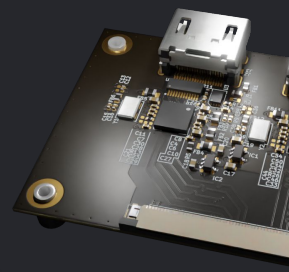
Stackup visualization

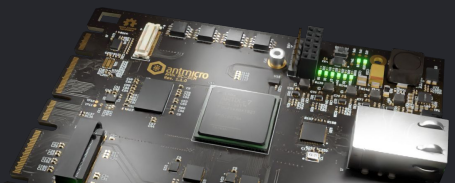
Growing open HW portfolio with photorealistic 3D renders











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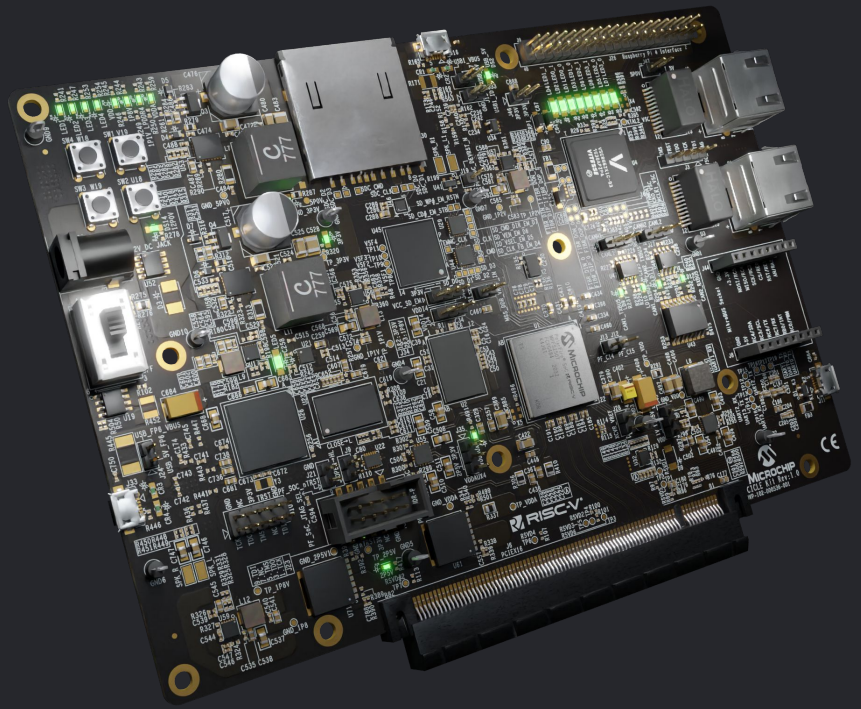

... but our flow can be used to visualize any board

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It's all part of the same landscape

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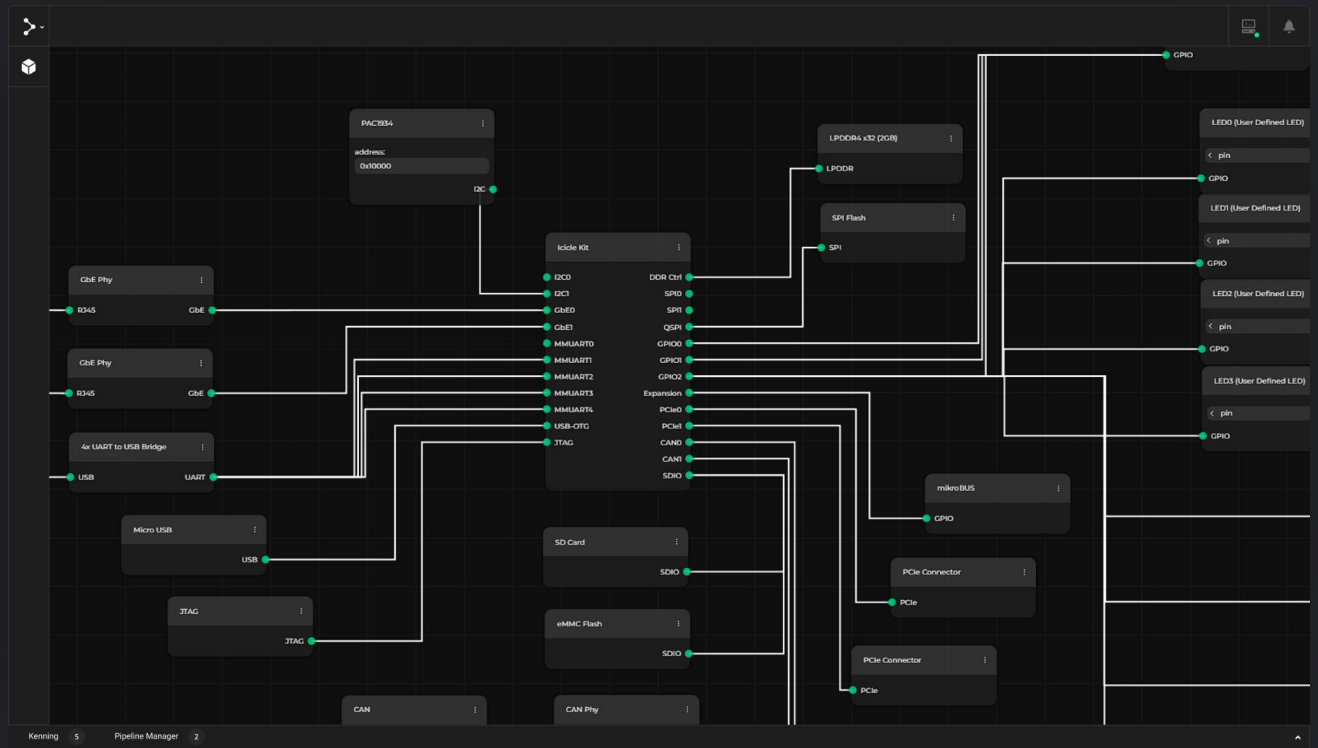
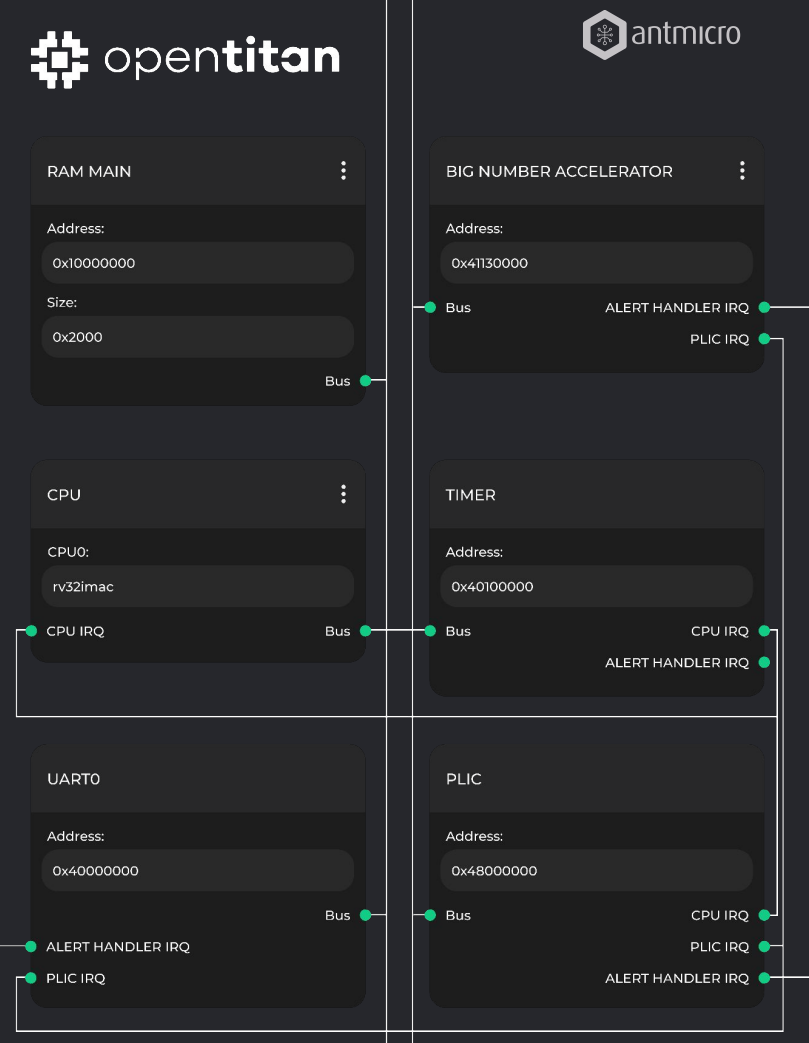
Introducing the Hardware Designer



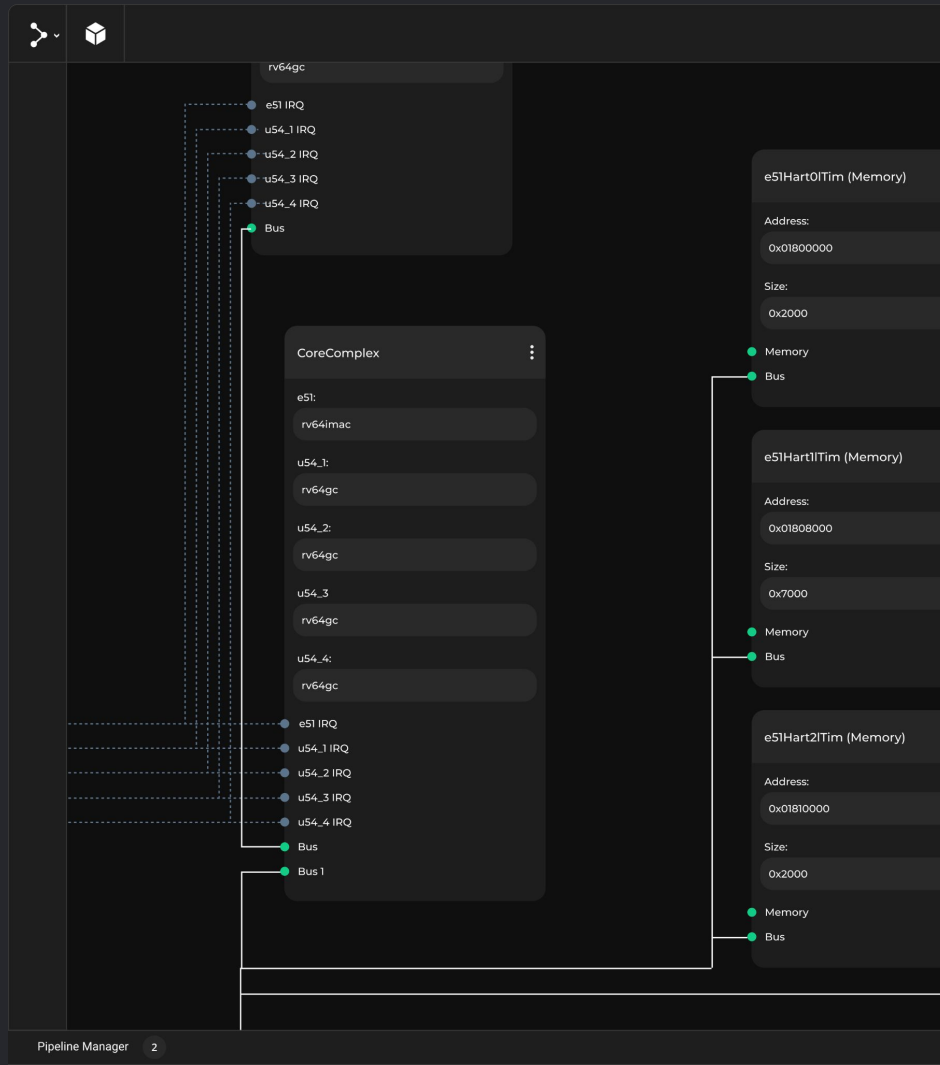
RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once

Unleash the freedom provided by RISC-V



RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once

Build SoCs from IP blocks



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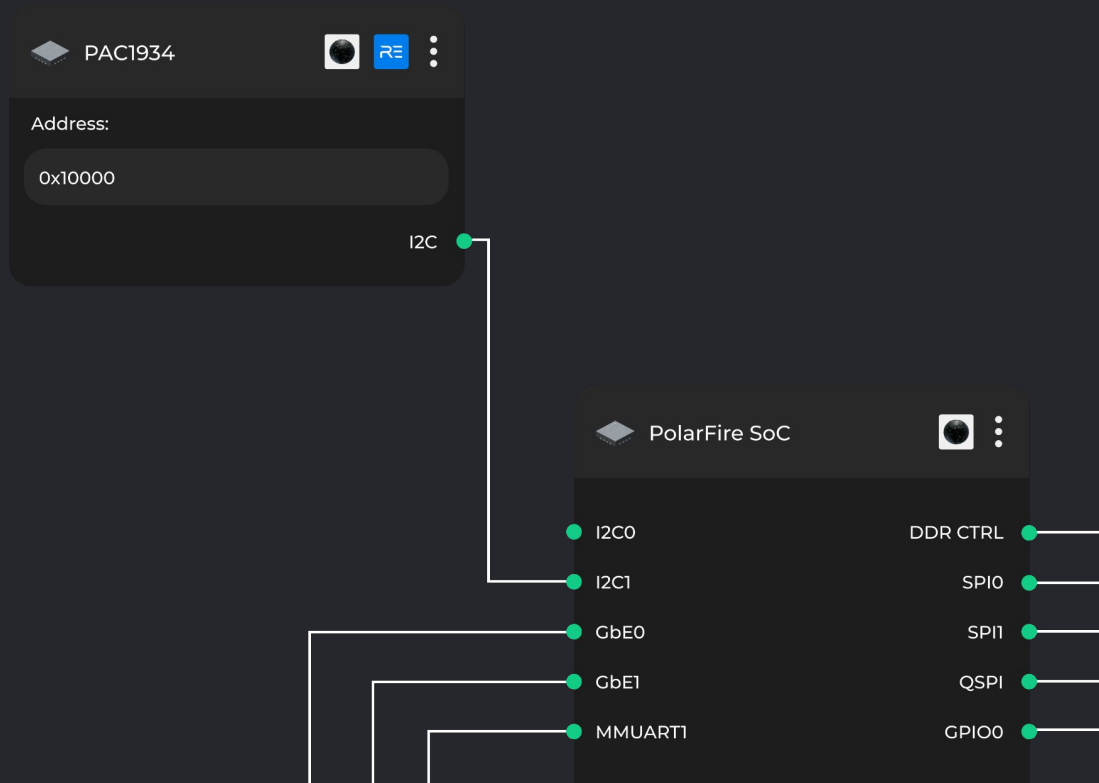
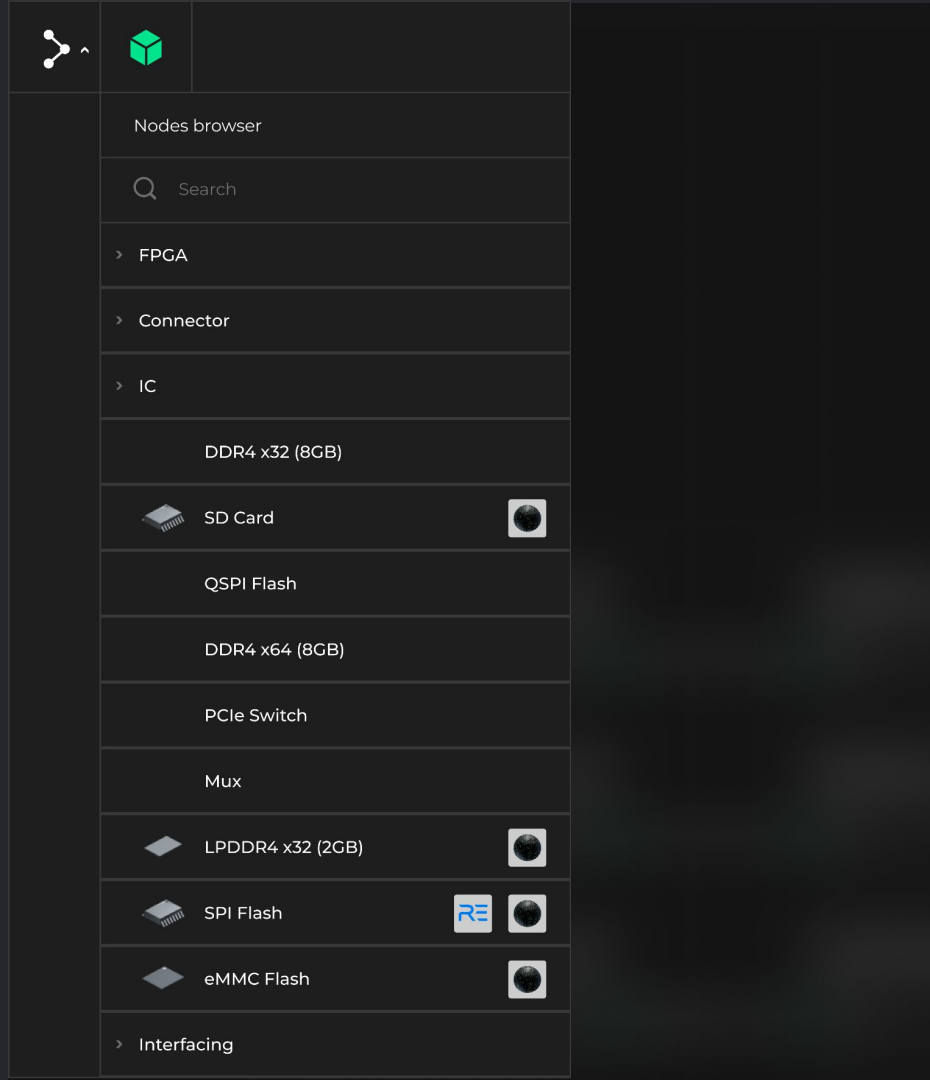
Expand to entire boards



Look up components in Renodepedia and our Open Hardware Portal



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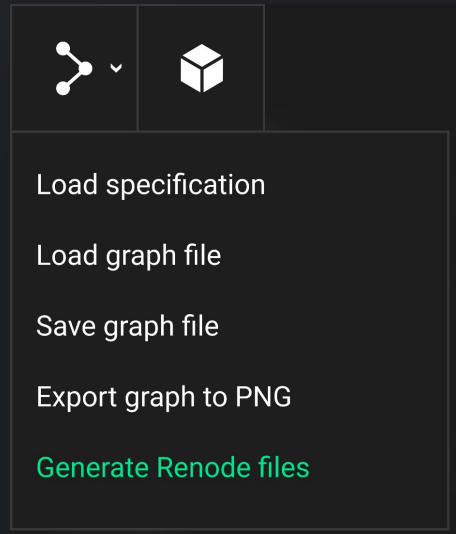
Generate Renode simulation files



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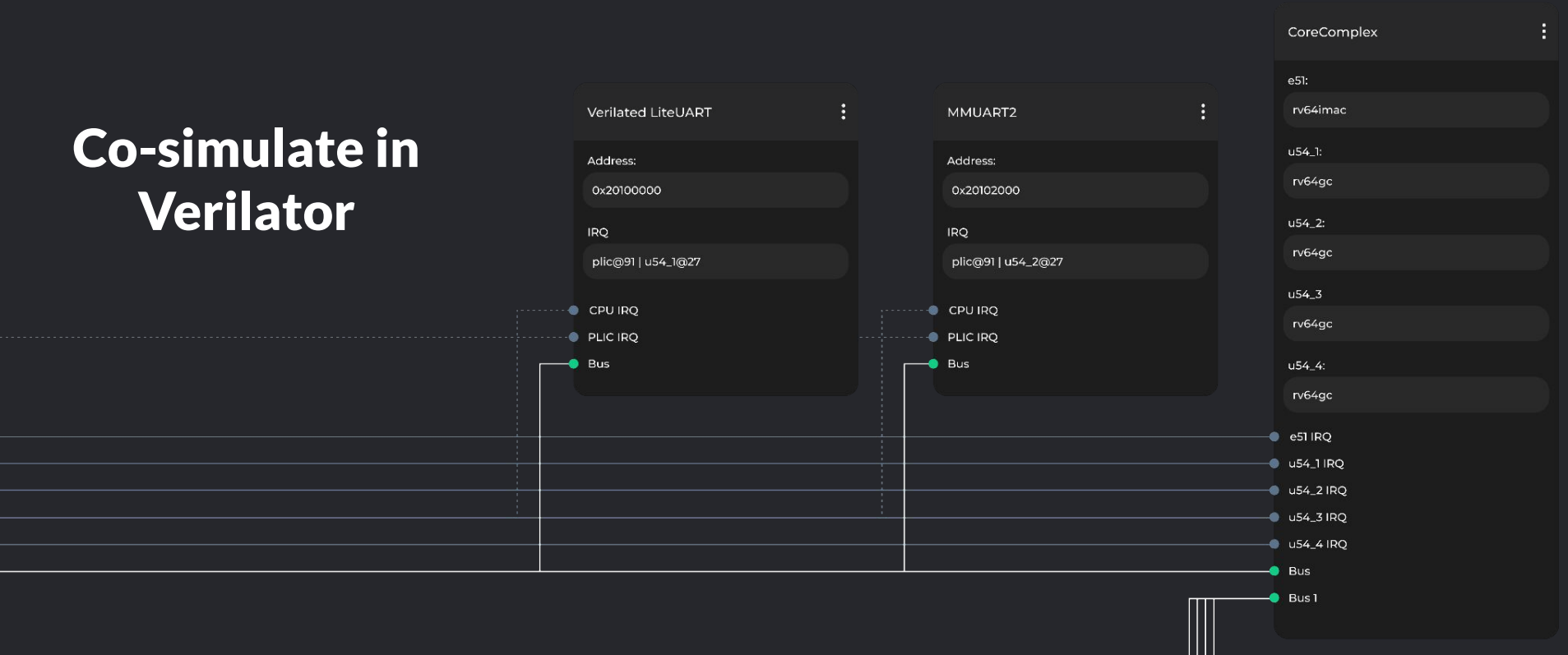
Co-simulate in Verilator



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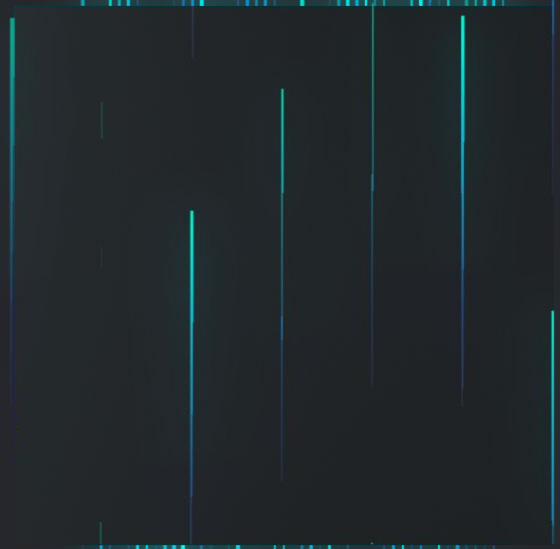
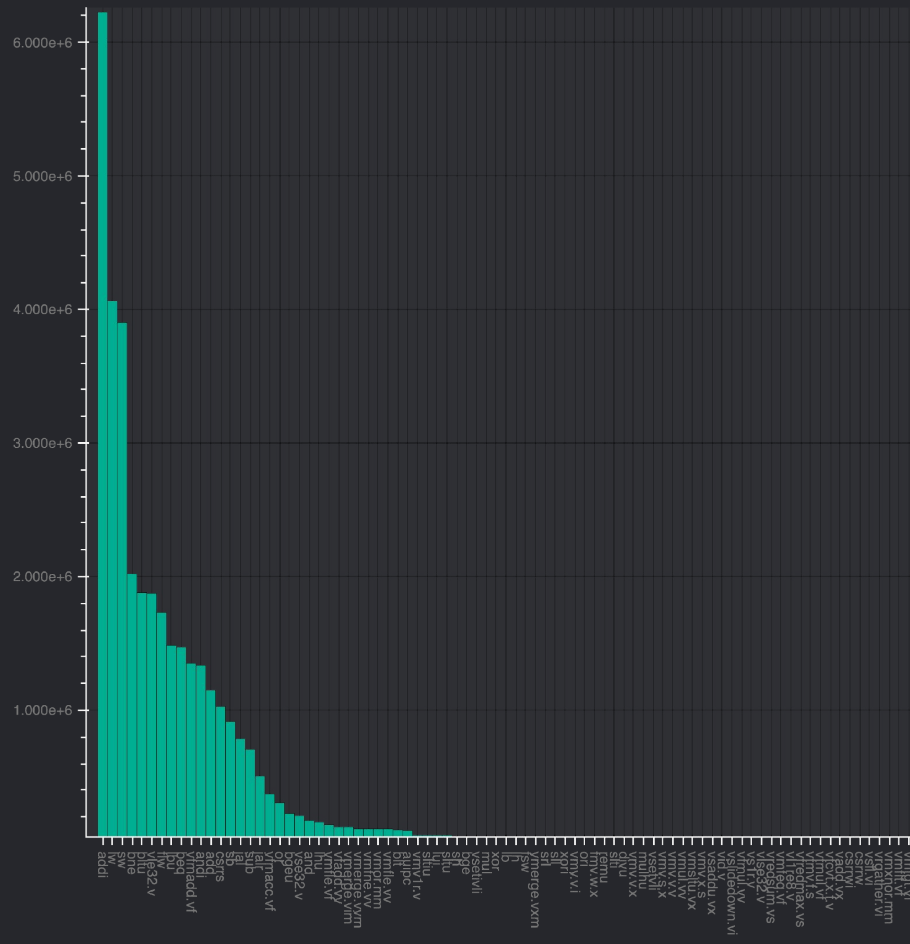
Co-development of ML, vector, custom instructions



Gather metrics from your implementation



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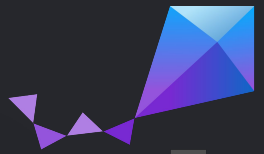
Verify your implementation with RISC-V DV

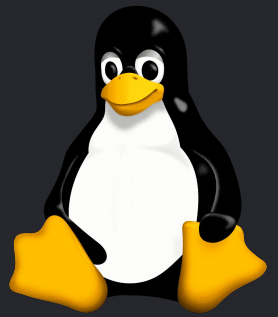
```
0x8000bfa8:   01010113  addi sp, sp, 16
0x8000bfac:   00008067  ret
0x8000c0b8:   fff00793  li a5, -1
0x8000c0bc:   00f50e63  beq a0, a5, 28
0x8000c0c0:   00a4dc63  bge s1, a0, 24
0x8000c0d8:   00847413  andi s0, s0, 8
0x8000c0dc:   30042473  csrrs s0, mstatus, s0
0x8000c0e0:   01c12083  lw ra, 28(sp)
0x8000c0e4:   01812403  lw s0, 24(sp)
0x8000c0e8:   01412483  lw s1, 20(sp)
0x8000c0ec:   02010113  addi sp, sp, 32
0x8000c0f0:   00008067  ret
0x8000cac4:   de1f50ef  jal -41504
0x800028a4:   00800793  li a5, 8
0x800028a8:   3007a7f3  csrrs a5, mstatus, a5
0x800028ac:   10500073  wfi
0x80000010:   fb010113  addi sp, sp, -80
```

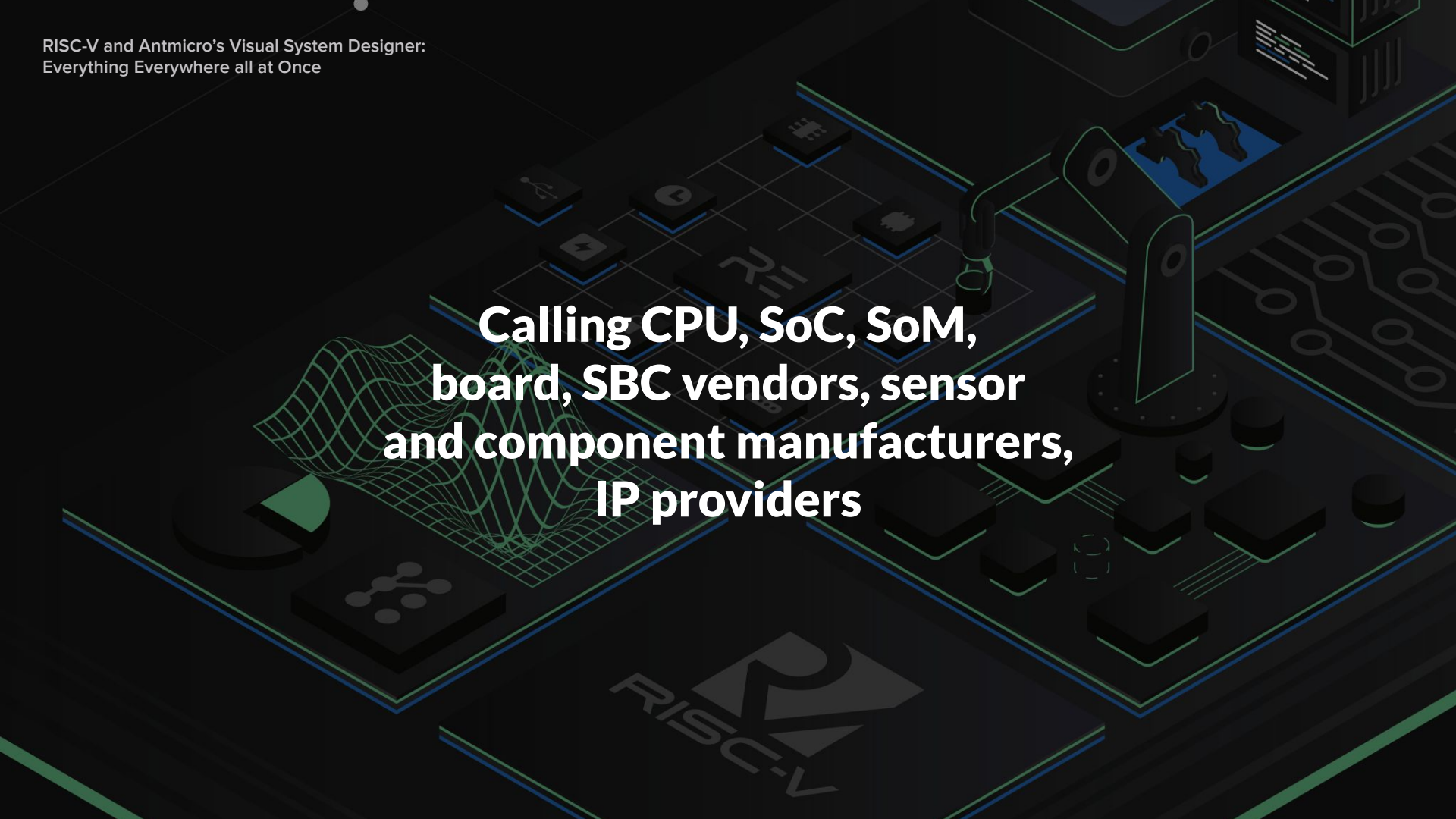
Generate Zephyr firmware, U-Boot, Linux kernels



Zephyr™

U-Boot




Calling CPU, SoC, SoM,
board, SBC vendors, sensor
and component manufacturers,
IP providers

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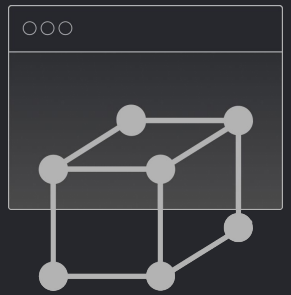
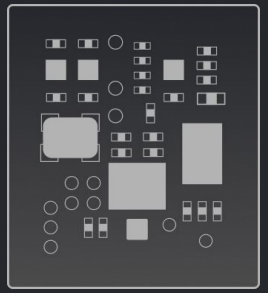
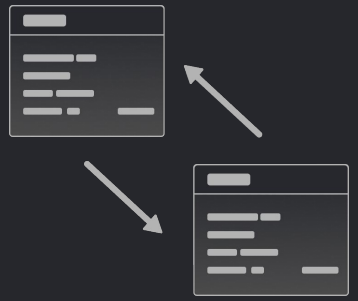
Calling end users, product development companies



add simulation models



build boards



port software

build/integrate core and un-core IP

RISC-V

RISC-V Summit Europe

Meet us at Booth 1