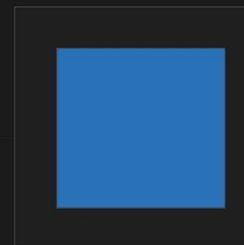
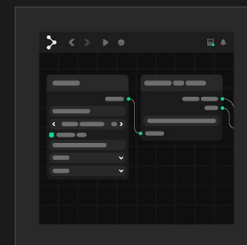
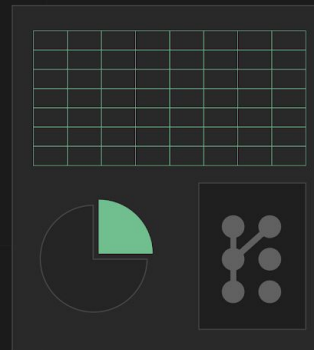
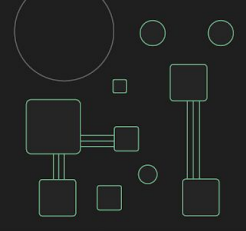
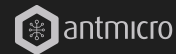


RISC-V and Antmicro's Visual System Designer: Everything Everywhere all at Once

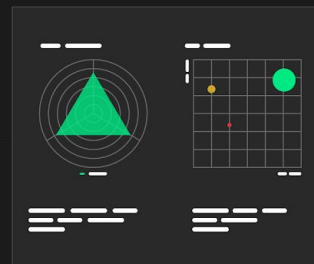
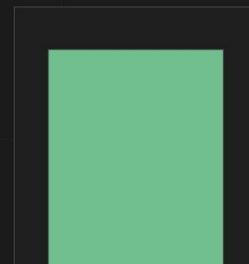
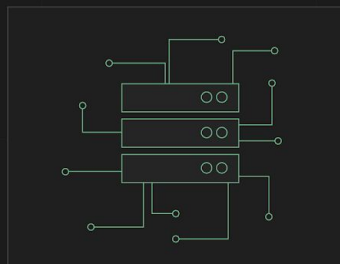
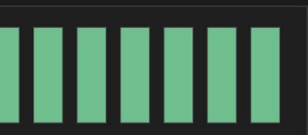
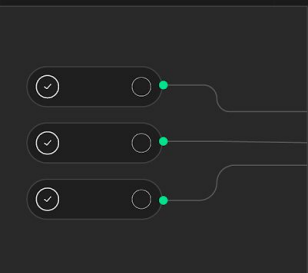
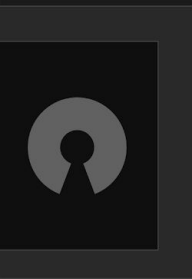
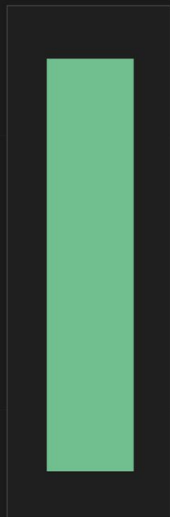
RISC-V Summit Europe, Barcelona, 2023-06-06

Michael Gielda, mgielda@antmicro.com

RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once



RISC-V - options, options everywhere



RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once

Fragmentation? More like augmentation



Helping customers adopt RISC-V since 2015



2015

2016

2017

2018

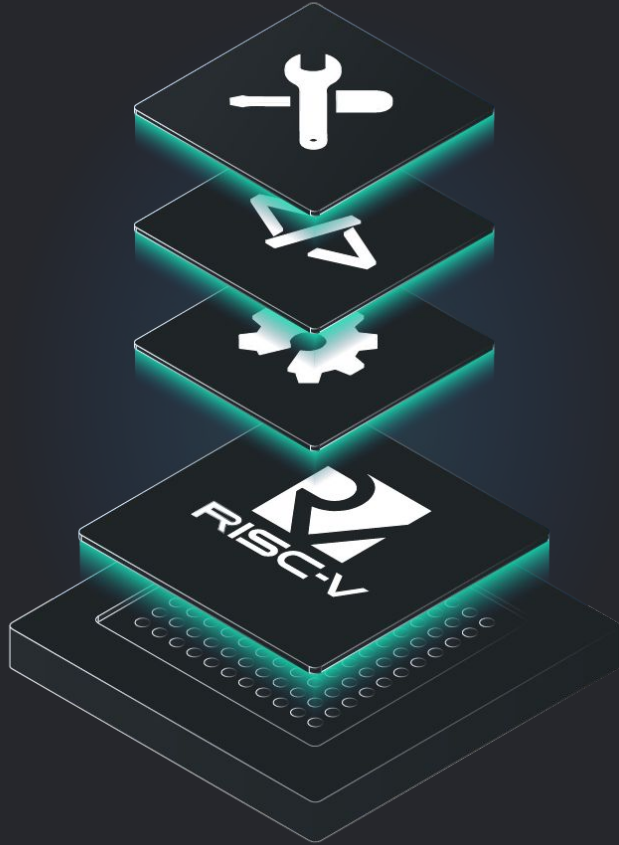
2019

2020

2021

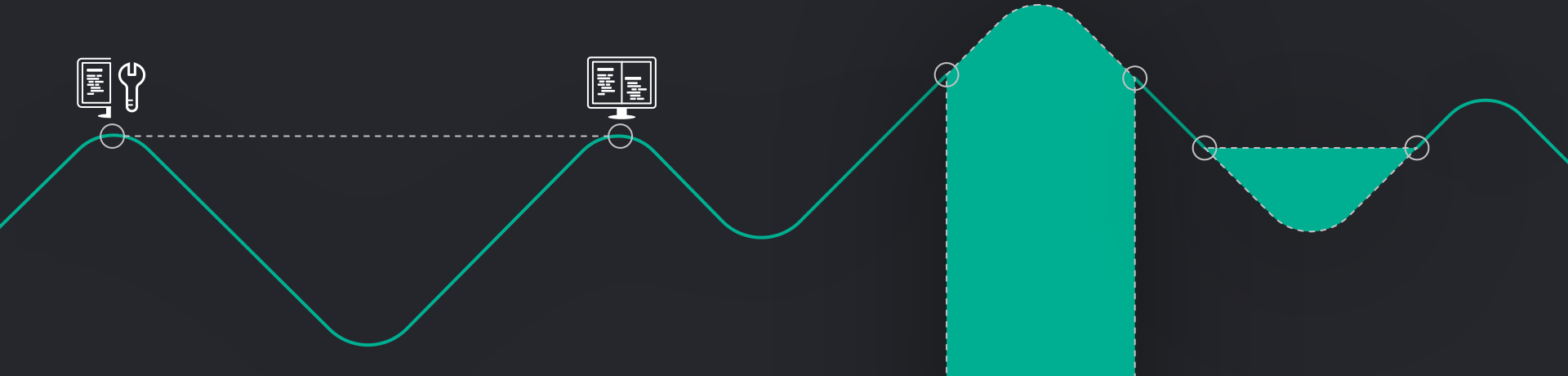
2022

2023



**Crossing all levels of the tech stack,
enabling vertical integration**

**Always improving the open source landscape,
connecting, documenting, filling the blanks**



RENODE™

common denominator, making all hardware virtual

Take this to the next level: Renodepedia



SiFive HiFive Unleashed



Software Hardware Peripherals

Samples


 **HELLO WORLD**
A simple sample that prints "Hello World" >

 **SHELL MODULE**
Zephyr shell interface demonstration >

 **PHILOSOPHERS**
Solution to the Dining Philosophers problem >

 **TENSORFLOW LITE MICRO**
Solution to the Dining Philosophers problem >

 **MICROPYTHON**
Solution to the Dining Philosophers problem >


 **BLINKY**
LED blinking using the Zephyr GPIO API >

Supported software

 **Zephyr RTOS**

MicroPython

This demo demonstrates the MicroPython Zephyr port by performing arithmetic operations, and by defining

 **Run locally**

You can run the MicroPython demo on the SiFive HiFive Unleashed board by following the instructions in the [MicroPython demo](#). To run the demo, you need [Python 3](#) and [pip](#) installed on your Linux machine, run the following commands to download Renode and the demo, and then run the simulation in Renode on your own machine:

```
pip3 install --user --upgrade git+https://github.com/antmicro/renode-run.git
renode-run demo -b hifive_unleashed micropython
```

 **Run in Colab**

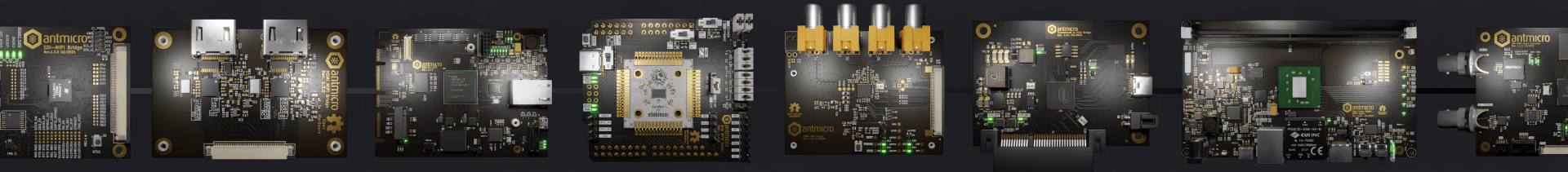
You can run this demo instantly on a cloud server in Google Colab by clicking the button below.

 **Google Colab**
Run HiFive Unleashed Micropython demo in Colab

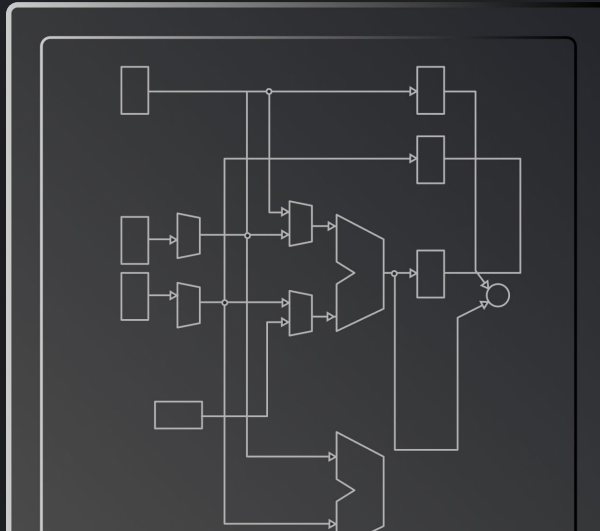
 **UART output**

```
*** Booting Zephyr OS build 6789c0d400d2 ***
MicroPython Fe2a833-dirty on 2023-05-31; zephyr-hifive_unleashed with unknown-cp
u
>>> 2+2
```

But software needs hardware...



... and hardware is all about structure

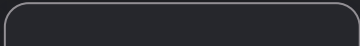
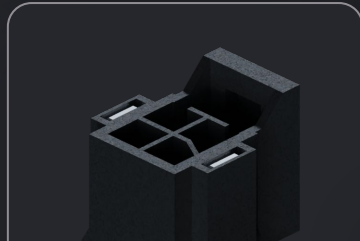
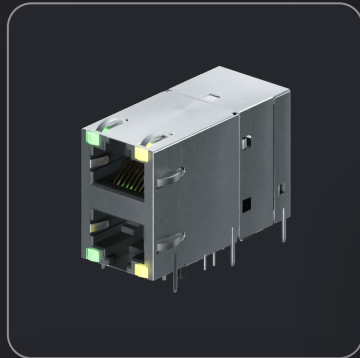
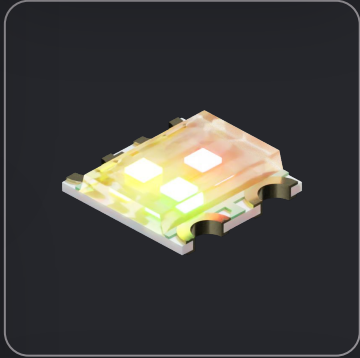
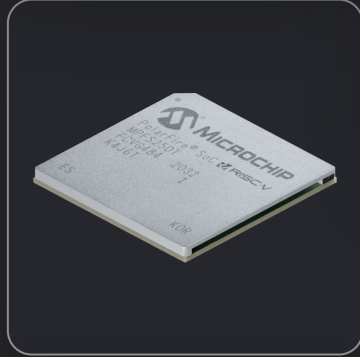
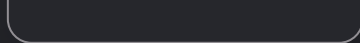


From the structure, the Open Hardware Portal was born



RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once

Open source components database with KiCad footprints and Blender models



SDI TO MIPI CSI-2 CONVERTER

Antmicro's SDI-to-MIPI bridge, based on the Lattice CrossLink-NX FPGA that allows SDI-based systems to harness the power of embedded AI platforms.

It allows you to connect SDI inputs over long distances using a single coaxial cable to the otherwise short-range (but extremely popular and widely available) MIPI CSI-2 interface. The board has enabled various customer projects where the bridge is used together with Antmicro's MIPI CSI-2 capable open hardware platforms, including the NVIDIA Jetson Baseboard or Snapdragon 845 Baseboard.

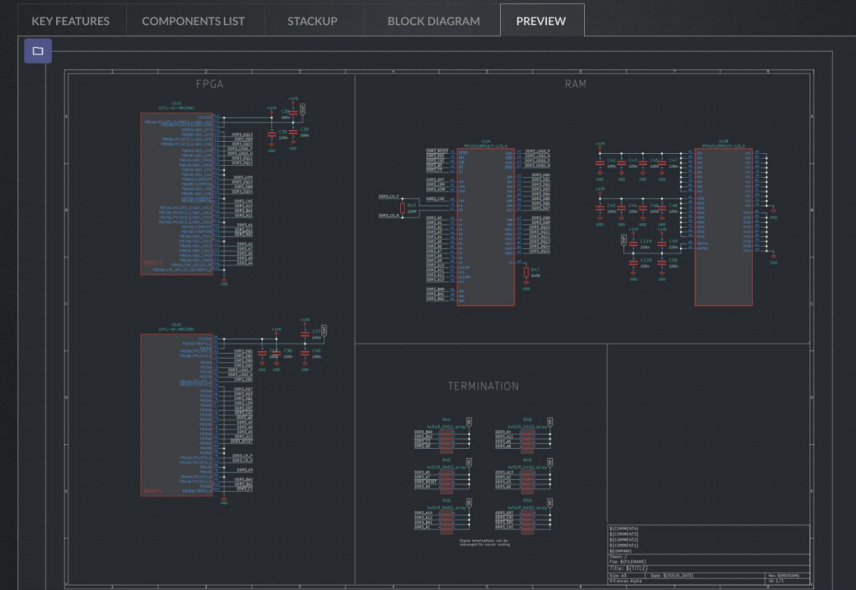
You can read more about the board in [this Antmicro blog note](#).

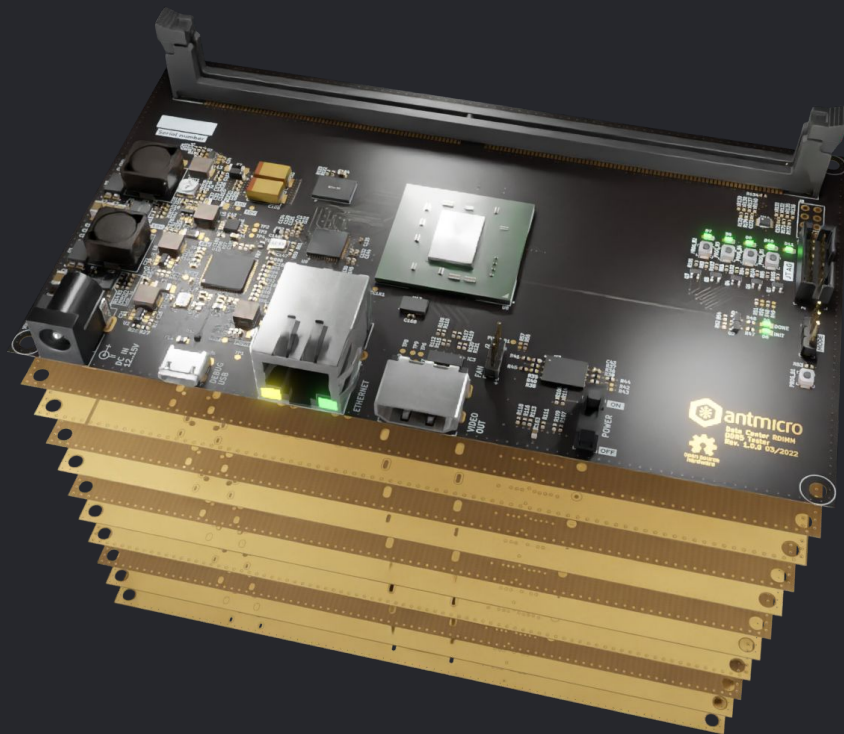
[Go to repo](#)

[Go to Open Source portal](#)



Interactive schematics viewer

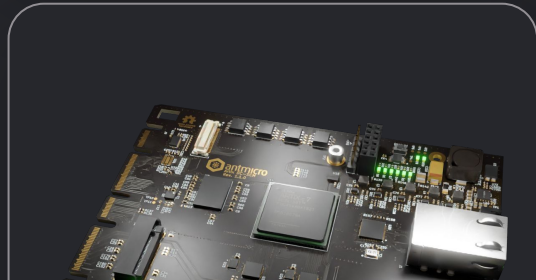
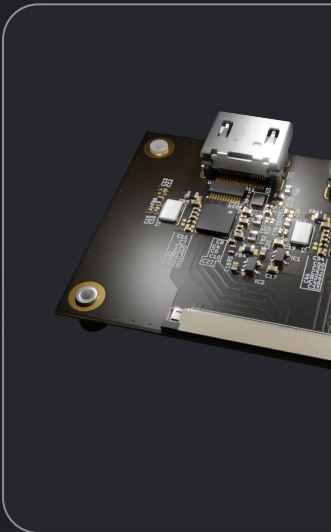
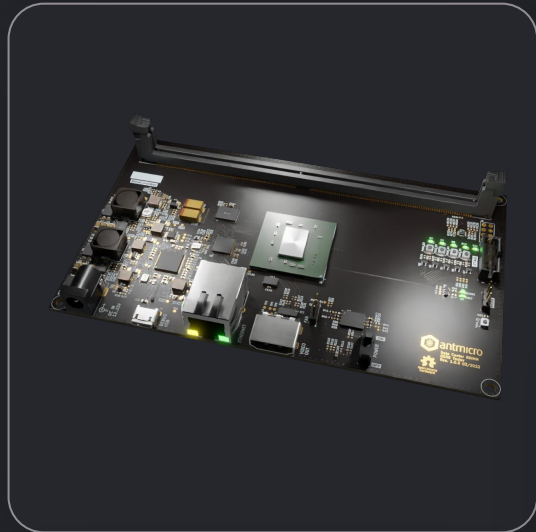
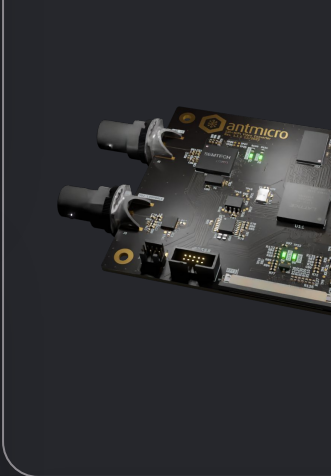
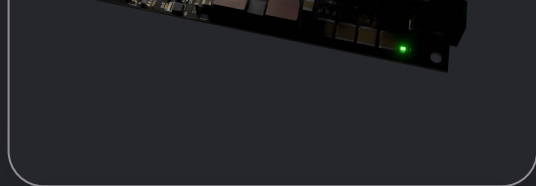


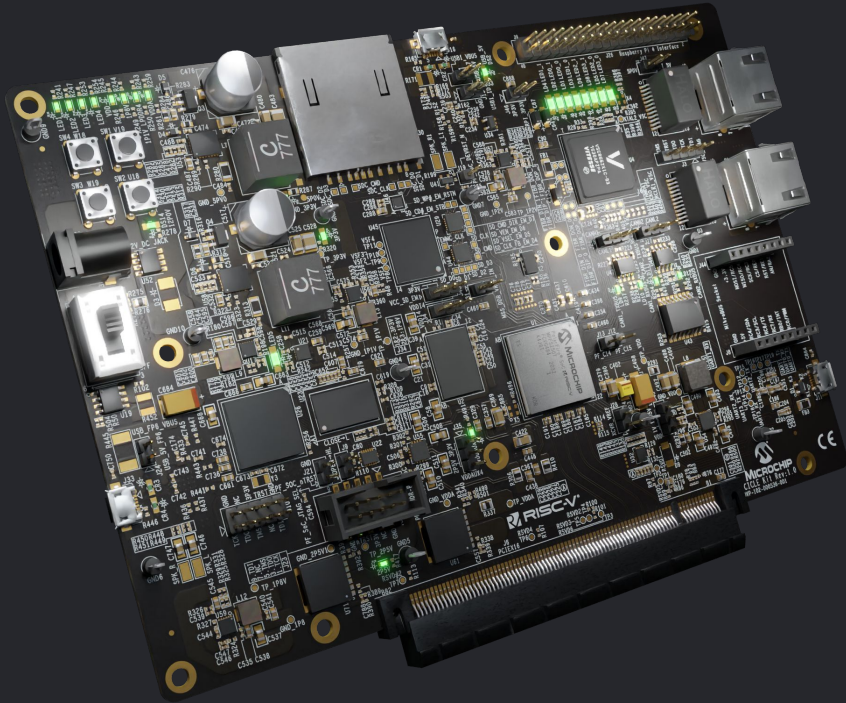


Stackup visualization

RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once

Growing open HW portfolio with photorealistic 3D renders



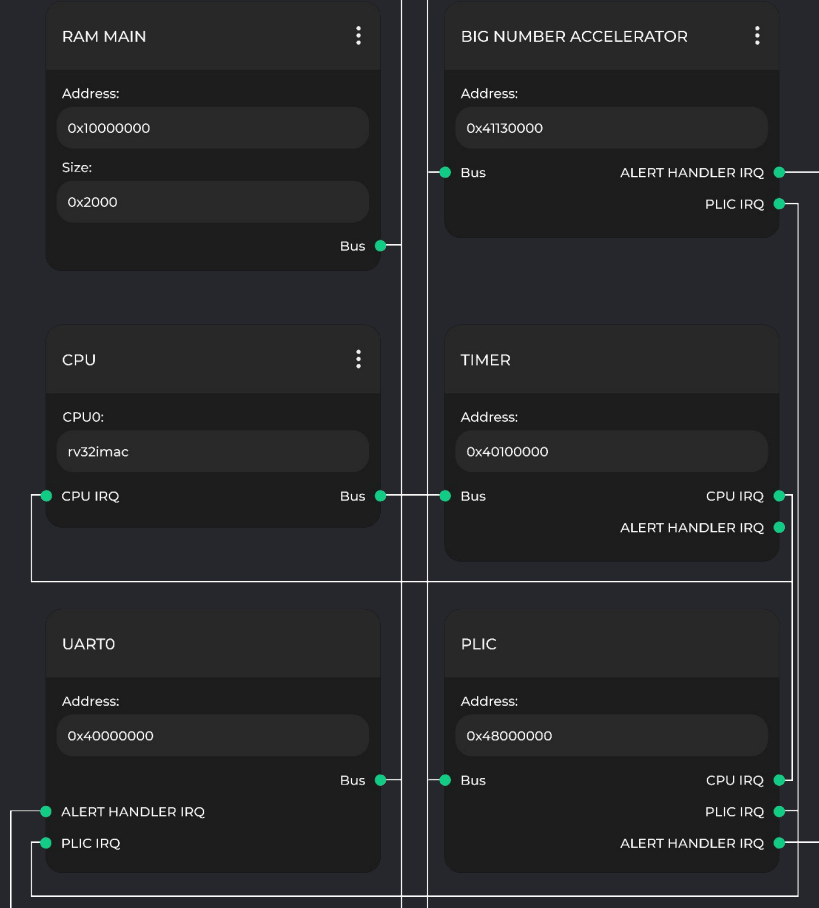
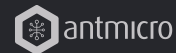


**... but our flow can be
used to visualize any
board**

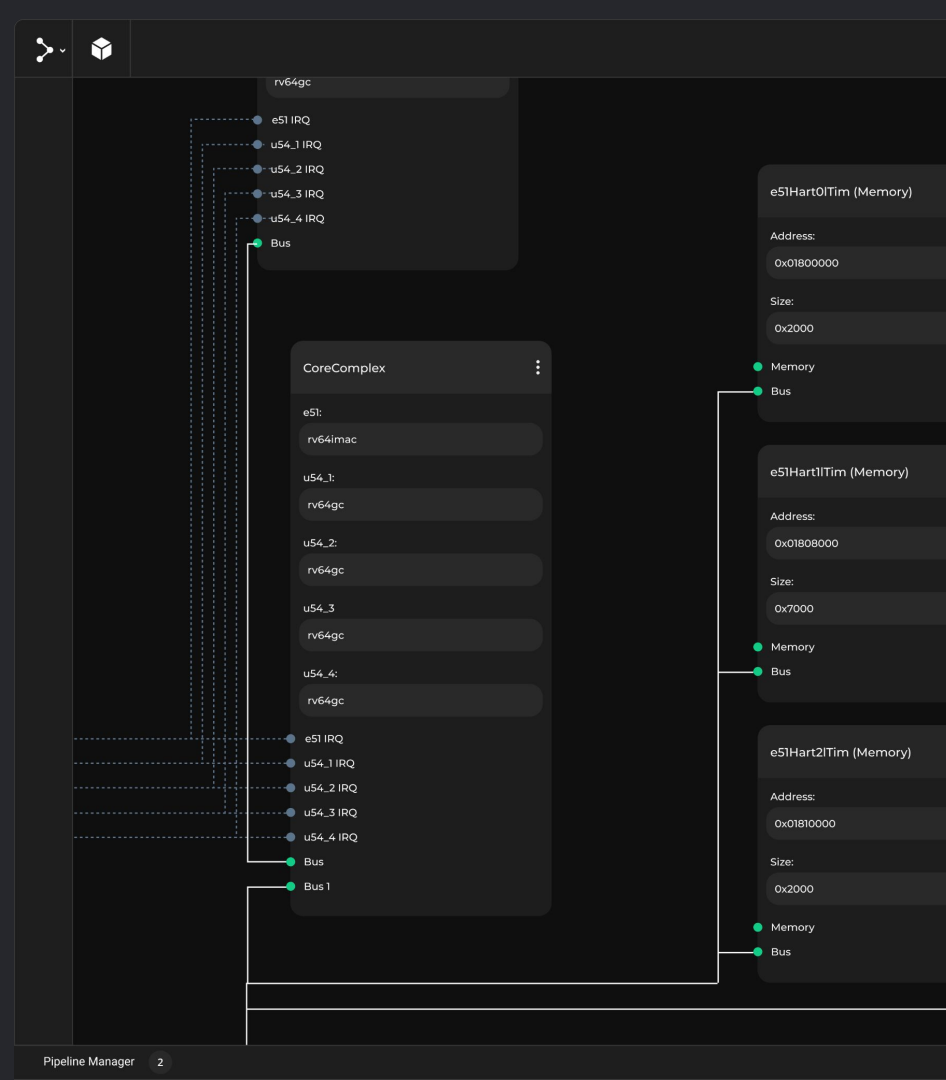
**It's all part of the
same landscape**



Unleash the freedom provided by RISC-V



Build SoCs from IP blocks

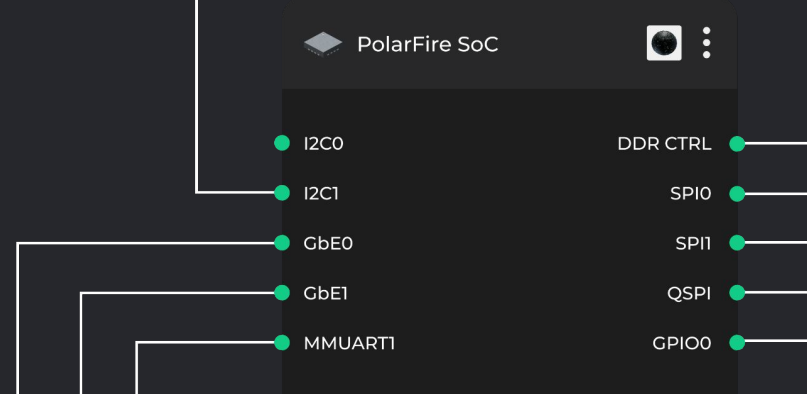


Expand to entire boards

PAC1934

Address:
0x10000

I2C



Look up components in Renodepedia and our Open Hardware Portal

Nodes browser



Search

> FPGA

> Connector

> IC

DDR4 x32 (8GB)



 SD Card 




QSPI Flash



DDR4 x64 (8GB)

PCIe Switch

Mux

 LPDDR4 x32 (2GB) 

 SPI Flash  

 eMMC Flash 

> Interfacing

Generate Renode simulation files



Load specification

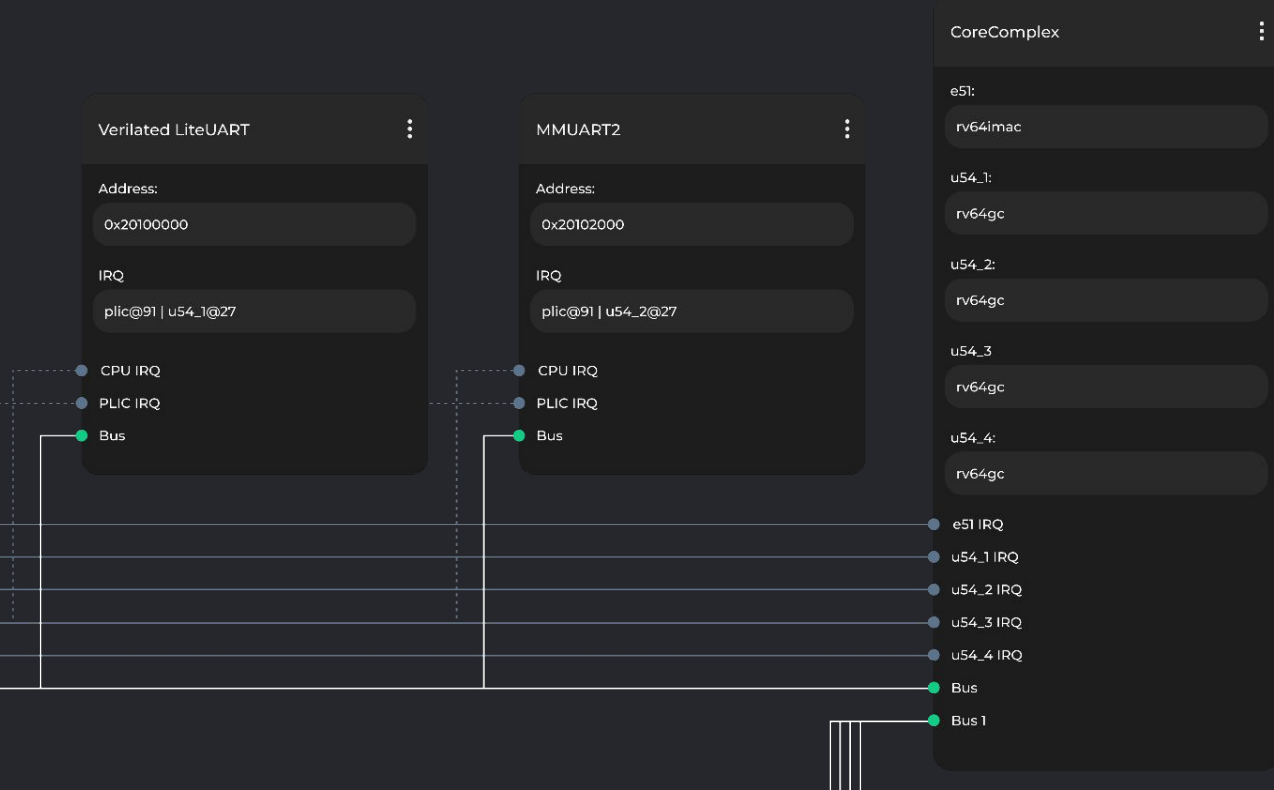
Load graph file

Save graph file

Export graph to PNG

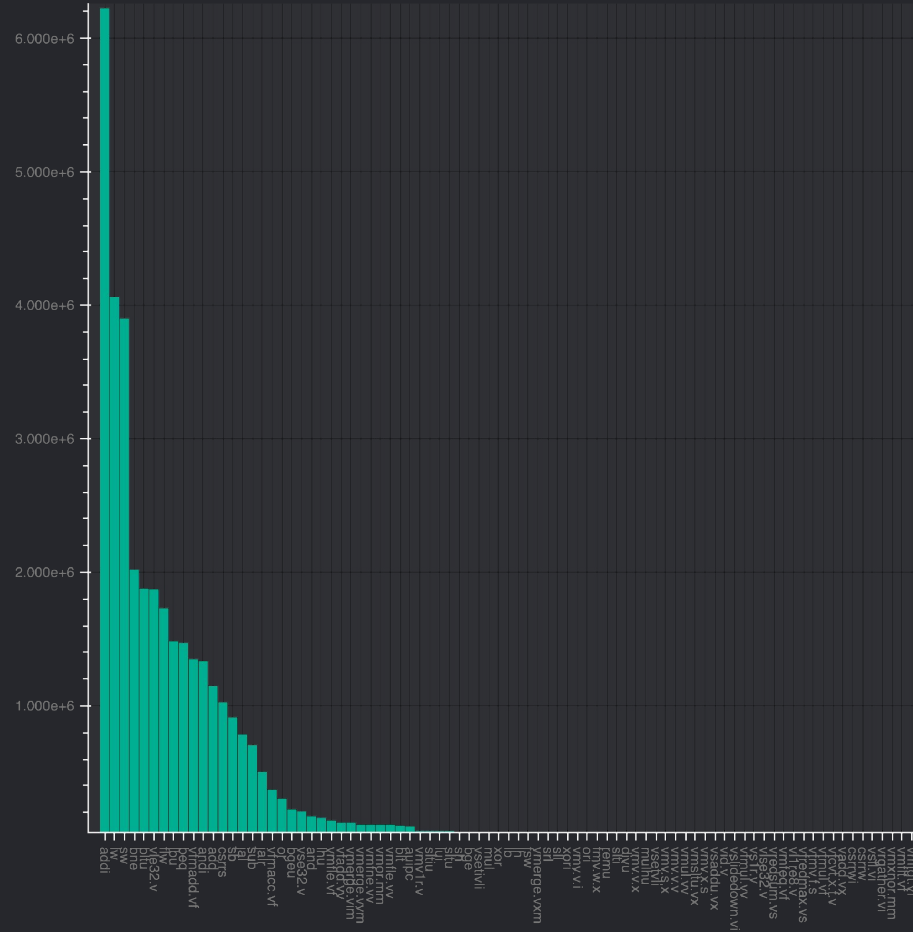
Generate Renode files

Co-simulate in Verilator



Co-development of ML, vector, custom instructions

Gather metrics from your implementation



Verify your implementation with RISC-V DV

```
0x8000bfa8: 01010113 addi sp, sp, 16
0x8000bfac: 00008067 ret
0x8000c0b8: fff00793 li a5, -1
0x8000c0bc: 00f50e63 beq a0, a5, 28
0x8000c0c0: 00a4dc63 bge s1, a0, 24
0x8000c0d8: 00847413 andi s0, s0, 8
0x8000c0dc: 30042473 csrrs s0, mstatus, s0
0x8000c0e0: 01c12083 lw ra, 28(sp)
0x8000c0e4: 01812403 lw s0, 24(sp)
0x8000c0e8: 01412483 lw s1, 20(sp)
0x8000c0ec: 02010113 addi sp, sp, 32
0x8000c0f0: 00008067 ret
0x8000cac4: de1f50ef jal -41504
0x800028a4: 00800793 li a5, 8
0x800028a8: 3007a7f3 csrrs a5, mstatus, a5
0x800028ac: 10500073 wfi
0x80000010: fb010113 addi sp, sp, -80
```

Generate Zephyr firmware, U-Boot, Linux kernels



U-Boot



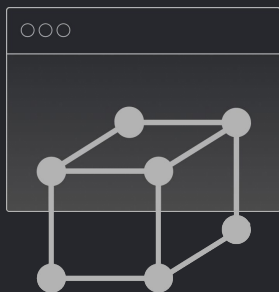
Zephyr™



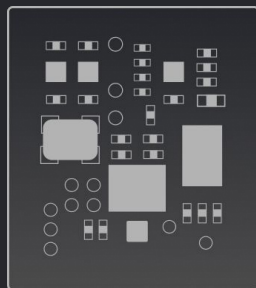
RISC-V and Antmicro's Visual System Designer:
Everything Everywhere all at Once

**Calling CPU, SoC, SoM,
board, SBC vendors, sensor
and component manufacturers,
IP providers**

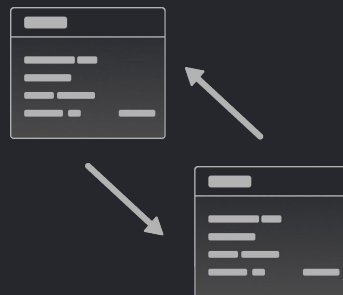
Calling end users, product development companies



**add simulation
models**



build boards



port software



**build/integrate core
and un-core IP**

RISC-V

RISC-V Summit Europe

Meet us at Booth 1

