中国科学院计算技术研究所
INSTITUTE OF COMPUTING TECHNOLOGY, CHINESE ACADEMY OF SCIENCES

BOSC

中国开放指令生态（RISC-V）联盟
China RISC-V Alliance

RISC-V in China:
Embracing the Era of Open-Source Chip

Yungang Bao
BOSC/ICT,CAS
June 7, 2023

RISC-V Summit Europe 2023, 5-9 June 2023, Barcelona, Spain

Outline

- **Part I**: Open-Source Chip Ecosystem (OSCE)
- **Part II**: RISC-V in China
- **Part III**: Progress in Building OSCE

Part I

Open-Source Chip Ecosystem (OSCE)

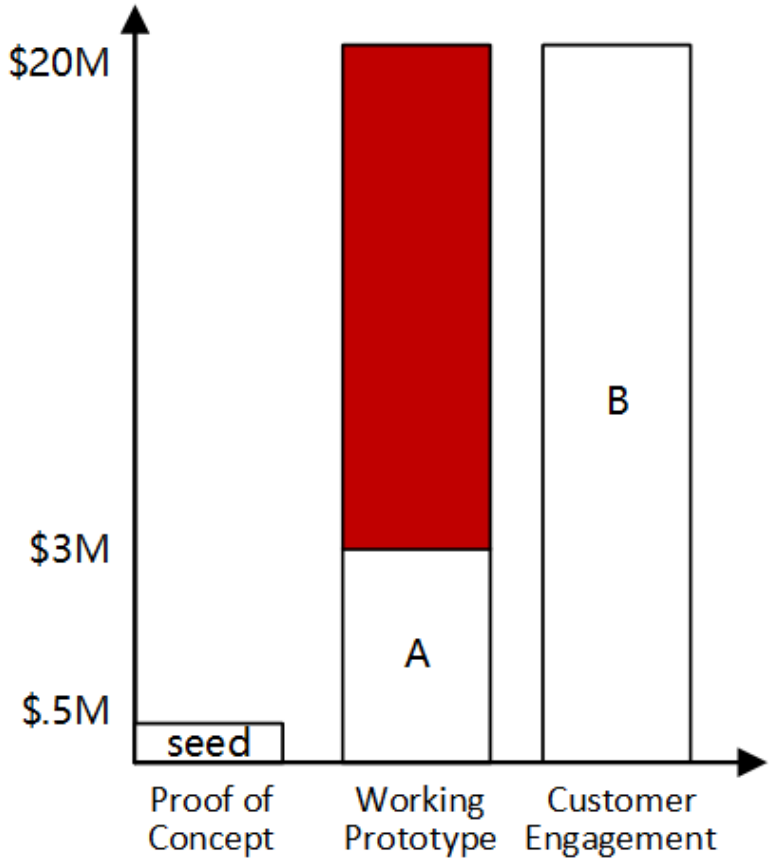
Three Dark Clouds Over the Chip Design Area

- **There are three dark clouds**
  I. Moore's Law is ending
  II. Fragmentation in IoT is coming
  III. Global supply chain crisis is appearing

- **We need innovation to counteract the dark clouds**
  - Leverage HW-SW co-design & domain-specific architecture (DSA)
  - Develop agile chip design methodology
  - Build an open & shared ecosystem

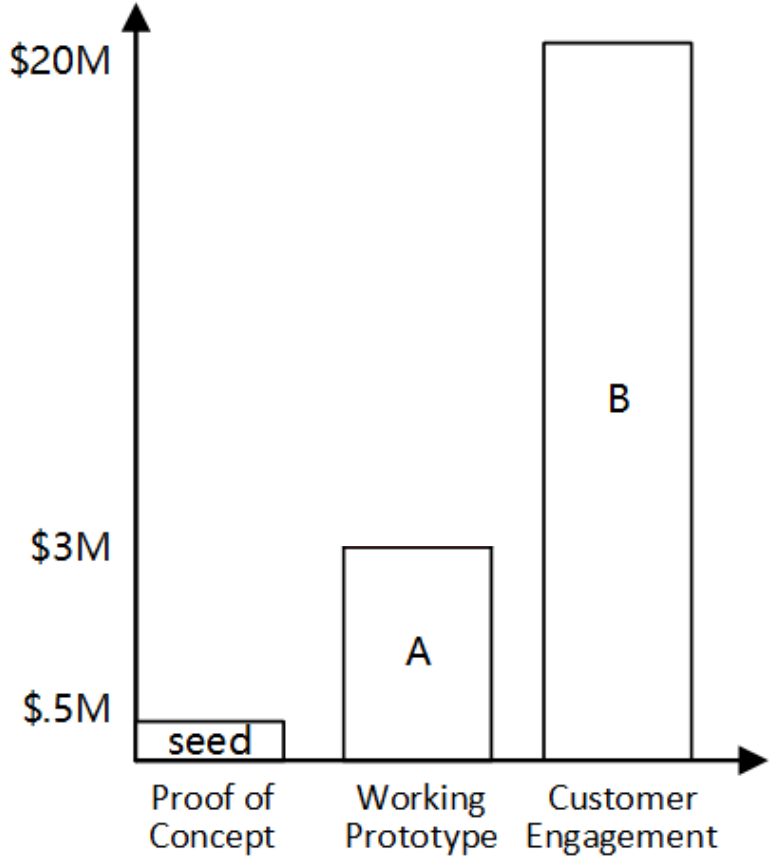
High Cost of Innovation for Chip Design

Chip Startups



V.S.

Internet Startups



Serge Leef, DARPA, Automatic Implementation of Secure Silicon, SIGARCH Visioning Workshop, 2019

Impact of Open-Source Software Ecosystem (OSSE)

- **OSSE lowers the cost of innovation**
  - A small group (**3-5 engineers**) can build a mobile App prototype in **3-5 months**
  - There were **8.9 million** mobile Apps by 2020

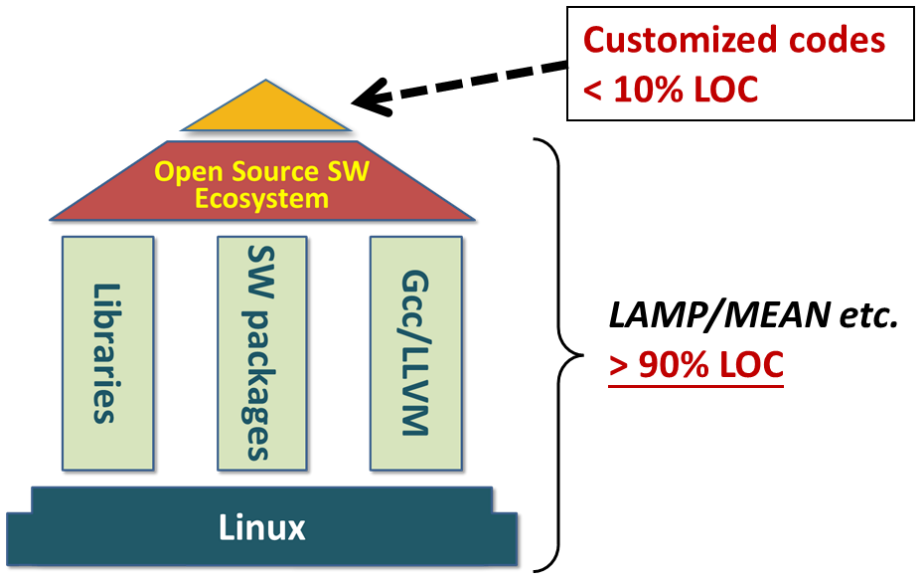
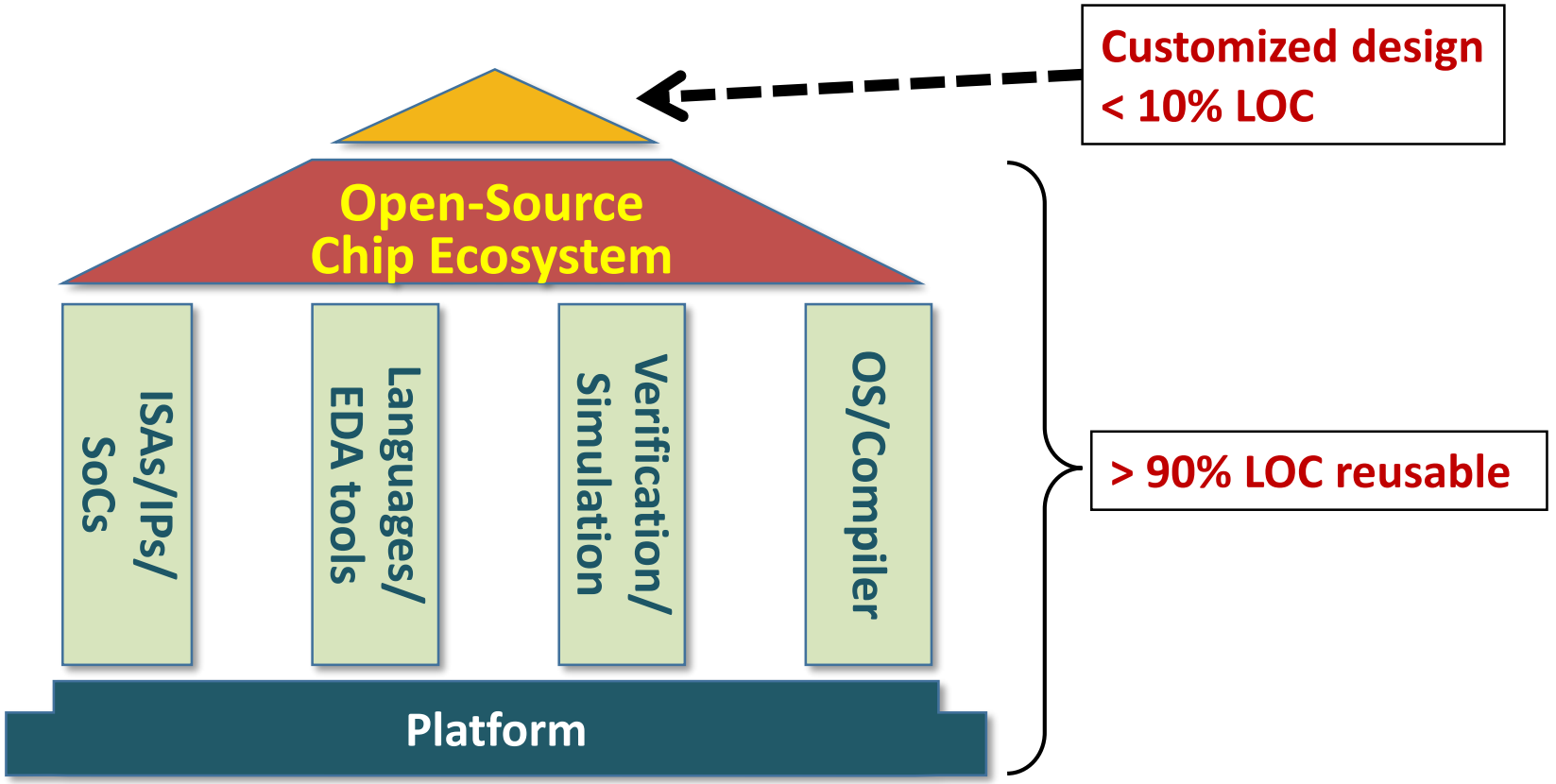


Image Source: https://blogginbryan.wordpress.com/2020/02/11/7-features-of-highly-successful-mobile-apps/

Open-Source Chip Ecosystem (OSCE)

- **Lower the barrier of chip development**
  - Save **time-to-market** and the **cost of IPs, EDA tools and engineers**



Yungang Bao, The Four Steps to An Open-Source Chip Design Ecosystem, ACM SIGARCH Visioning Workshop, June 2019

Three levels of OSCE

L1: OPEN ISA

L2: OPEN Design & Implementation

L3: OPEN Tools & Infrastructure

3 **Open Tools & Infrastructure**

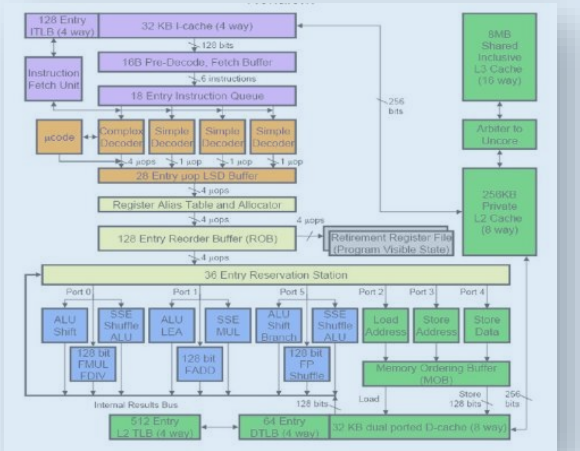
Microarch. → Engineering → EDA Tools

ISA Spec.

RISC-V®

1 **Open ISA**

Docs



RTL codes

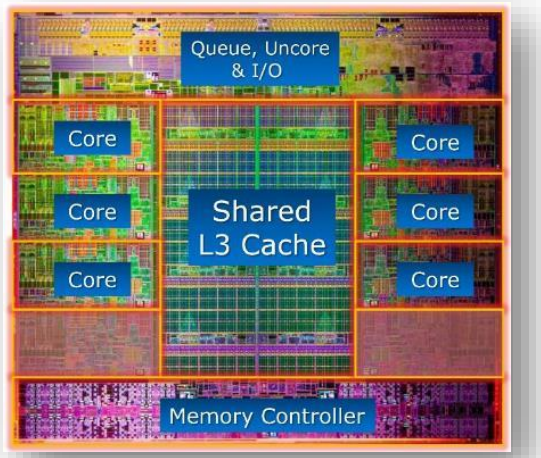
```
component DebugCoreTop is
   port (
      -- Trigger and Data
      cu_Clk      : in    std_logic_vector(2 downto 0) := (others => '0');
      cu0_Trig    : in    t_trig_0 := (others => (others => '0'));
      cu1_Trig    : in    t_trig_1 := (others => (others => '0'));
      cu2_Trig    : in    t_trig_2 := (others => (others => '0'));
      cu0_Data    : in    t_data_0 := (others => (others => '0'));
      cu1_Data    : in    t_data_1 := (others => (others => '0'));
      cu2_Data    : in    t_data_2 := (others => (others => '0'));

      -- Downstream I2C
      SCL         : in    std_logic := '0';
      SDA         : inout std_logic := '0';

      -- Upstream
      gt_RefClk_p : in    std_logic := '0';
      gt_RefClk_n : in    std_logic := '0';
      gt_RX_p     : in    std_logic_vector(2 downto 0) := (others => '0');
      gt_RX_n     : in    std_logic_vector(2 downto 0) := (others => '0');
      gt_TX_p     : out   std_logic_vector(2 downto 0);
      gt_TX_n     : out   std_logic_vector(2 downto 0)
   );
end component;
```

2 **Open Design & Implt**

Layout



Lessons from an unborn “national ISA”

- Various ISAs (**Alpha, MIPS, PowerPC, SPARC, X86 etc.**) were adopted in China around 2010
- In 2012, MIIT proposed to merge these ISAs into **a unified ISA**
- **Hard to reach a consensus**:
  - Choose an existing ISA or design a new ISA?
  - Which ISA to be chosen?
  - Who own the unified ISA?

V.S.

- **RISC-V’s answer:**

“ISAs should be free!”

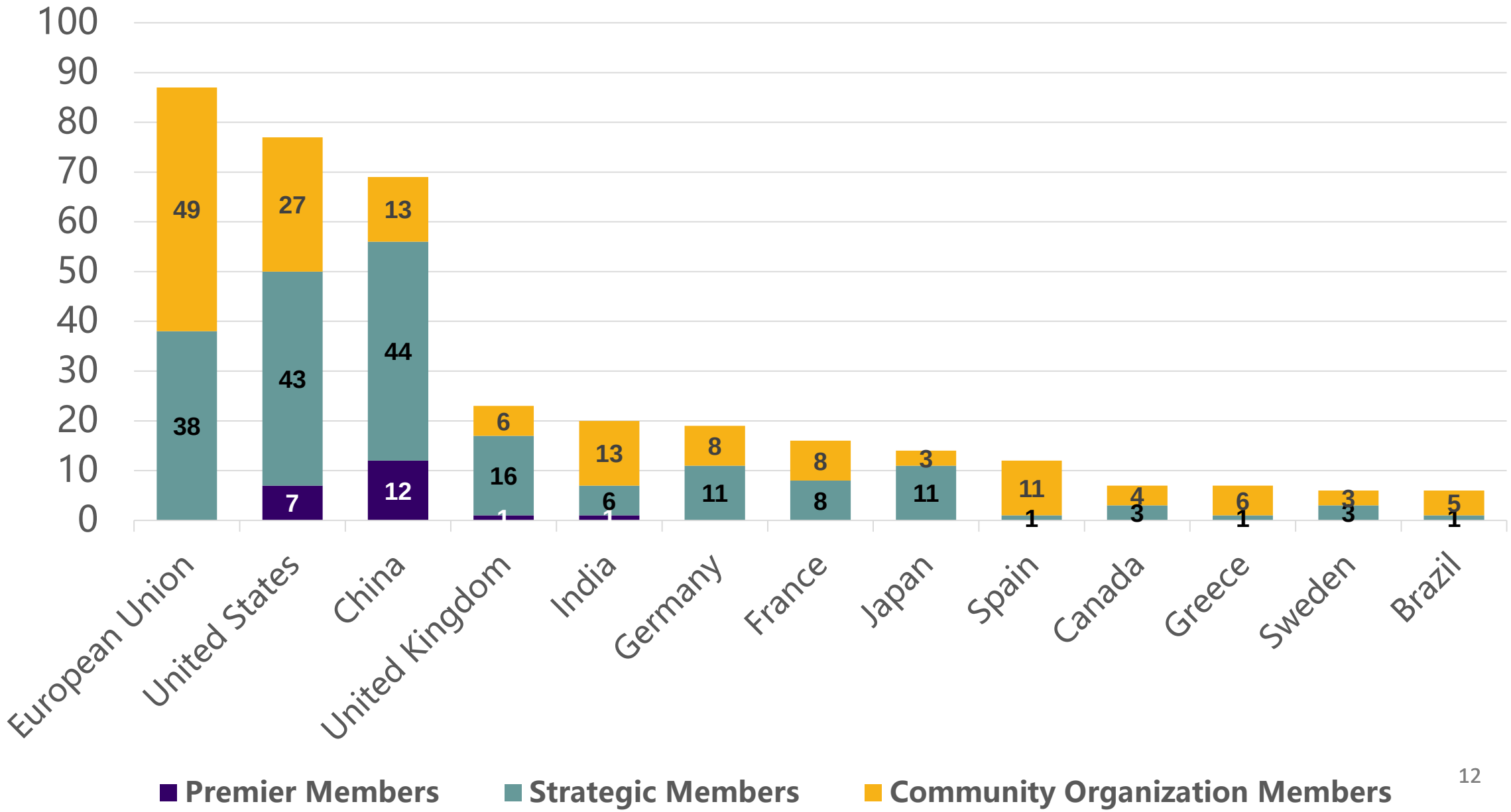
Part II

RISC-V in China

Timeline of RISC-V in China (partial)

- **2015**, Chinese version position paper was published on CCCF
- **2015**, organizations became the founding members of RISC-V Foundation
- **2016**, scholars present research work at the 4th RISC-V Workshop
- **2017**, the 6th RISC-V Workshop was held in Shanghai
- **2018**, CRVA and CRVIC were founded
- **2018,** Alibaba/T-Head (BoD) and many RISC-V startups were founded
- **2019**, CAS launched a project to promote RISC-V in China
- **2019**, RIOS Lab was established (BoD)
- **2020,** the 1st "One Student One Chip" Initiative was announced
- **2021**, the 1st RISC-V Summit China was held
- **2021**, Allwinner D1, XiangShan v1 and other ten RISC-V chips released
- **2021**, BOSC (BoD) was founded
- **2022,** more and more companies chose RISC-V, such as Tencent
- **2022**, eleven RISC-V chips released
- **2023**, Sophon announced 64-core RISC-V processor SG2042

Members of RISC-V International



RISC-V Startups in China

Company	Round of Financing	Total number of financing	Total financing amount (Million $)
Company-1	C	4	**916.2**
Company-2	A+	Many times	**140.8**
Company-3	D	6	**34.5**
Company-4	B+	3	**27.9**
Company-5	A	5	**20.0**
Company-6	A	1	**14.1**
Company-7	PreA+	3	**14.1**
Company-8	B+	2	**7.0**
Company-9	Angel Round	1	**2.8**
Company-10	Pre-A	1	**2.8**
Others	-	–	**Undisclosed**
			> 1180

RISC-V CPU IPs are widely adopted

CAS

T-Head

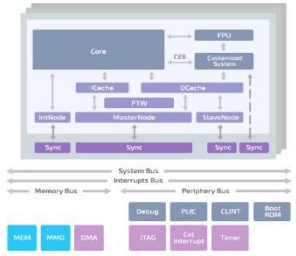
Allwinners

Nuclei

RIOS

ThunderSoft

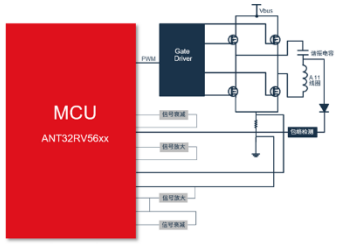
UC TECHIP



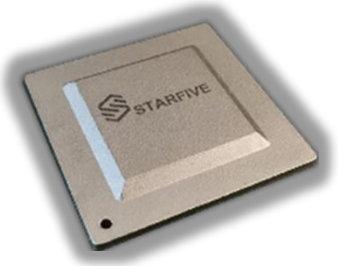
GigaDevice

ZEPP

CMSEMICON

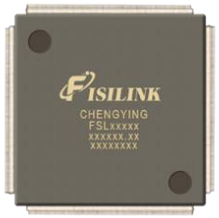


StarFive



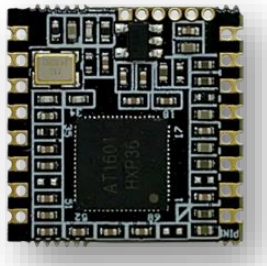
StarFive

FISILINK



MCH

TiMESiNTELLi



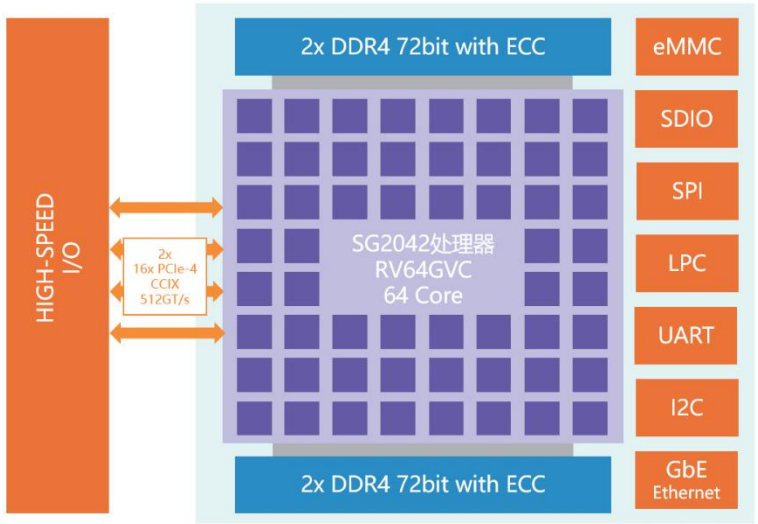
Jeejio

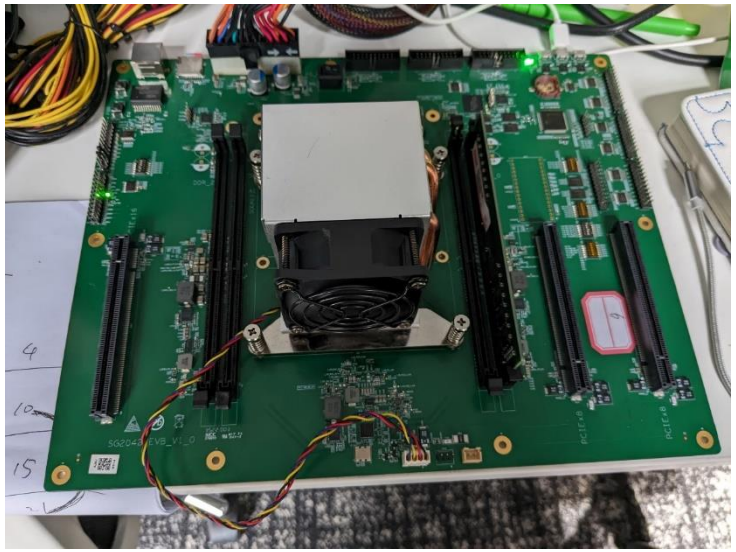
Cambricon

XITC

High performance RISC-V Chips (SOPHGO)

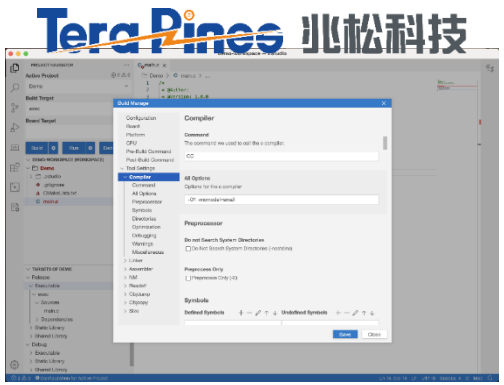
- **64 RISC-V cores** (T-Head XuanTie C920) running at up to 2GHz
- Buy **motherboard suites** from Taobao (1000-1400 USD)
- SOPHGO **donated 50** motherboards to RVI



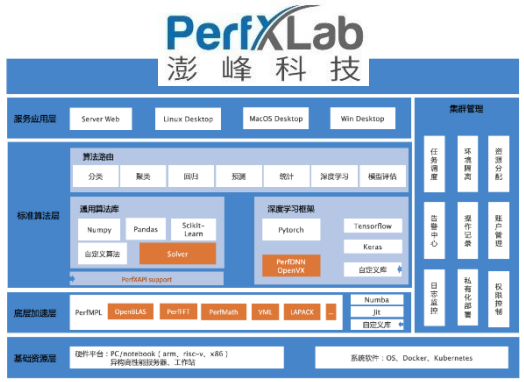


Efforts in RISC-V Software Ecosystem

Compiler & Studio

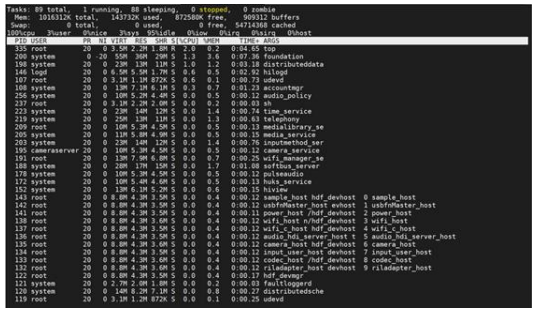


HPC Platform

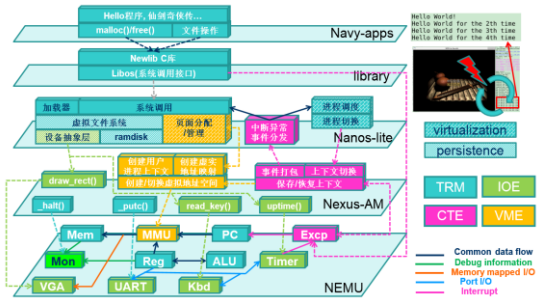


Compiler IDE

OS for RISC-V



Simulator



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Contributions from China to the RISC-V Ecosystem

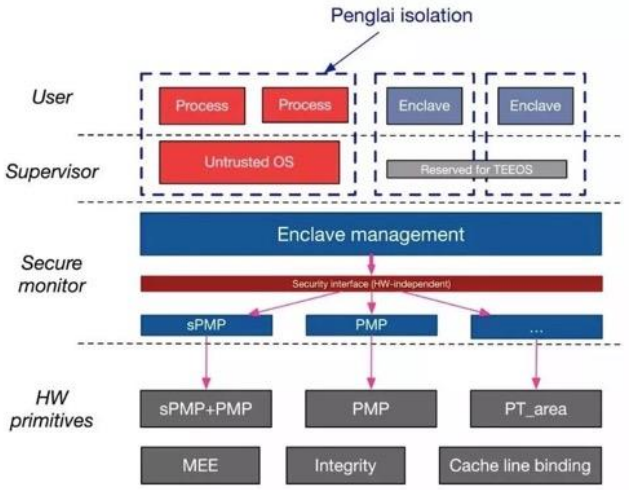
- **AOSP RISC-V** (upstreaming): main contributors (Alibaba T-Head, PLCT Lab@ISCAS, ESWIN, …)
- **OpenJDK RISC-V** (upstreamed): main contributors & port maintainers (Huawei, Aliababa, PLCT Lab@ISCAS, …)
- **V8 RISC-V** (upstreamed): main contributors & port maintainers (PLCT Lab@ISCAS), FutureWei, …)
- **Firefox Spidermonkey RISC-V backend** (upstreamed): key contributors & port maintainers (PLCT Lab@ISCAS)
- **GNU Toolchain, Clang/LLVM, MLIR, QEMU, Spike, Gem5**: active contributors (RiVAI, Alibaba, PLCT Lab@ISCAS, Huawei, WindRiver, Tsinghua, …)
- **Chisel:** active contributors & maintainers (PLCT Lab@ISCAS)
- **OpenCV RISC-V Vector Optimization**: key contributors (PLCT Lab@ISCAS)
- **OpenBLAS RISC-V Arch**: key contributors & maintainers (PerfXLab, …)
- **Box64**: key contributors (PLCT Lab@ISCAS)
- **LuaJIT:** contributors (PLCT Lab@ISCAS)
- **Debian** (RISC-V port): many active contributors (PLCT Lab@ISCAS, …)
- **Fedora** (RISC-V port): many active contributors (RedHat, PLCT Lab@ISCAS, …)
- **Arch Linux** (RISC-V port): main contributors & maintainers (PLCT Lab@ISCAS, …)
- **Gentoo Linux** (RISC-V port): main contributors & core developers (PLCT Lab@ISCAS, …)
- **openEuler** (RISC-V): key contributors & maintainers (PLCT Lab@ISCAS, …)
- ……

Source: Wei Wu@PLCT Lab

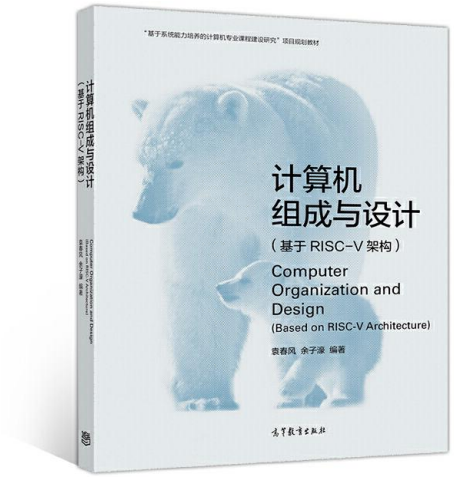
Research & Education

- MOST and NSFC are inviting proposals for RISC-V related research
- More and more universities use RISC-V for teaching

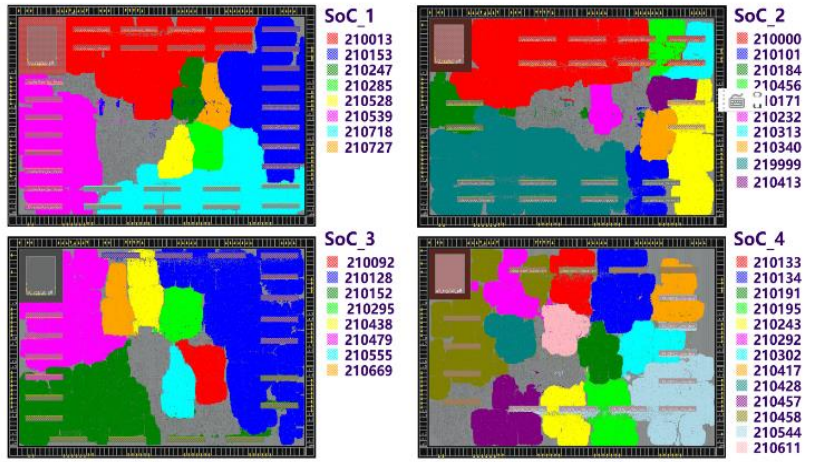
Peilai TEE @ SJTU



Textbook @ NJU



One-Student-One-Chip @UCAS



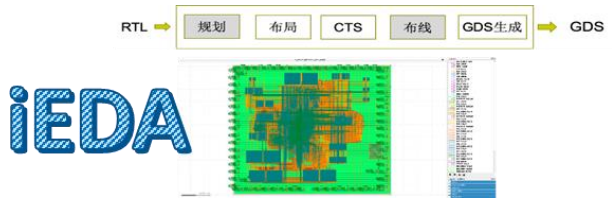
Part III

Progress in Building OSCE

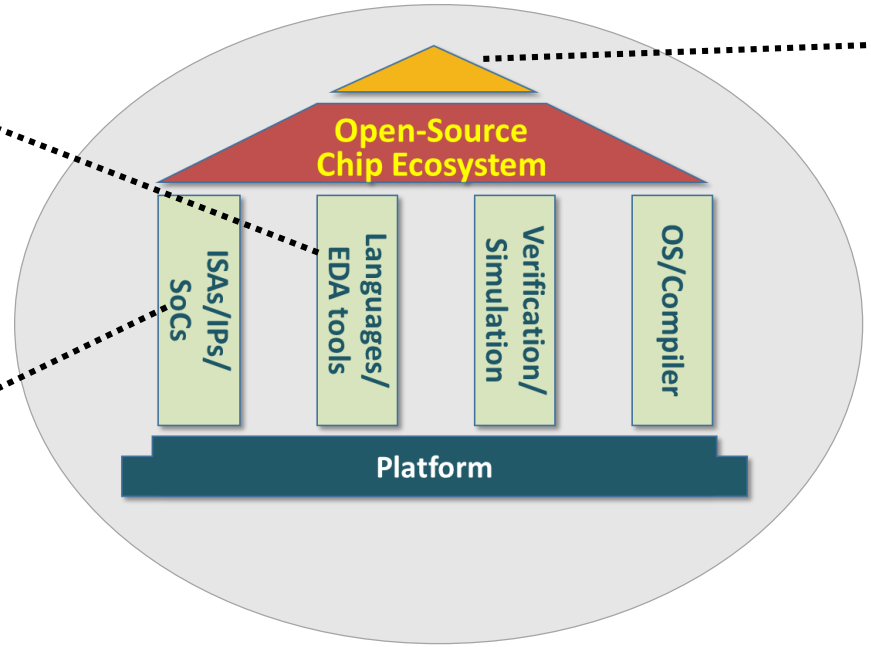
The “3-Step Plan” towards OSCE (by 2030)

- When China RISC-V Alliance (CRVA) was founded in 2018, we also put forward the “**3-Step Plan**”:
- **Step 1**: Provide silicon-proven open-source RISC-V IPs & SoCs (3-5 years)
- **Step 2**: Develop open-source SoCs by open-source EDA tools (5-7 years)
- **Step 3**: Build open-source hardware automatically by open-source EDA tools (10-15 years)

An overview of Work-in-Progress

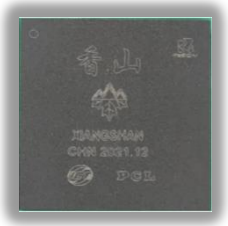


Open-source EDA



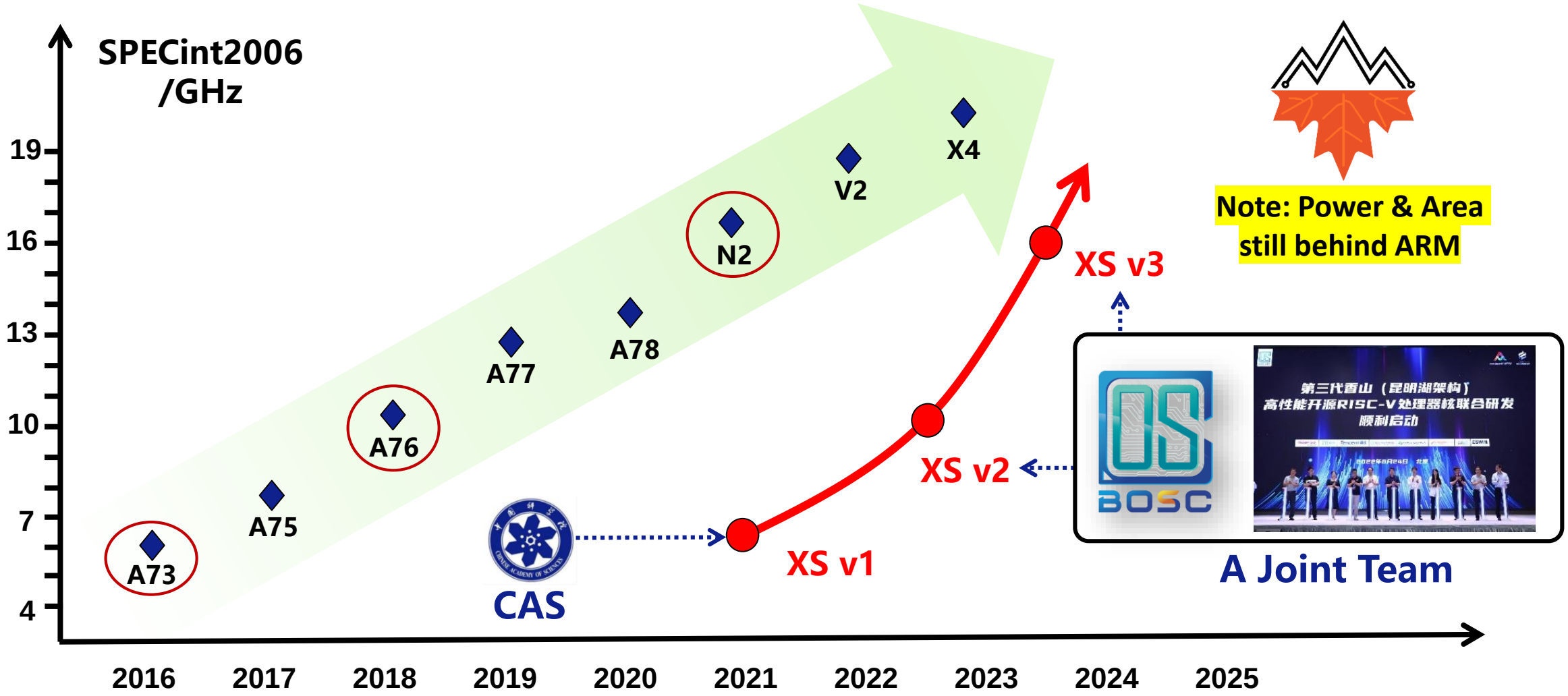
One-Student-One-Chip Initiative

XIANGSHAN



Open-Source CPU Core

XiangShan (XS): Open-Source High Performance RISC-V Core



XiangShan v1 (Yanqihu)

- RV64GC, 11-stage, 6-issue, out-of-order
- **The real chip was back in January 2022**
  - SoC: CPU, SPI Flash, UART, SD card, Ethernet, DIMM
  - Correctly running Debian with SD card and ethernet

SPECint 2006: 7.03@1GHz
SPECfp 2006: 7.00@1GHz

SPECint 2006 @ 1GHz	
400.perlbench	6.14
401.bzip2	4.37
403.gcc	6.71
429.mcf	6.83
445.gobmk	7.92
456.hmmer	5.24
458.sjeng	6.85
462.libquantum	17.71
464.h264ref	10.91
471.omnetpp	5.65
473.astar	5.16
483.xalancbmk	7.35

SPECfp 2006 @ 1GHz	
410.bwaves	9.28
416.gamess	6.59
433.milc	8.41
434.zeusmp	7.65
435.gromacs	4.99
436.cactusADM	3.97
437.leslie3d	6.93
444.namd	8.00
447.dealII	10.17
450.soplex	7.03
453.povray	7.14
454.Calculix	2.86
459.GemsFDTD	8.35
465.tonto	6.42
470.lbm	10.39
481.wrf	7.26
482.sphinx3	9.07

SSH into the Debian on XiangShan, and run a GUI program via X11 forwarding

```
wanghuizhe@open02:~$ ssh -X xs@172.28.2.246
xs@172.28.2.246's password:
Linux open02 4.20.0-44668-ge9c195ab0c63-dirty #109 Thu Feb 17 17:41:13 CST 2022

The programs included with the Debian GNU/Linux system are free software;
the exact distribution terms for each program are described in the
individual files in /usr/share/doc/*/copyright.

Debian GNU/Linux comes with ABSOLUTELY NO WARRANTY, to the extent
permitted by applicable law.
You have no mail.
Last login: Thu Feb 17 11:10:31 2022 from 172.28.9.102
xs@open02:~$ xclock
Warning: locale not supported by C library, locale unchanged
```

XiangShan v2 (Nanhu)

- **Target performance:** 2GHz@14nm, SPEC CPU2006 10/GHz (> ARM Cortex-76), 40% improvement over XS v1
  - Note: power and area are still poorer than Cortex-A76

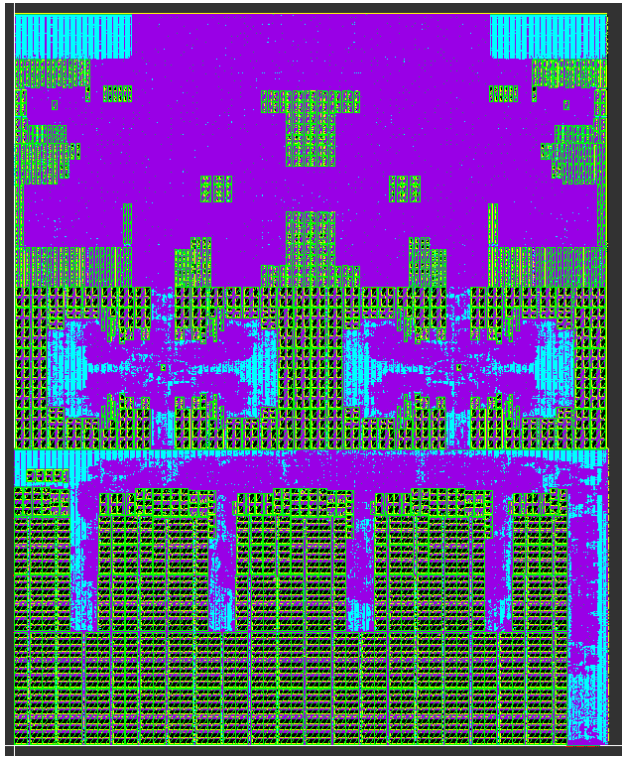
SPECint 2006: 9.55/GHz
SPECfp 2006: 11.09/GHz

*********SPECINT2006*********	
400.perlbench	19.291
401.bzip2	11.348
403.gcc	21.971
429.mcf	20.509
445.gobmk	15.981
456.hmmer	19.222
458.sjeng	17.203
462.libquantum	36.989
464.h264ref	28.542
471.omnetpp	14.009
473.astar	14.196
483.xalancbmk	21.522
SPECint2006@2GHz	***19.099***
SPECint2006/GHz	***9.549***

*********SPECFP2006*********	
410.bwaves	18.049
416.gamess	23.822
433.milc	18.328
434.zeusmp	28.14
435.gromacs	17.532
436.cactusADM	24.223
437.leslie3d	20.272
444.namd	23.837
447.dealII	33.505
450.soplex	25.64
453.povray	27.055
454.Calculix	9.185
459.GemsFDTD	24.637
465.tonto	17.669
470.lbm	32.056
481.wrf	19.728
482.sphinx3	28.353
SPECfp2006@2GHz	***22.175***
SPECfp2006/GHz	***11.088***

***Evaluation On FPGA**

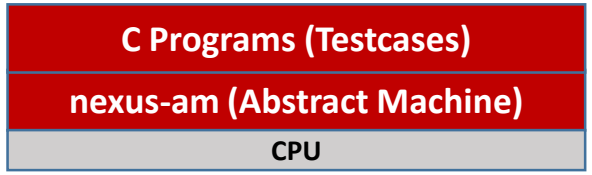
Layout of dual-core SoC



Four Levels of Verification for XiangShan

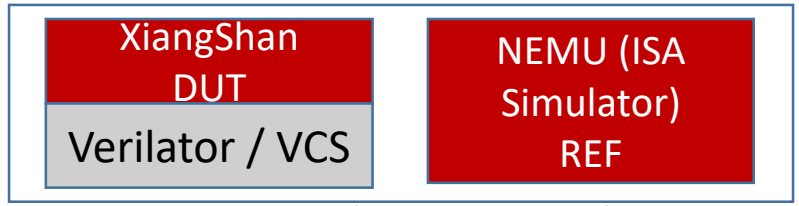
System Level

EDA： **Agile Verification**
FPGA: OS + test program



Sub system Level

EDA： **Agile Verification**
FPGA: OS + Applications



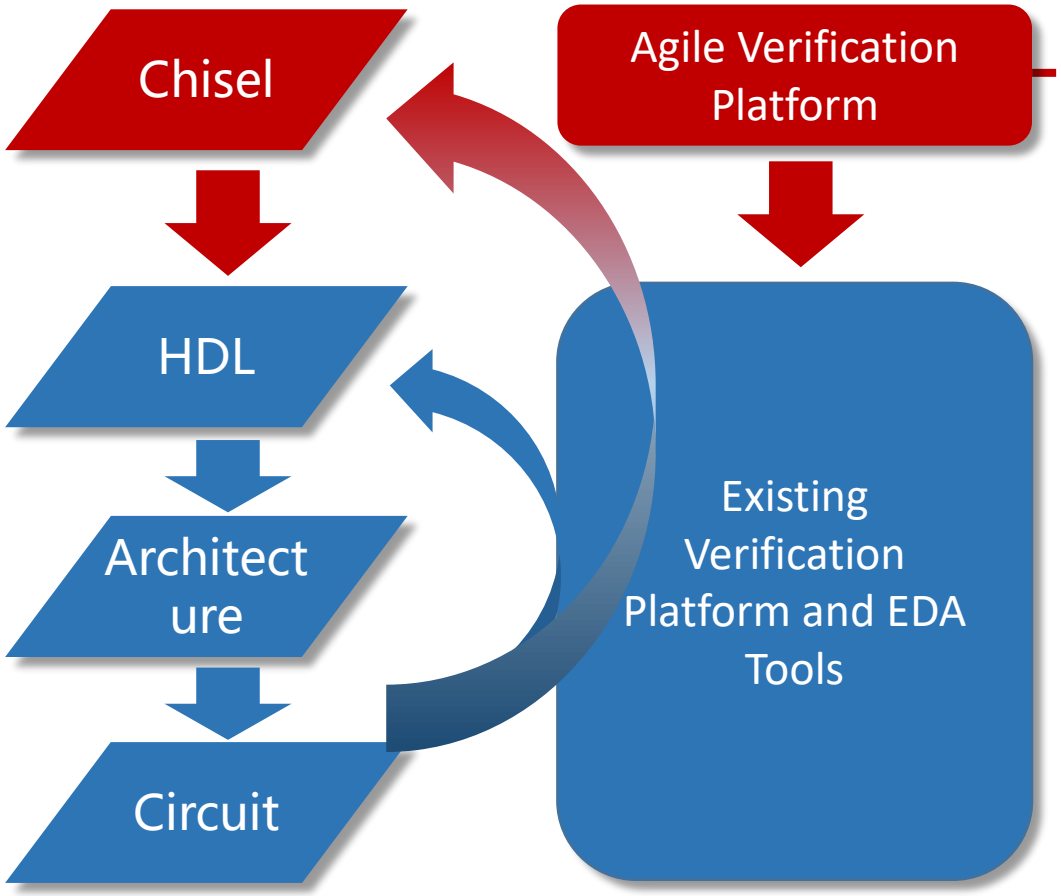
Multi-module Level

EDA： 3 DUTs, > 5000 tests

Module Level

EDA： 11 DUTs, > 7000 tests
Formal： float/fix fu

Agile Verification Flow and Tools



① Functional Verification

- difftest
- Snapshot
- ArchDB
- LightSSS
- WT

② Performance Verification

- Chisel-based prototypes
- RISC-V Checkpoint
- XSPerf
- Functional Warmup
- Top-down analysis

VERILATOR

umd-memsys/ **DRAMsim3**

DRAMsim3: a Cycle-accurate, Thermal-Capable DRAM Simulator

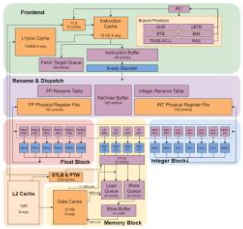
SimPoint

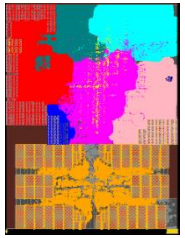
.....

Agile Verification Tools

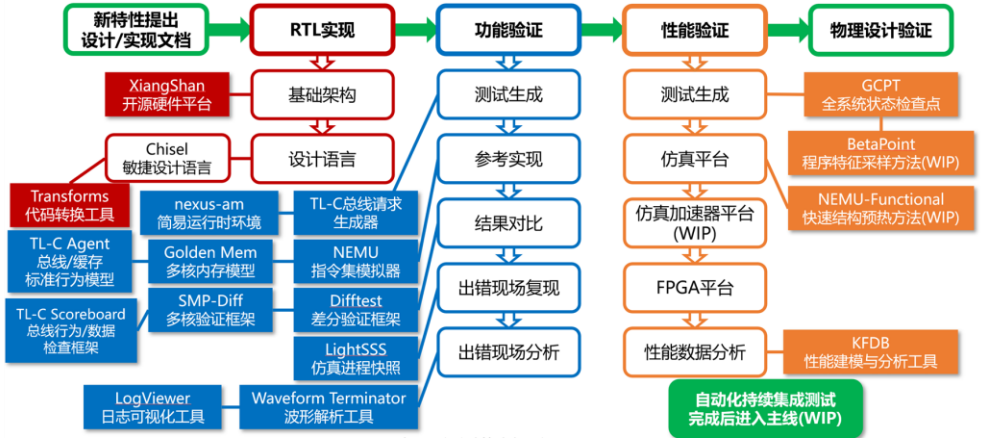
All Are Open-Sourced

XS Core RTL





Design & Verification Tools

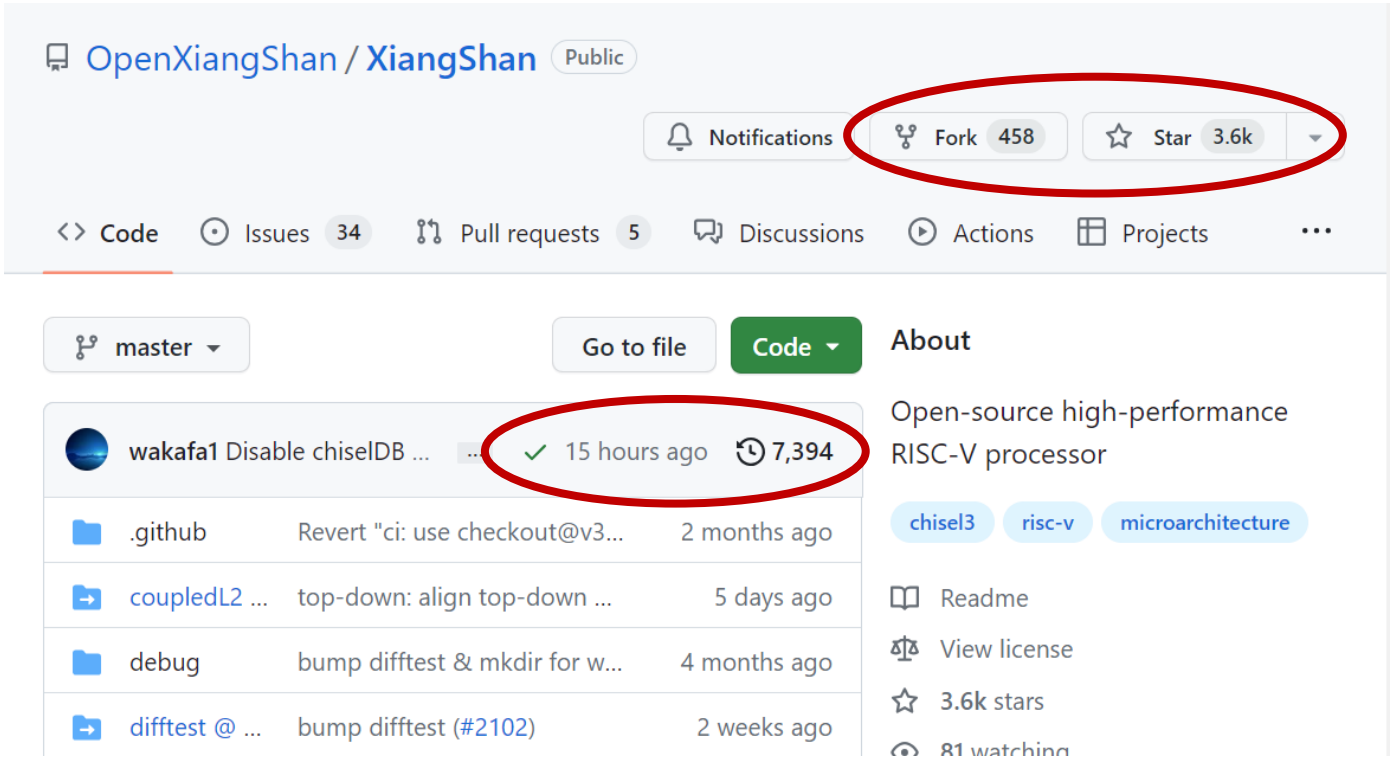


> 20 newly designed tools

Published on MICRO'2022, selected as IEEE Micro Top Picks

All Are Open-Sourced (cont.)

GitHub: ~3600 Stars, 458 Forks



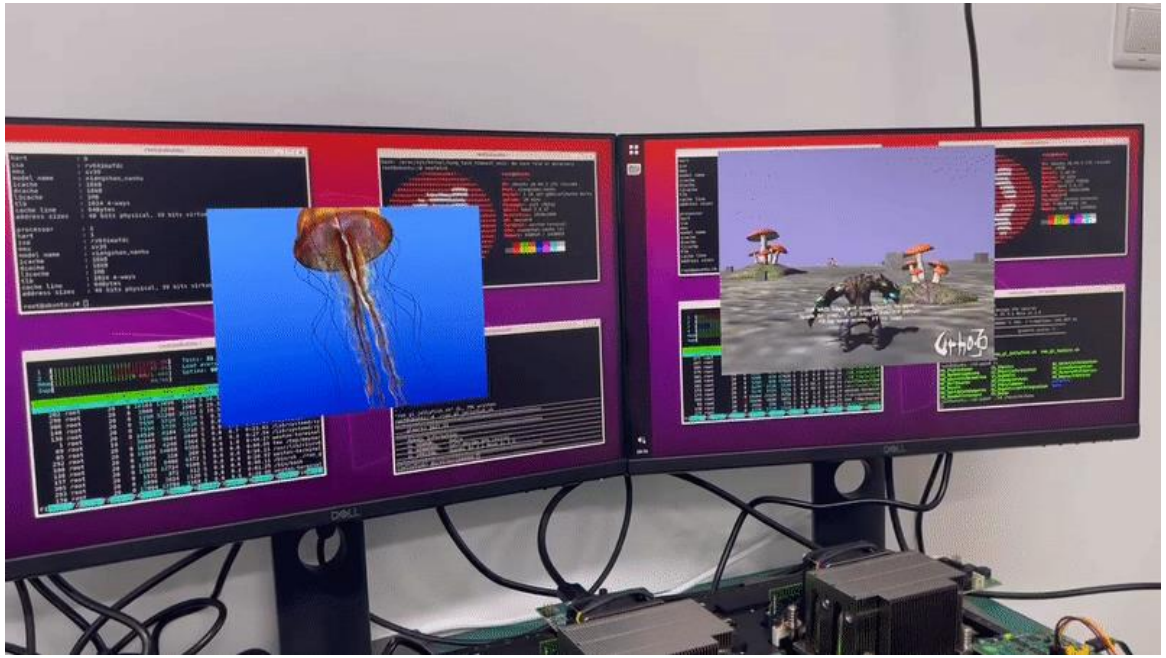
Nanhu Core Spec for Integration and Programming Guide

Contents

XiangShan is recognized and adopted by companies

- **Already used (2022)**
  - 7nm SoC Testchip, tapeout
  - 5nm AI Chip

- **Will use (2023)**
  - 28nm SoC Chip
  - 16nm Testchip
  - 12nm AI video chip
  - 12nm Server CPU
  - 7nm GPU
  - 7nm DPU
  - 7nm Server CPU



A startup (Xinchen Technology) took only **two weeks** to integrate **dual XS cores** into an SoC and run on FPGAs

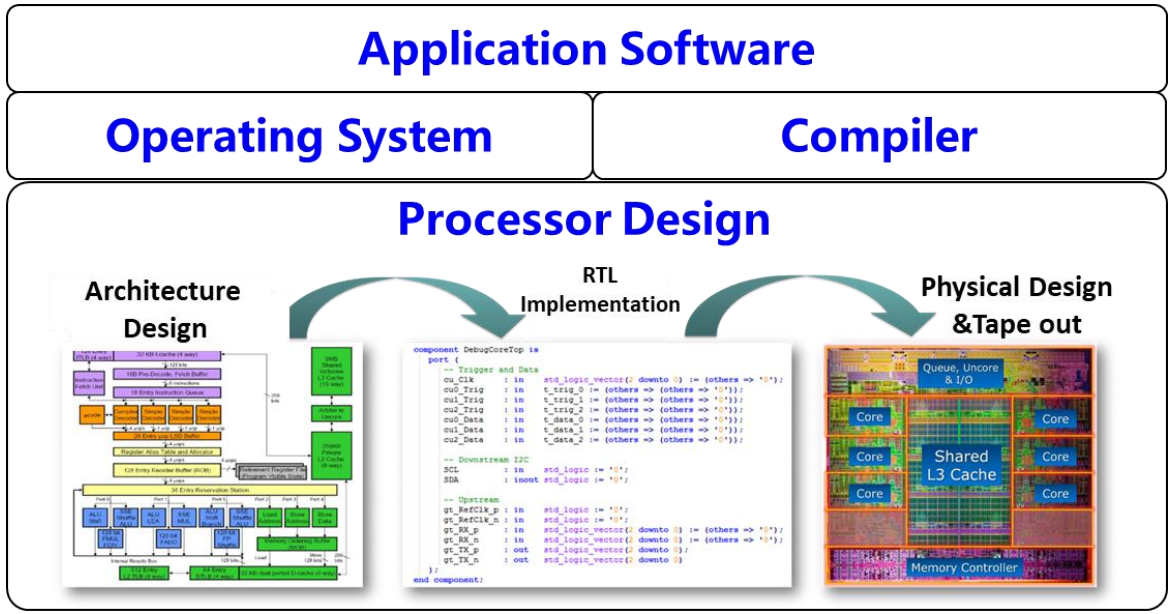
A Joint Team for XiangShan v3

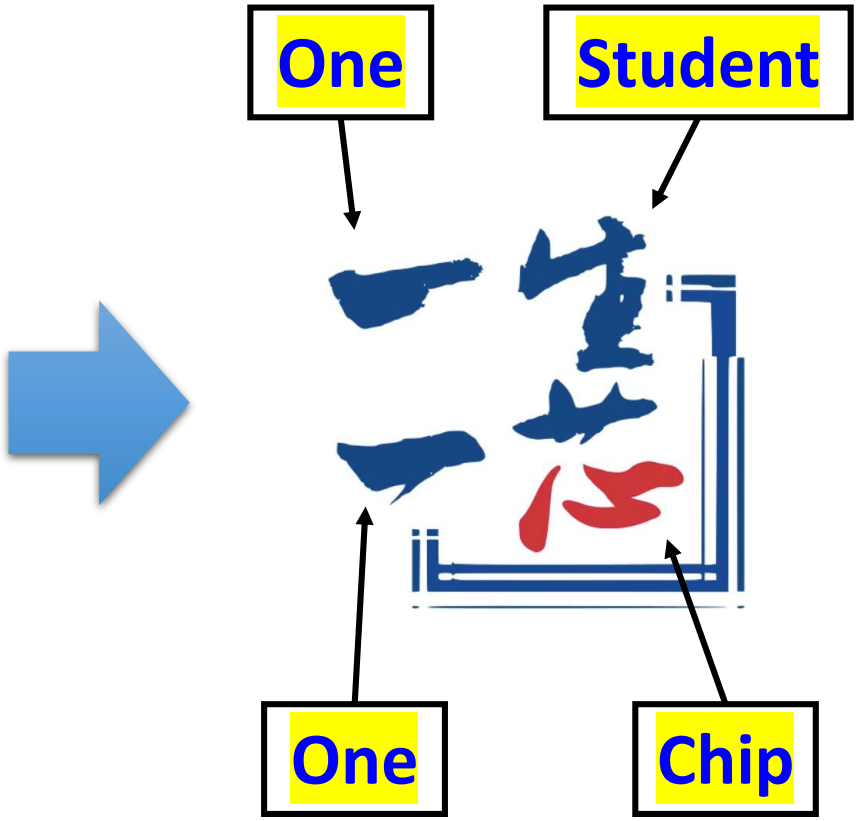
- **About 10 companies**
- **Target ARM Neoverse N2**
  - SPECCPU2006: 45 @ 3GHz (15/GHz)

Tencent 腾讯
阿里巴巴 Alibaba.com
ThunderSoft
ZTE中兴
中科创达
ESWIN
算能 SOPHGO
BOSC
北京开源芯片研究院
BEIJING INSTITUTE OF OPEN SOURCE CHIP

The One Student One Chip (OSOC) Initiative

- Learning-by-Doing: Teach undergraduates to build real chips
- Launched the OSOC Initiative in 2019





The 1st OSOC (2019)

- Five senior undergraduates participated
- Completed the design of **a 64-bit RISC-V** processor in four months
- The chip was **taped out** with 110nm and ran Linux and a self-built UCAS-core OS

Yue Jin

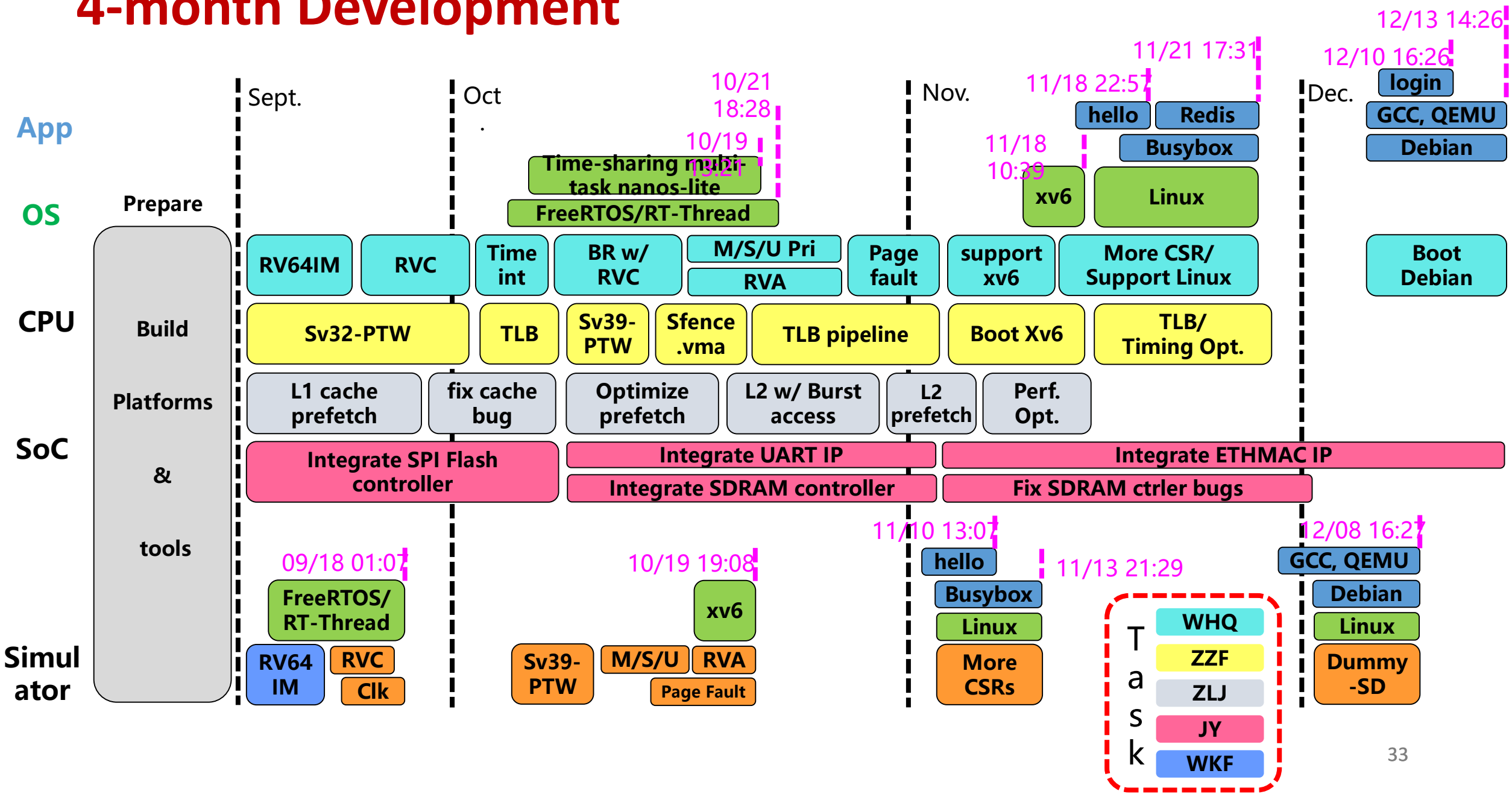
Huangqiang Wang

Kaifan Wang

Linjuan Zhang

Zifei Zhang

4-month Development

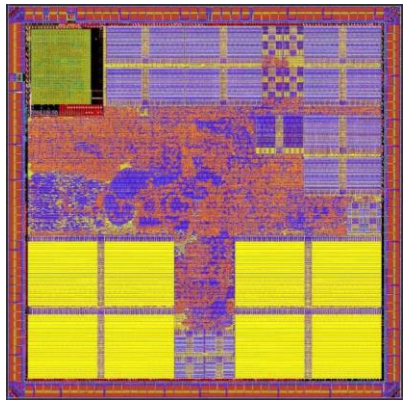


NutShell: A Linux-Compatible RISC-V Processor Designed by Undergraduates

A 64-bit RISC-V Processor

- Single-issue, 9-stage, in-order
- RV64IMAC，support M/S/U
- 2-bit BPU，512 BTB，16 RAS
- Sv39, hardware TLB refill
- 32K L1I & L1D
- Read consistency for L1I & L1D
- 128K L2 cache，next line prefetch
- Use Chisel
- SDRAM, SPI flash, UART
- Support Linux 4.18.0 kernel
- Support Busybox
- Can run Debian 11 on Emulator & FPGA

Tape-out w/ 110nm-node



- 110nm
- 10mm^2
- 200mw@350MHz Typical
- TQFP100 package

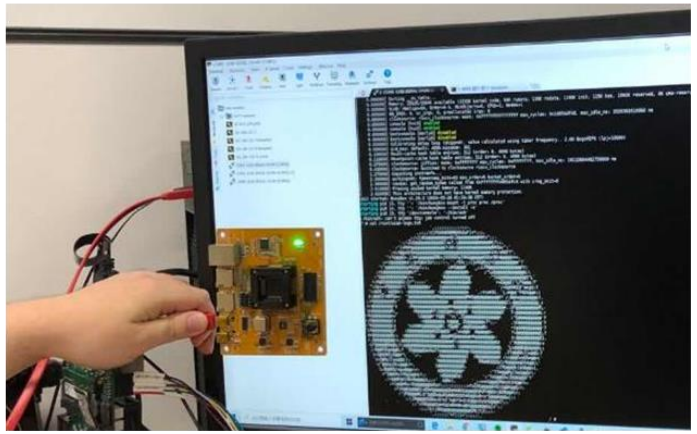
Real Chips

Chips

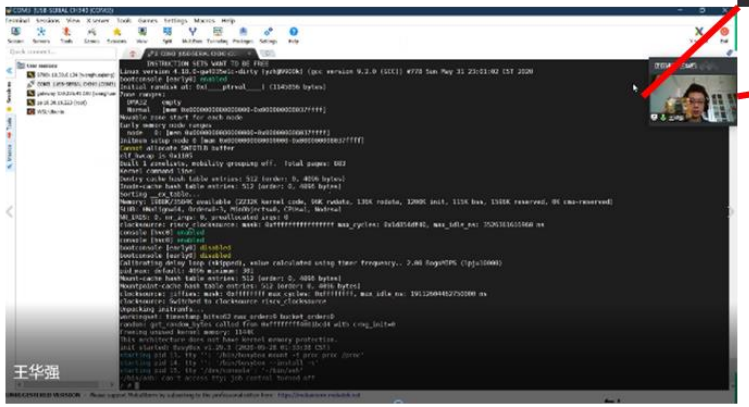
Frequency: 350MHz

配置开关	倍率	50MHz晶振	100MHz晶振
000	1	50MHz	100MHz
001	1.5	75MHz	150MHz
010	2	100MHz	200MHz
011	2.5	125MHz	250MHz
100	2.75	137.5MHz	275MHz
101	3	150MHz	300MHz
110	3.5	175MHz	350MHz
111	4	200MHz	400MHz

Demo



Run Linux
Display CAS logo



Theis Defense
2020.6.2

Accepted to RISC-V Global Forum 2020

NutShell: A Linux-Compatible RISC-V Processor Designed by Undergraduates

Your submission was accepted for RISC-V Global Forum 2020

The RISC-V Event Team ★ 详情

Dear Huaqiang,

It is our pleasure to inform you that we have accepted your submission, ***Nutshell: A Linux-Compatible RISC-V Processor Designed by Undergraduates,*** as a lightning talk, and would like to welcome you as a speaker to the RISC-V Global Forum 2020, happening virtually Thursday, September 3. Sessions will overlap during US, Europe, and Asia working hours. We ask that you please review the information below and on the Speaker Guide and complete all the required items to confirm your speaking engagement.

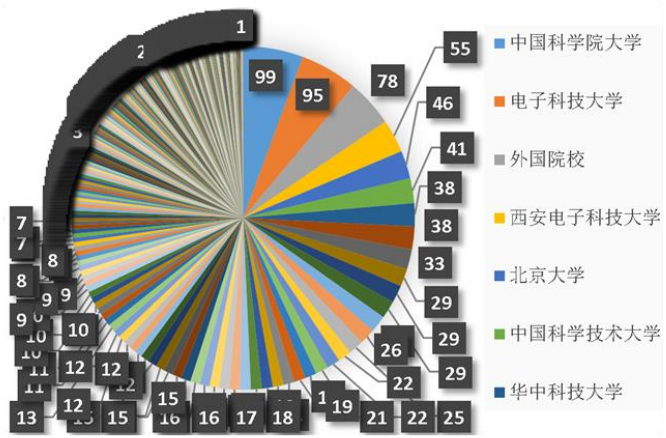
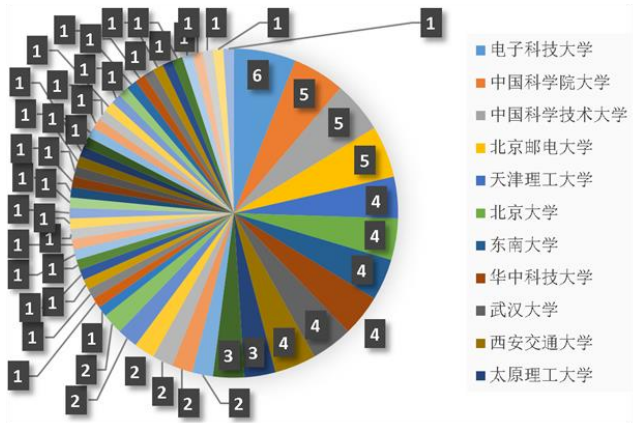
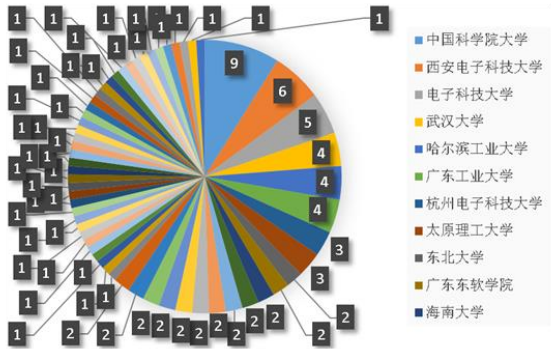
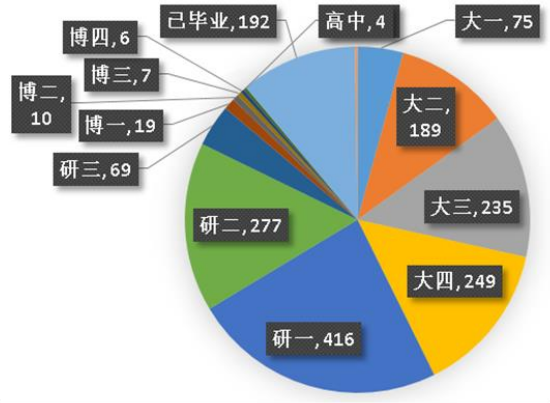
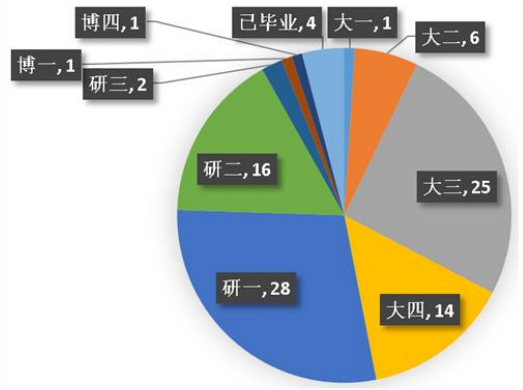
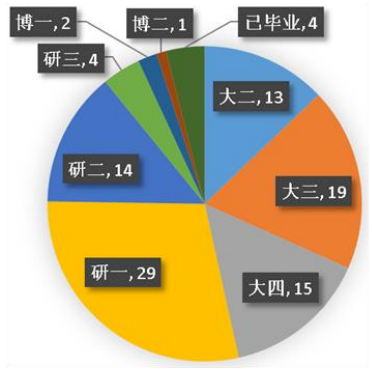
The event will take place on the virtual event platform, MeetingPlay. The

> 4000 students participated in the OSOC Initiative

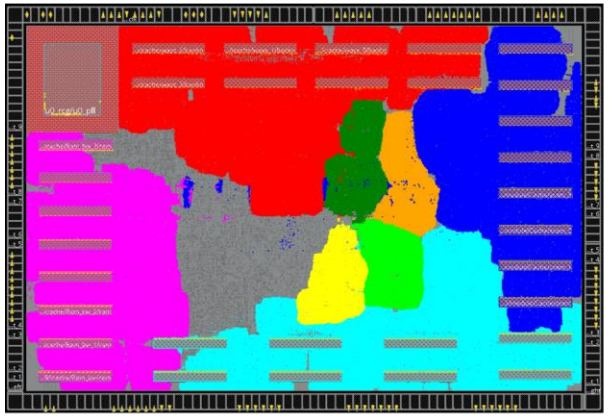
No.	Start	End of Enrollment	#Enrollment	#School	#Stu. Learning > 10%	#Stu. Finish
1st	Aug, 2019	-	5	1	5	5
2nd	Aug, 2020	-	11	5	11	11
3rd	Jul, 2021	Sep, 2021	760	168	215	51
4th	Feb, 2022	Aug, 2022	1753	328	215	16
5th	Aug, 2022	In progress	1689	335	148	6
6th	Will start in July, 2023					

Updated: Jun 6th, 2023

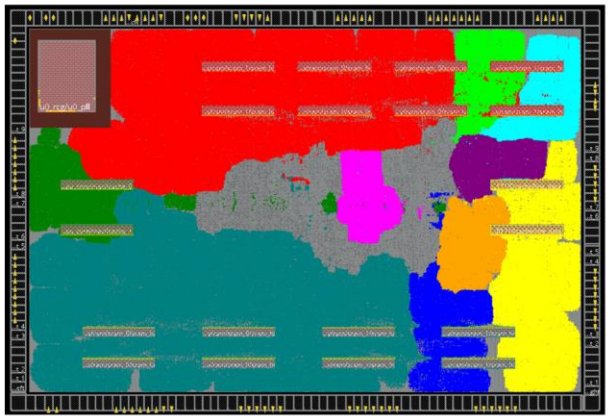
Track how students are learning

	Applications(1753)	Basic (98)	Advanced (101)
Universities			
Grades			

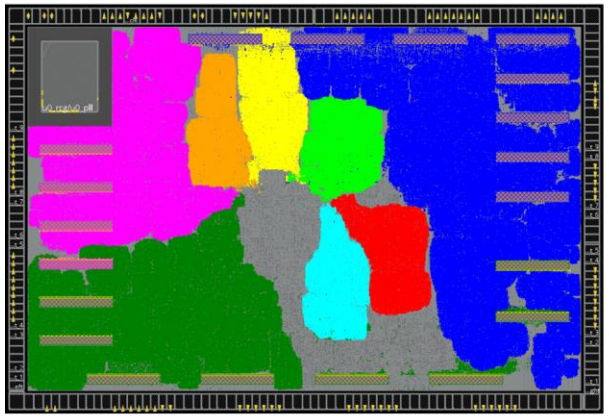
GDSII Layouts of Chips Designed by 50 Students



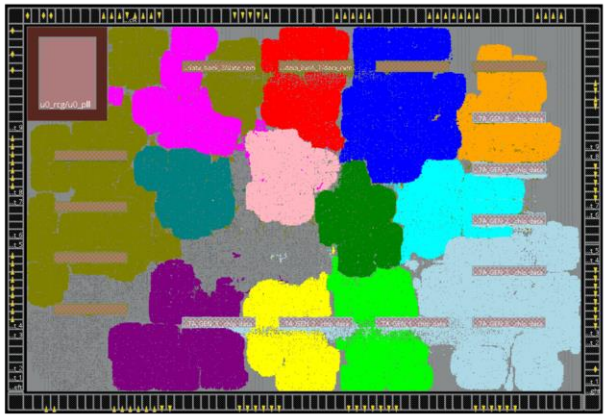
SoC_1
- 210013
- 210153
- 210247
- 210285
- 210528
- 210539
- 210718
- 210727



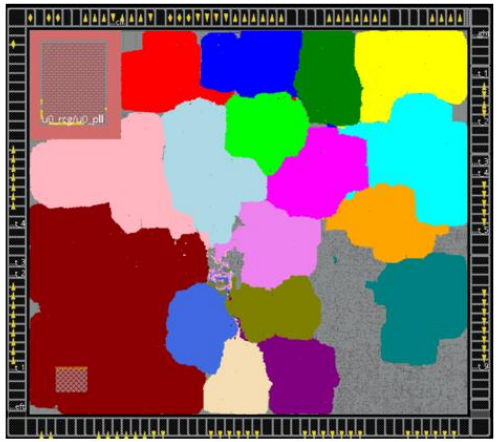
SoC_2
- 210000
- 210101
- 210184
- 210456
- 210171
- 210232
- 210313
- 210340
- 219999
- 210413



SoC_3
- 210092
- 210128
- 210152
- 210295
- 210438
- 210479
- 210555
- 210669

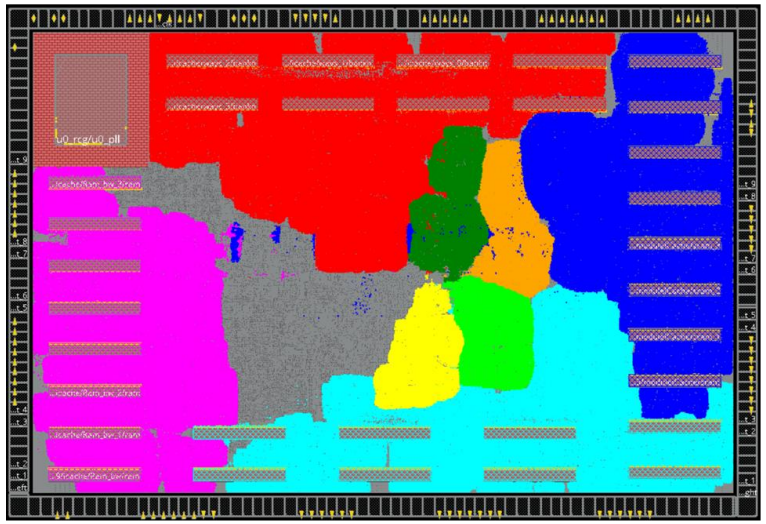


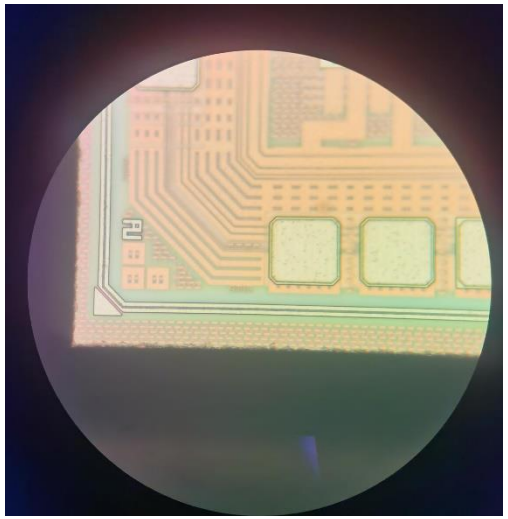
SoC_4
- 210133
- 210134
- 210191
- 210195
- 210243
- 210292
- 210302
- 210417
- 210428
- 210457
- 210458
- 210544
- 210611

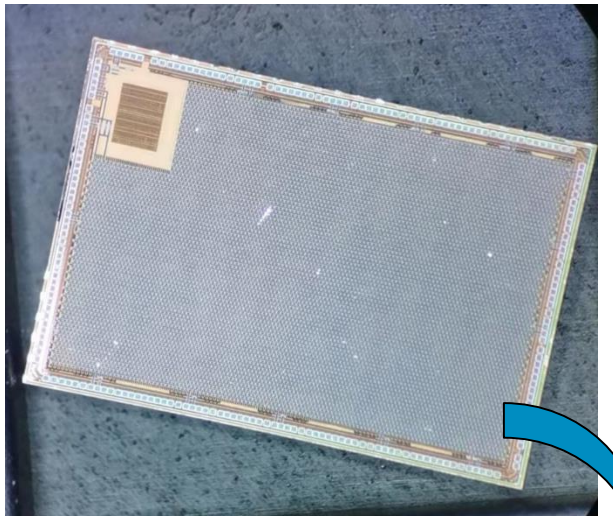


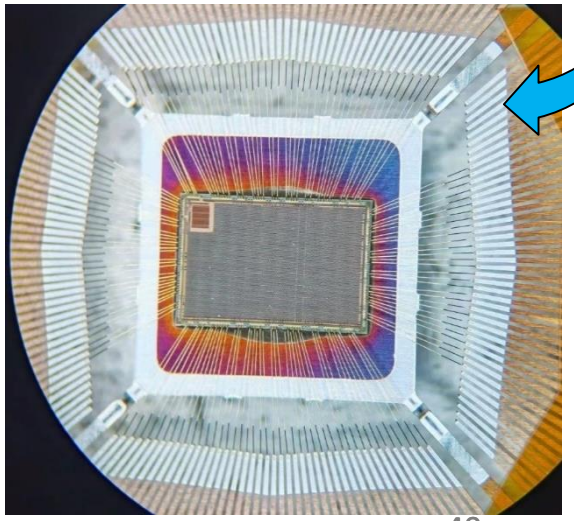
SoC_5
- 210745
- 210407
- 210596
- 210703
- 210366
- 210448
- 210324
- 210760
- 210746
- chenxi
- chenguokai
- hbh
- lx
- yanyue
- yyh
- zjv
- zzy

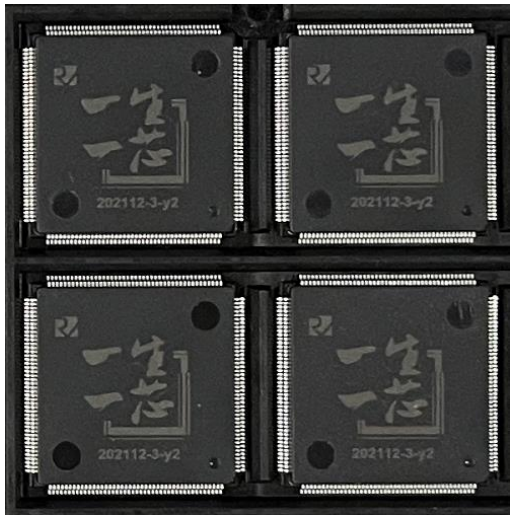
Real Chips were Back

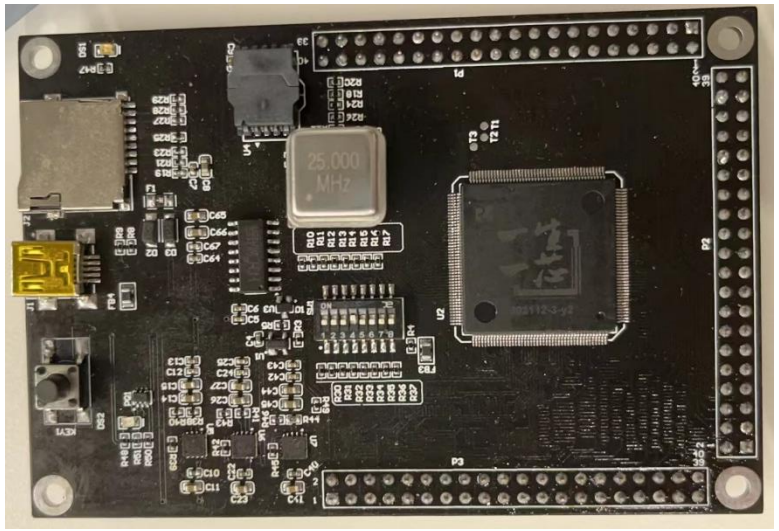




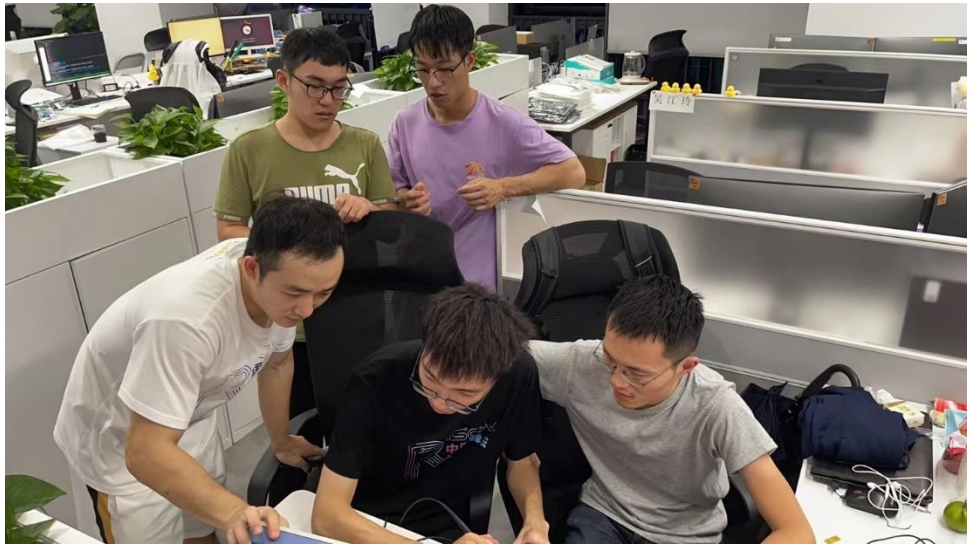


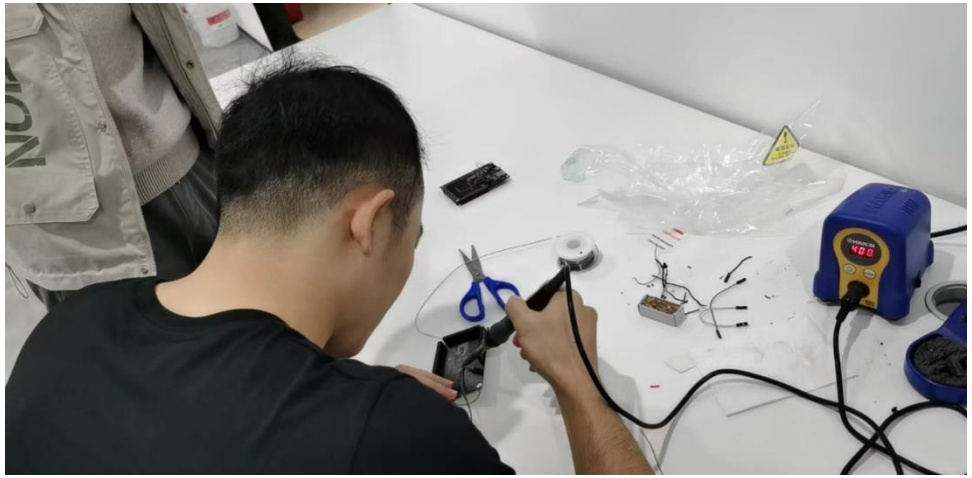


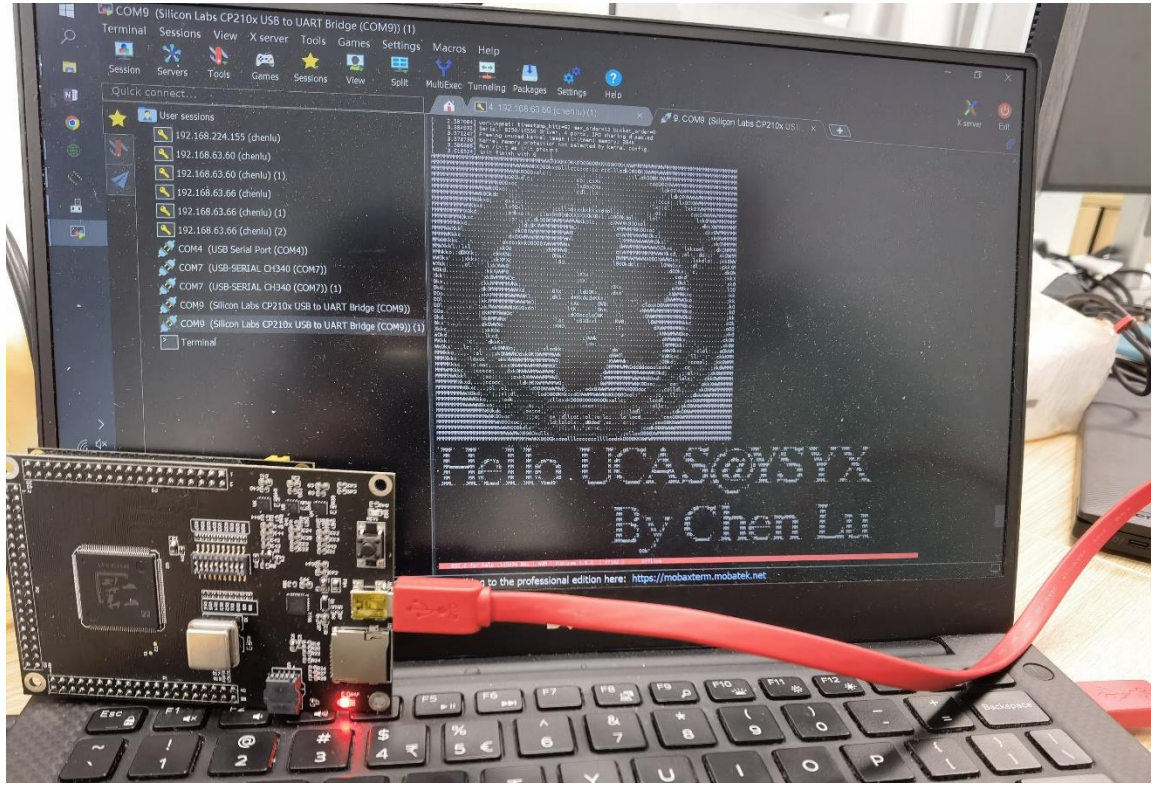




Testing Chips







Contributors to RVI Certification Course

- **Translate Courses into Chinese**
  - RISC-V Overview
  - RISC-V Instruction Set Architecture
  - Assembly Language for RISC-V
  - High Level Languages for RISC-V - C Programming
  - RISC-V Operating Systems & Tools

Name	University
Faker Miao	University of Science and Technology of China
Zhenwei Duan	University of Science and Technology of China
Frank Liu	Taiyuan University of Technology
Asher Cao	University of Science and Technology of China
Haifan Yang	Zhejiang Gongshang University
Caosy	University of Science and Technology of China
Rentao Ni	Northeastern University, China
Ren Wei	Lanzhou University
Jiabin Wu	ShanghaiTech University
Lu Chen	University of Chinese Academy of Sciences
Jinlun Su	Taiyuan University of Technology


Faker Miao


Zhenwei Duan


Frank Liu


Asher Cao


Haifan Yang


Caosy


Rentao Ni


Ren Wei


Lu Chen

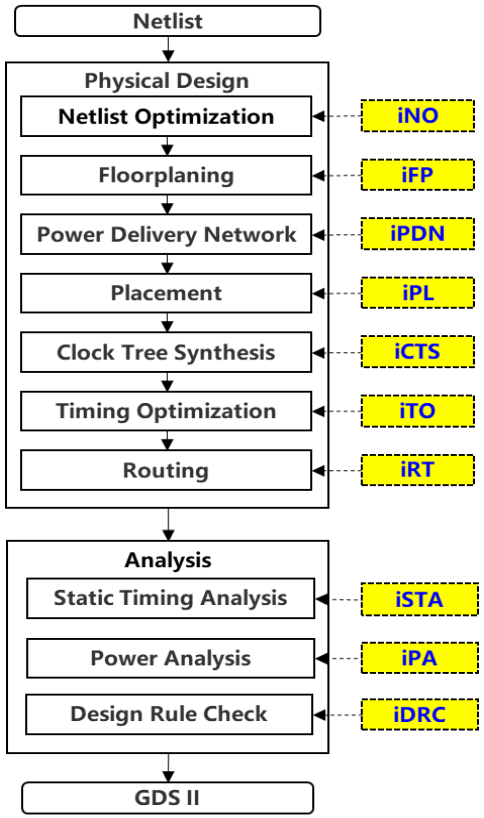

Jinlun Su


Jiabin Wu

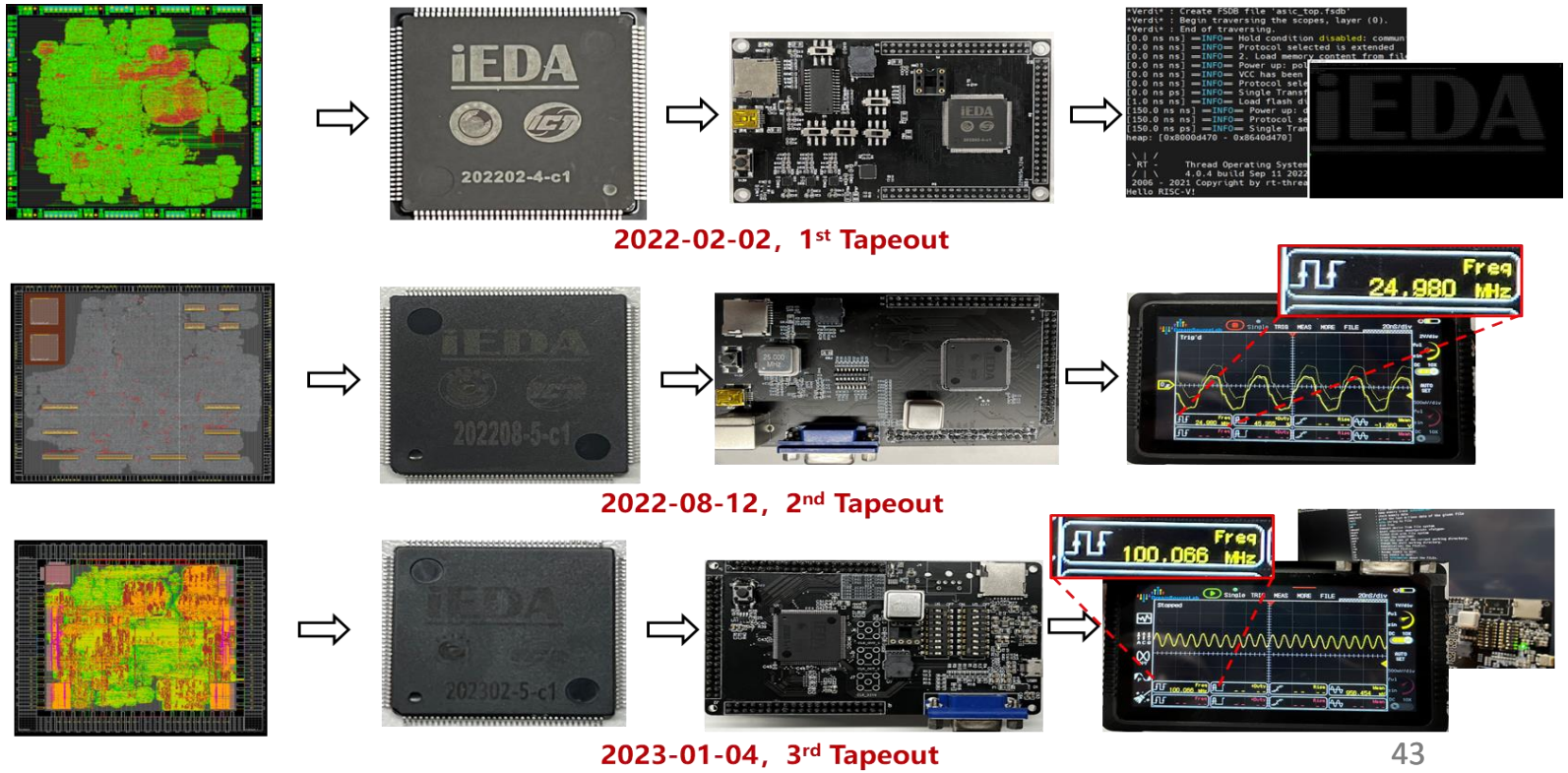
What's Next?

- Have developed an open-source EDA tools (iEDA) and completed three tape-outs
- Will let students use open-source EDA tools to build open-source Chips

iEDA Flow w/ 11 new Tools



Three tape-outs w/ iEDA (110nm, 110nm, 28nm)



Towards Three levels of OSCE

3 Open Tools & Infrastructure

Microarch. Engineering EDA Tools

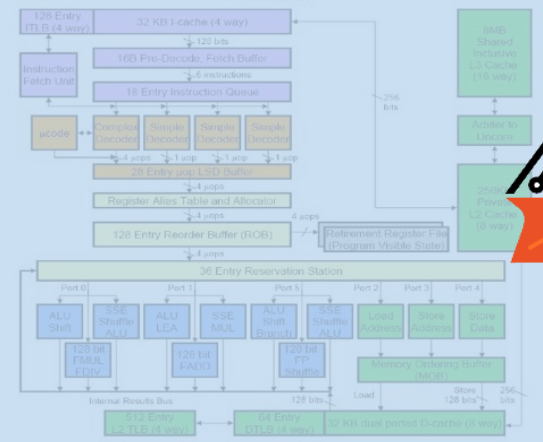
+ iEDA

ISA Spec.

RISC-V®

1 Open ISA

Docs

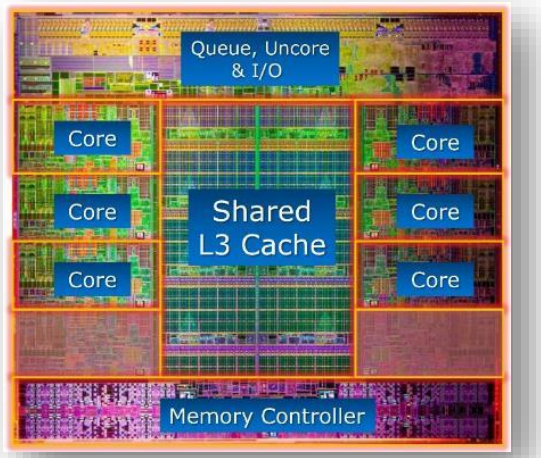


RTL codes

```
component DebugCoreTop is
  port (
    -- Trigger and Data
    cu_Clk      : in    std_logic_vector(2 downto 0) := (others => '0');
    cu0_Trig    : in    t_trig_0 := (others => (others => '0'));
    cu1_Trig    : in    t_trig_1 := (others => (others => '0'));
                : in    t_trig_2 := (others => (others => '0'));
                : in    t_data_0 := (others => (others => '0'));
                : in    t_data_1 := (others => (others => '0'));
                : in    t_data_2 := (others => (others => '0'));
                eam I2C
                : in    std_logic := '0';
                : inout std_logic := '0';
    - Upstream
    _RefClk_p : in    std_logic := '0';
    _RefClk_n : in    std_logic := '0';
    gt_RX_p     : in    std_logic_vector(2 downto 0) := (others => '0');
    gt_RX_n     : in    std_logic_vector(2 downto 0) := (others => '0');
    gt_TX_p     : out   std_logic_vector(2 downto 0);
    gt_TX_n     : out   std_logic_vector(2 downto 0)
  );
end component;
```

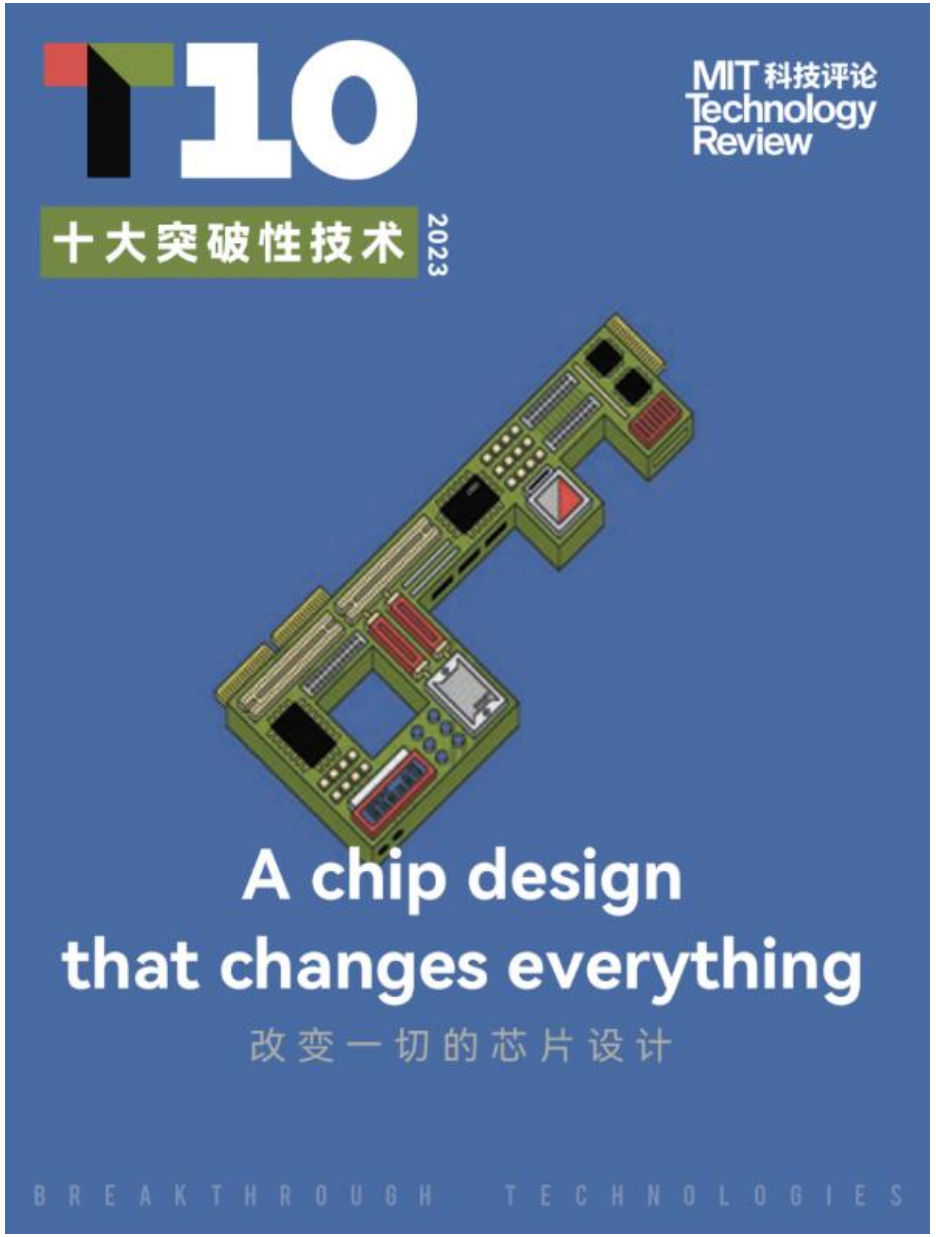
2 Open Design & Implt

Layout



Summary

- **RISC-V: A chip design that changes everything**
  - 10 breakthrough of MIT TR 2023
- **It is the best time for us to build a globally shared open-source chip ecosystem**
- **The Chinese community has been contributing and will contribute more to OSCE**



Welcome to RISC-V Summit China 2023 in Beijing

RISC-V® Summit China 2023

RISC-V®
Summit China 2023

August 23-25, 2023

Beijing, China

- ≥ **1000** in-person, ≥ **100,000** online

Shangri-La Beijing

How to participate in RISC-V Summit China 2023

Sponsors

DDL: 30th June

email：anxu@bosc.ac.cn

For Non-sponsors

DDL: 15th July

Exhibition display booths

Speakers

DDL: 5th July

Call for Speakers:

https://riscv-summit-china.com/submit-my-talk.html

Notification to Authors： 20th July

Agenda Published： 10th Aug

On-site attendance

website：**https://riscv-summit-china.com**

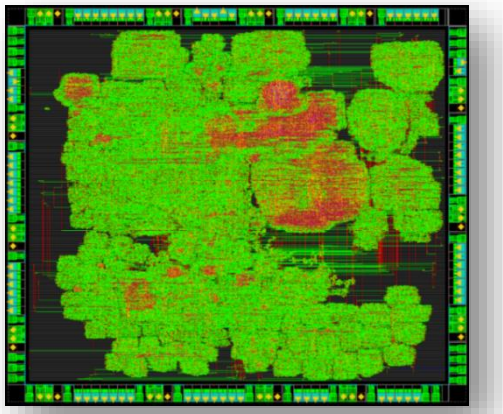
Registration will open at the end of June - beginning of July

Thanks!

iEDA-Tapeout

- 1st Tapeout
  - 2022-02-02，110nm node，0.7M gates, Freq: 25MHz，Core Density: 30%
- 2nd Tapeout
  - 2022-08-12, 110nm node，1.5M gates, Freq: 25MHz, Core Density: 35%
- 3rd Tapeout
  - 2023-01-04, 28nm node，1.5M gates, Freq: 200MHz, Core Density: 40%

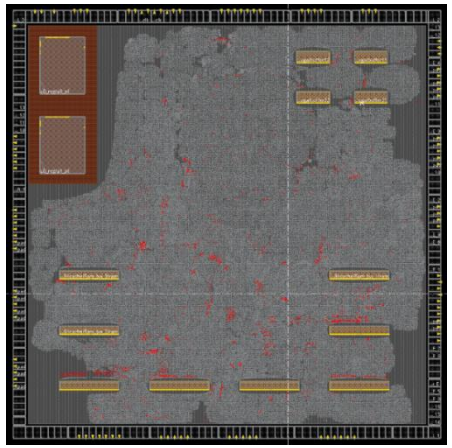
2022-02-02，1st Tapeout



110nm node，0.7M gates, 25MHz
(5-level pipeline，IP:Chiplink、UART、SPI)

Macro, Multi-clock,
Scale increasing,
Auto-design

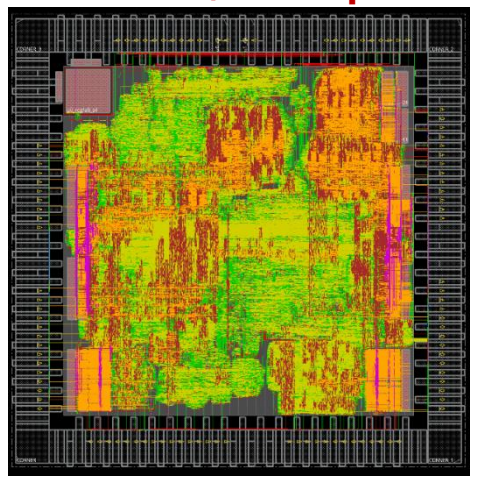
2022-08-12，2nd Tapeout



110nm node，1.5M gates
(11-level pipeline with cache、IP:
UART、VGA、PS/2、SPI、SDRAM,
Two PLL on SoC，Support Linux)

110nm -> 28nm

2023-01-04，3rd Tapeout



28nm node，1.5M gates
(11-level pipeline with cache、IP:
UART、VGA、PS/2、SPI、SDRAM,
Two PLL on SoC，Support Linux)