TRISTAN

Together for **RIS**c-V **T**echnology and **A**pplicatio**N**s

Patrick Pype
Director Strategic Partnerships
NXP Semiconductors

RISC-V Summit Barcelona, June 7th, 2023

European Commission
KDT JU
Key Digital Technologies Joint Undertaking

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Agenda

- How it all started…
- The TRISTAN consortium and project
- How TRISTAN contributes to the EU Roadmap on RISC-V and Open-Source
- Why TRISTAN needs ISOLDE ?
- Conclusions

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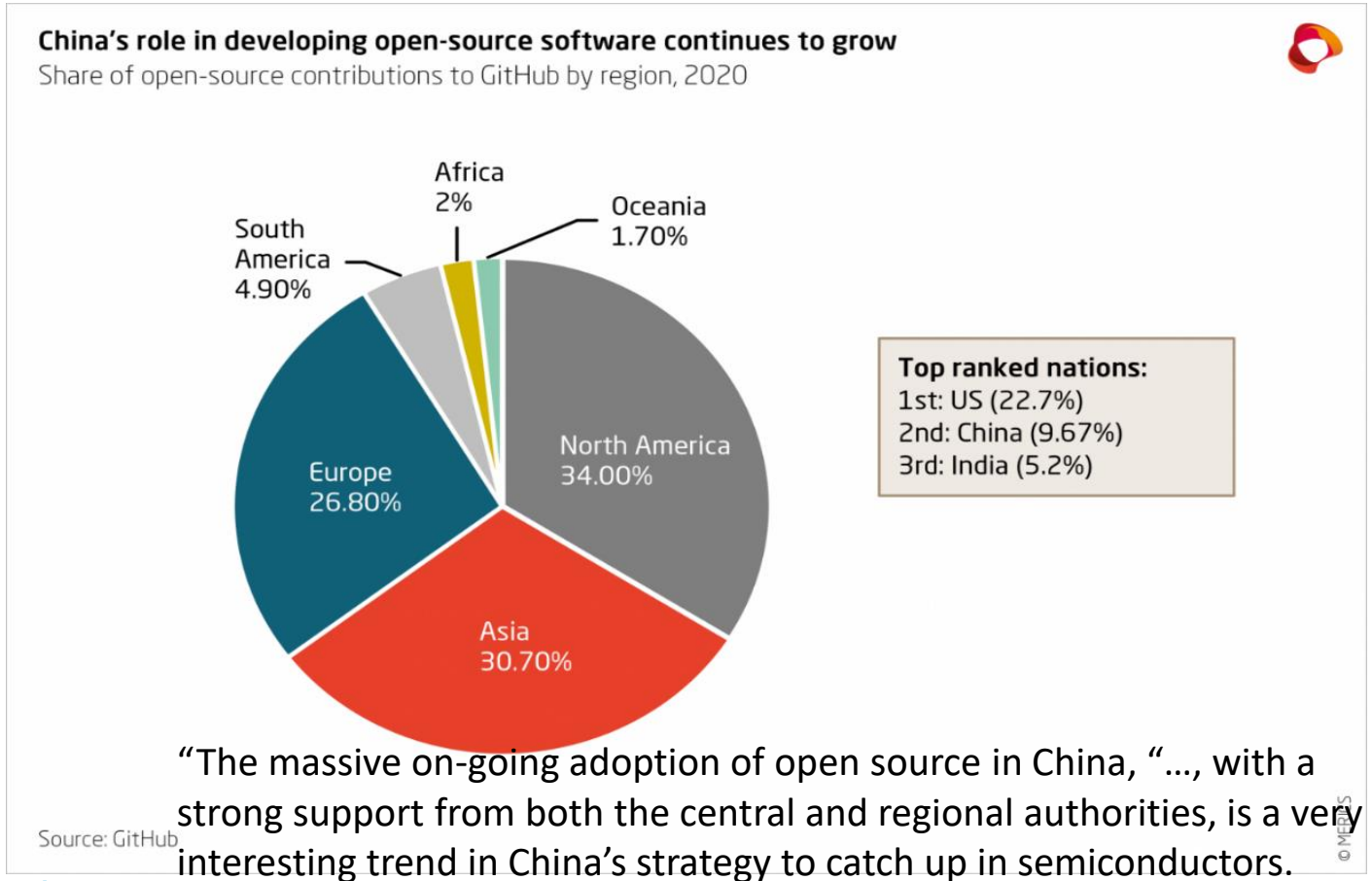
How it all started...
Europe to urgently catch up with China

HW ➡ "Alibaba introduced first RISC-V based product (XT910) in July 2020"
(Source : https://www.nextplatform.com/2020/08/21/alibaba-on-the-bleeding-edge-of-risc-v-with-xt910/)

SW ➡



"The massive on-going adoption of open source in China, "…, with a strong support from both the central and regional authorities, is a very interesting trend in China's strategy to catch up in semiconductors.

"For China, open source is an **industrial policy tool** and important part of its **push for technological autonomy**"

Source : https://merics.org/en/short-analysis/china-bets-open-source-technologies-boost-domestic-innovation

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How it all started…
Why RISC-V in Europe ?

STRENGTHS
- Easy access & low barrier for SoC design
- Ability to customize
- Accessible data for safety & security analysis (whitebox)
- Availability of SW ecosystem
- Lower export control restrictions
- Less vulnerable to geo-political risks
- Strong academic support ; educational use
- Steers Innovation

WEAKNESSES
- Not Industrial Quality IP yet (HW/SW)
- Long-term guaranteed support to industrial users not yet established
- Risk of maintenance
- Lack of some IP (e.g. interconnect)

OPPORTUNITIES
- Customization opportunities
- Sharing development costs
- Sharing support costs
- New licensing models
- Support to SME's
- New industrial leaders

THREATS
- Risk not to create enough critical mass in Europe
- US/China competitors are running fast, with large investments and acceptance by leading end-user companies

MAXIMISE

RESOLVE

Europe must develop the RISC-V supply chain to support autonomy in critical market sectors and reduce its dependency on US & China

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How it all started...

European WG to create Recommendations & Roadmap

Members of the Open Source HW/SW Working Group

Chair :

Patrick Pype	NXP Semiconductors

Participants :

Jan Andersson	Cobham Gaisler
Luca Benini	ETH Zürich / Univ. Bologna
Sven Beyer	Siemens
Holger Blasum	SYSGO GmbH
Sylvain Depierre	NanoXplore
Marc Duranton	CEA
Wolfgang Ecker	Infineon
Michael Gielda	Antmicro Ltd
Edwin Hakkennes	Technolution
Andreas Koch	Technische Universität Darmstadt
Loic Lietar	GreenWaves Technologies
Andreas Mauderer	Bosch
Jan-Hendrik Oetjens	Bosch
Jérôme Quévremont	Thales
John Round	NXP Semiconductors
Javier Serrano	CERN
Herbert Taucher	Siemens

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How it all started…

Defining a RISC-V Eco-System : IP to SoC Landscape

Base Building Blocks

- High-end RISC-V core
- Mid-end RISC-V core
- Low-end RISC-V core
- Other SoC IPs (interconnect, peripherals…)

RISC-V is a modular ISA:

- Basic
- Standard extensions
- Custom extensions

- Software (OS, tool chains, compilers, drivers, debuggers…)

Domain-specific features (safety, security, acceleration, AI…)

- Custom RISC-V extensions
- Co-processors / accelerators

Customized solutions for various markets

- Automotive
- Industrial
- Communication
- Data
- Other sectors

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TRISTAN Consortium

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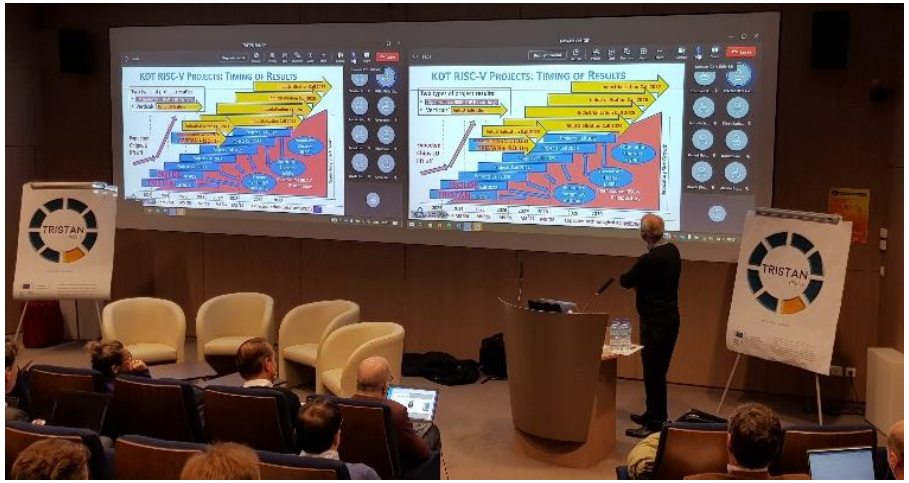
TRISTAN Kick-off Meeting

Caen, France, 11-12 January 2023



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Overarching Aim of TRISTAN
Aim of the WP

Expand
Mature
Industrialize

the European RISC-V ecosystem in order to compete with existing commercial/proprietary alternatives

How ?

- leveraging the Open-Source community to gain in productivity and quality
- defining a European strategy for RISC-V based designs including the creation of a repository of industrial quality building blocks to be used for SoC designs in different application domains (e.g. automotive, industrial, etc.)
- applying a holistic approach, covering both electronic design automation tools (EDA) and the full software stack
- exposing a large number of engineers to RISC-V technology, which will further strengthen adoption.

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TRISTAN Objectives & Expected Impact

Objectives	Expected Impact 3-5 years after project end
Processor Development	At least 4 industrial RISC-V based SoC design starts per year
Eco-system of Industrial Quality SoC Building Blocks	At least 2 Building Blocks used in 4 industrial design-ins
SoC Development Infrastructure	Availability of SW stacks, development & EDA-tools TRISTAN stack visible in at least 1 Open-Source project per year
Vendor Independence	At least 80% of TRISTAN HW IP's simulates and synthesizes with at least 2 different vendors and Open-Source tools
Active EU Open-Source HW Community	At least 5 new requests outside TRISTAN consortium making use of TRISTAN results in the OpenHW Core-V CVA6 repository At least 10 references of TRISTAN are found in design-ins
Demonstration of Building Block Interoperability	At least 2 examples of Building Blocks interworking visible in design-ins
Pre-Certification & Validation	Effort of certifying a product composed of TRISTAN items is reduced by 80%

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How Open-Source SW penetration can evolve towards an Open-Source mixed HW/SW eco-system

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TRISTAN's 3 levels of operation

in order to encourage rapid industry adoption of an increasingly rich RISC-V eco-system

DEVELOPMENT	VALIDATION	OUTREACH
Extend RISC-V processor designs with new capabilities for industrial adoption	Clarify alignment with, and differentiation from other IS families	Introduce new engineers to RISC-V
Created supporting IP-blocks to industrial quality level, with simple and transparent licensing	Demonstrate that RISC-V addresses real-world problems as well, if not better, than existing proprietary solutions	Create a productive binding between Les, SMEs and RTOs working on RISC-V across Europe
Reduce EU dependence on 'opaque IP' blocks which cannot be independently verified	Demonstrate that developed toolchains are capable of rendering structured and full ASIC design by real tape-outs	Improve the relationship between the Open-Source and Industrial Communities
Create and solidify robust EDA tooloing for microcontroller, SoC and CPU designs		Educate the industrial community in how to work constructively with Open-Source
Develop world class SW tooling to develop RISC-V applications		Encourage commercial organizations to become less fearfull of Open-Source
		Build a reference repository for RISC-V compliant IP-blocks

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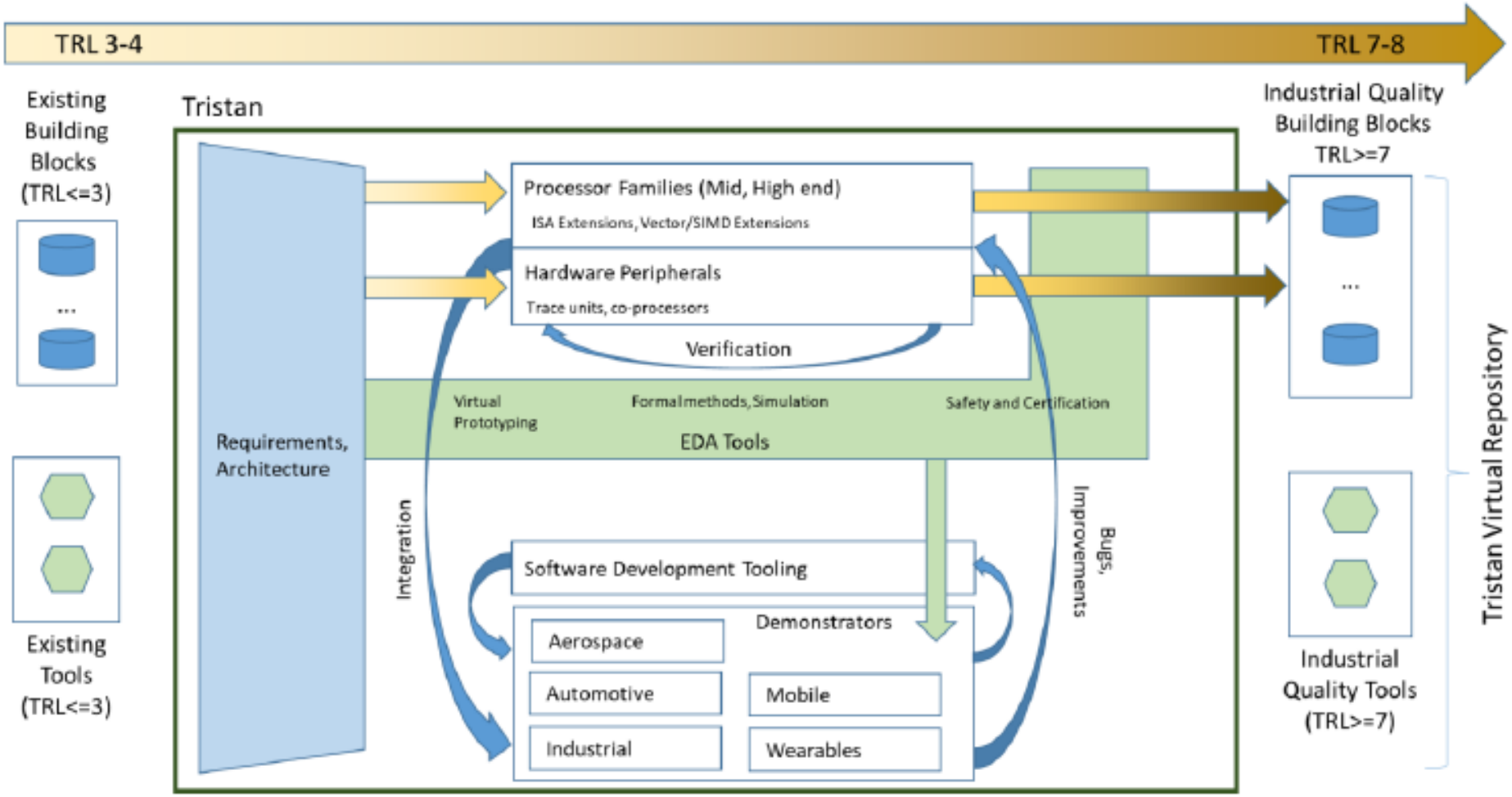
TRISTAN's Scientific Methodology



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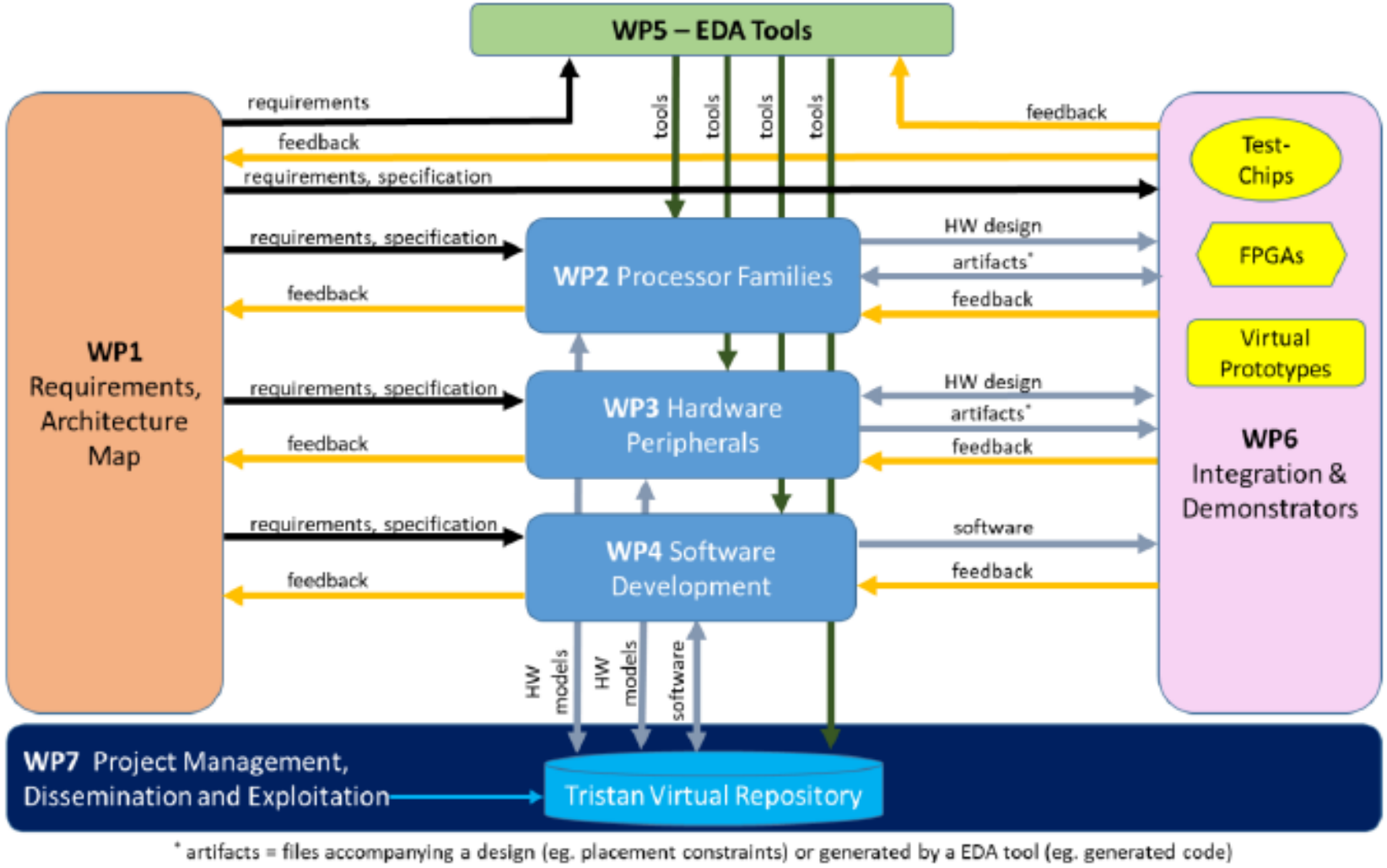
TRISTAN Implementaton Plan & WP Structure



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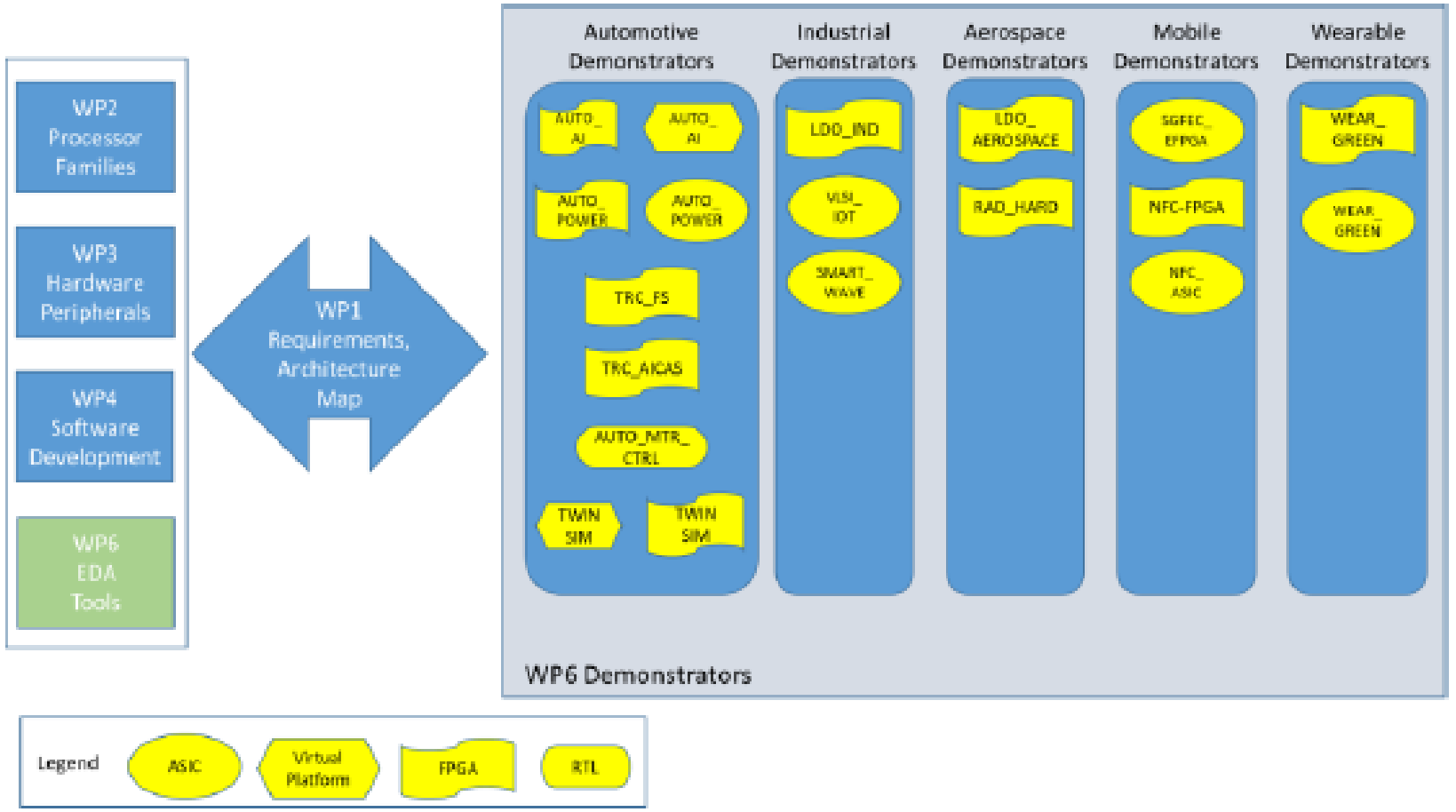
TRISTAN Building Blocks & Demonstrators



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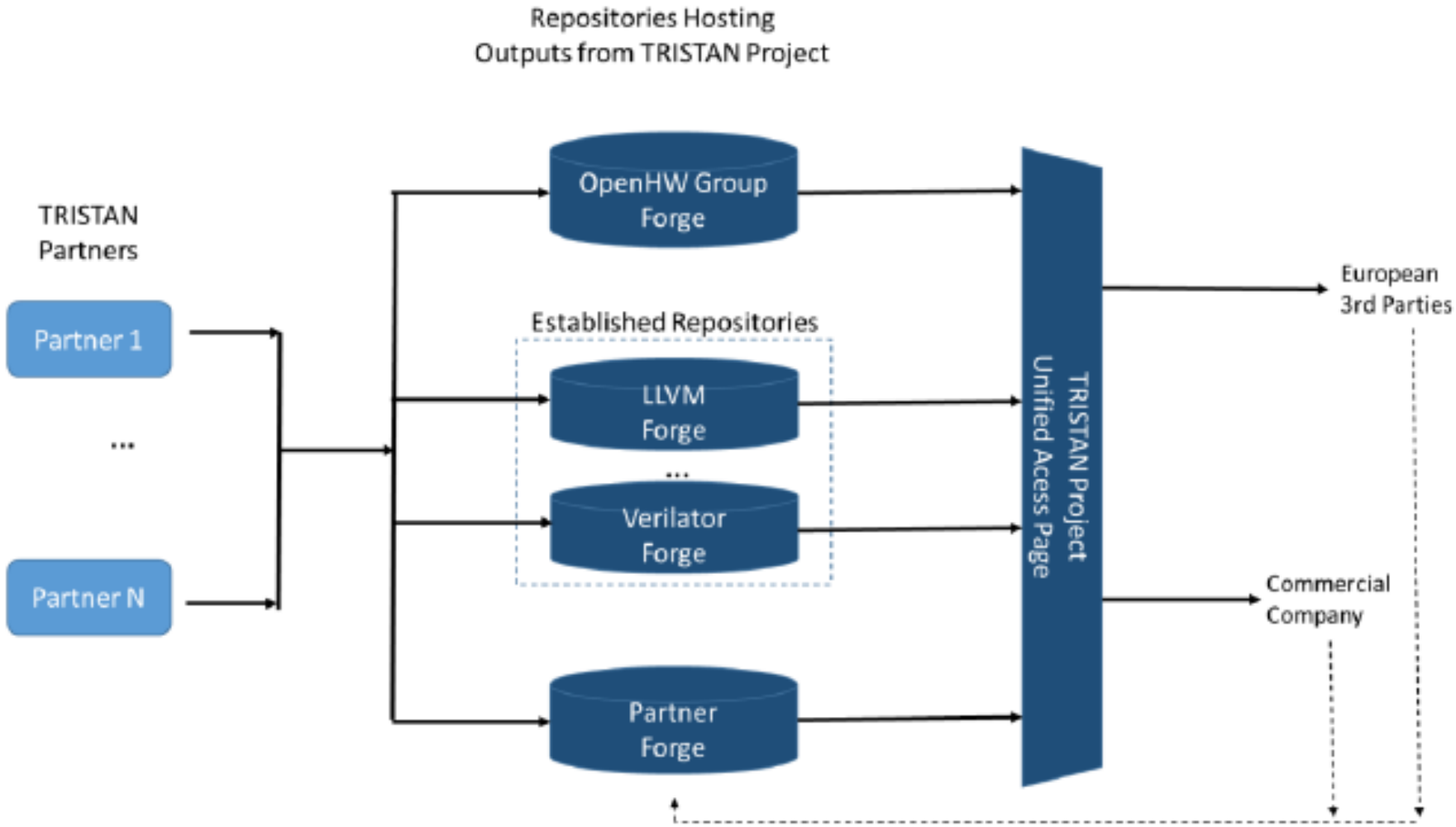
TRISTAN Virtual Repository

connecting to established Open-Source repositories



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How TRISTAN contributes to the EU Roadmap

RISC-V and Open-Source

Positioning of TRISTAN developments in EU RISC-V & Open-Source Roadmap
Roadmap Elements
Repository of RISC-V based Processor Platforms
Domain-Specific Processor Features
Repository of Open Source HW Peripheral Blocks
Interconnect for Real-Time and Mixed Criticality
Interconnect for System Integration
Domain-Specific Accelerators
Software
Methodology and EDA Tools
Domain-Specific Demonstrators

Short Term 2-5 years	Mid-Term 5-10 years	Long Term > 10 years

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Extract from TRISTAN positioning on EU Roadmap

Positioning of TRISTAN developments in EU RISC-V & Open-Source Roadmap		
Roadmap Elements	***TRISTAN IP Developments***	***Comments***
Repository of RISC-V based Processor Platforms		
High-end: Highly customizable Multi-core Out of Order 64-bit open source infrastructure with the associated memory hierarchies (caches&coherency, off-chip) and communication (fast cores to cores, cores to accelerators, cores/accelerators to system). This should be suitable for various instances of processor IP.	I:Data-cache-WI3.1.5	Optimised Caches feature flexible strategies, multi-requestors, writeback control, support for error correction and performance stats etc. Applied to CVA6
Highly customizable high-end domain-specific cores for high-performance embedded system and/or general-purpose application (link with EuroHPC-call on HPC processors)	C:CVA6-W2.4.1, WI2.4.2, WI2.4.3, WI2.5.3, WI5.2.2 I:Data-Cache WI3.1.5 : L1D$ optimized for high-performance applications	These are extendable CPUs, and uncore that are or will be open-source industrial-grade verified IPs for building RISC-V SoCs for application-class systems. CVA6 is a 6-stage, single issue, in-order CPU which implements the 64-bit RISC-V instruction set. It fully implements I, M, A and C extensions Hypervisor support for the application core RVV co-processor with support for low precision integer arithmetic and multi-precision floating point operations. Coprocessor interface based on CX-X-IF supporting memory access through cva6 internal load and store unit. design a superscalar and multi-issue architecture cva6 evolution to increase performance.
Domain-Specific Processor Features		
Provide public artifacts for safety and security by architecture at an initial assurance level	I: Value-boundary-checking I:Side-channel-WI2.1.1 I: Lockstep/Ext Mem Security/ECC WI3.3.3 WI.2.1.3 definition of architectural features for safety to reach the highest ASIL levels as defined in the ISO26262 norm	Support for timing channel protection: ETH

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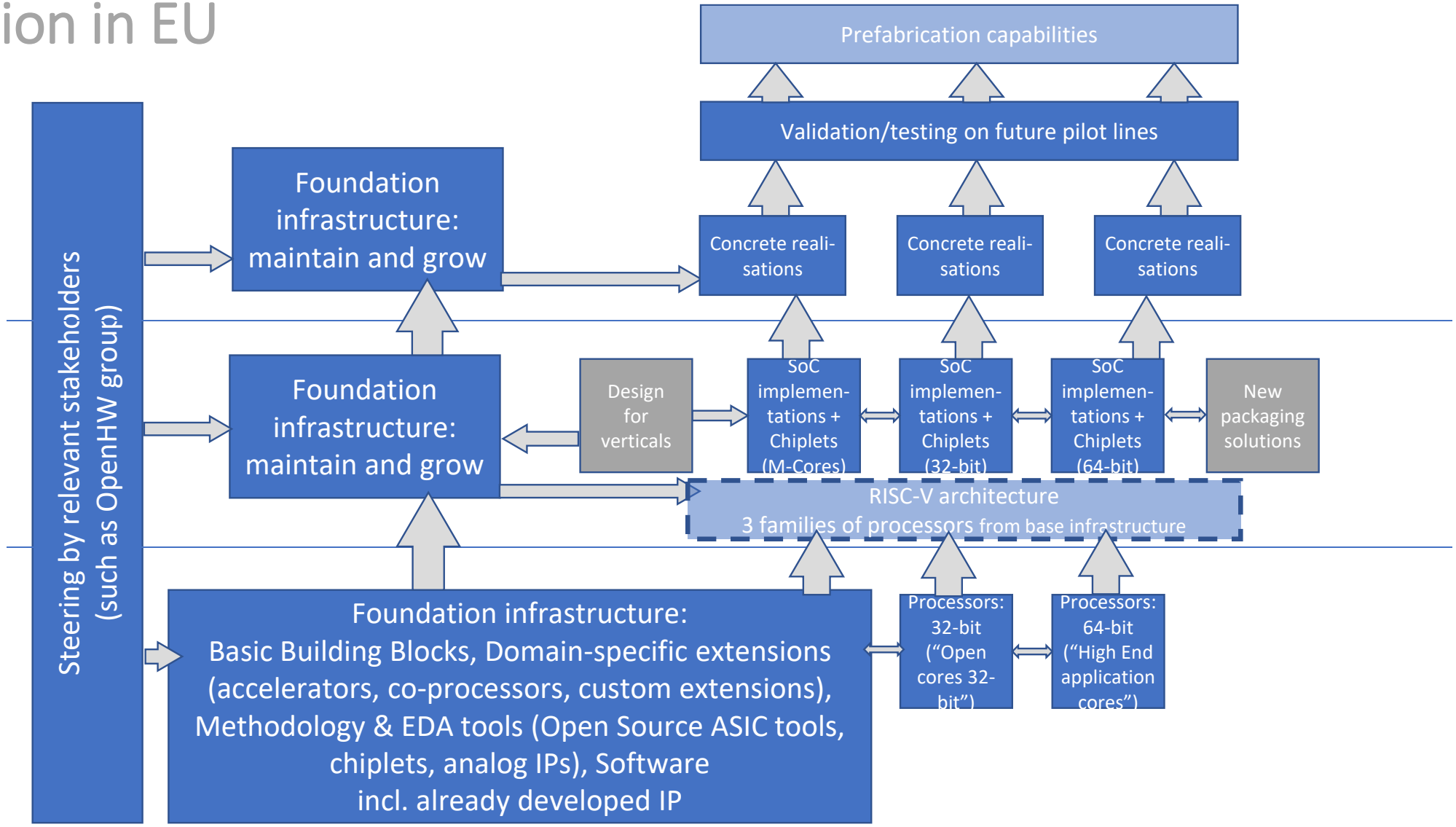
How TRISTAN contributes to the EU Roadmap

Vision in EU



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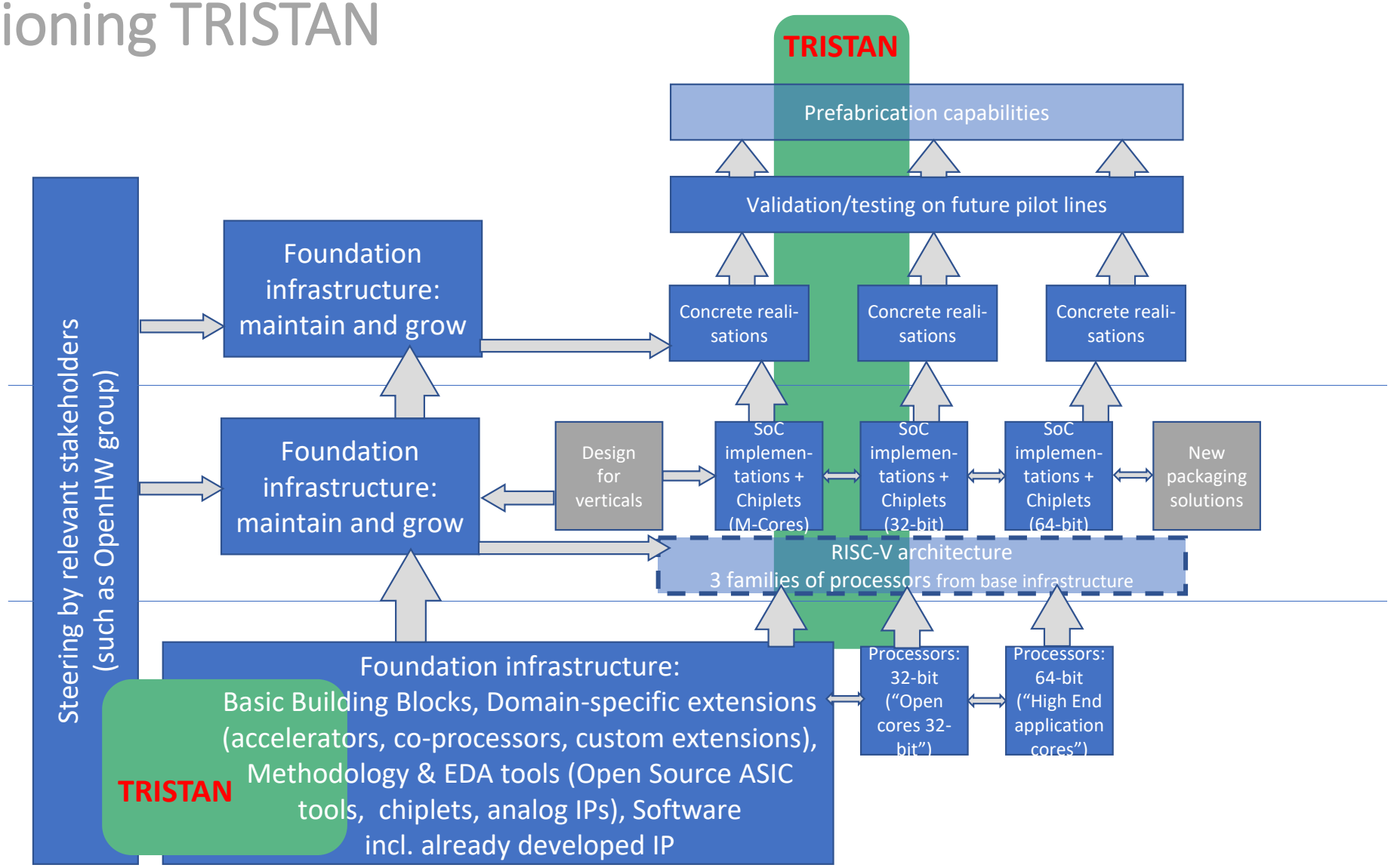
How TRISTAN contributes to the EU Roadmap

Positioning TRISTAN



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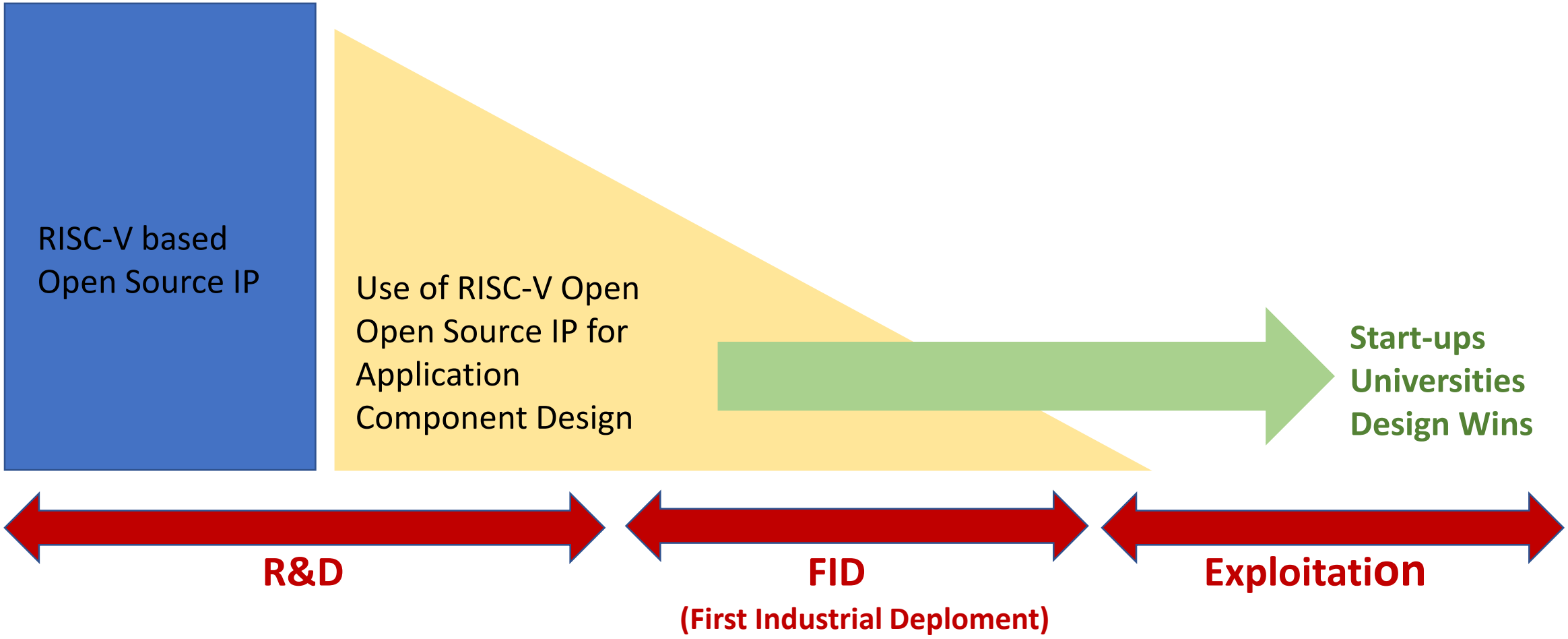
Approach to European Success Story

From Niche to Certified Mass Deployment



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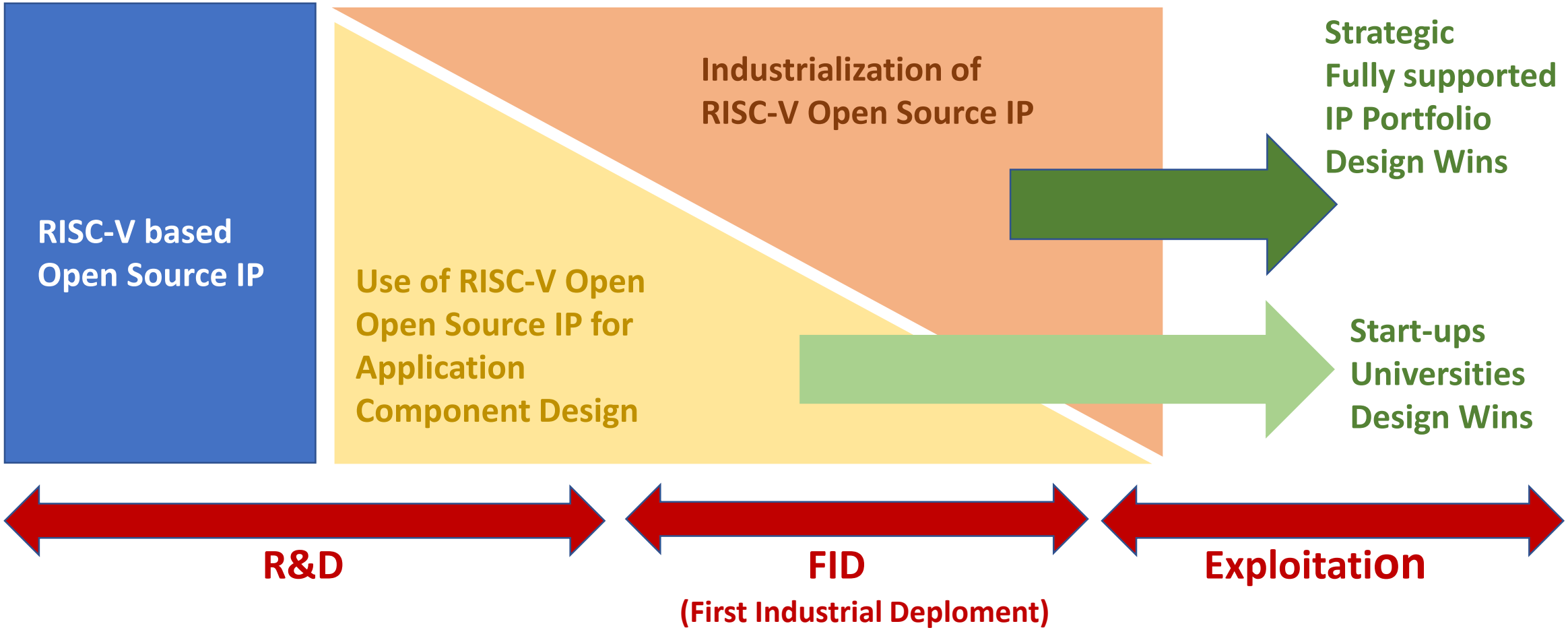

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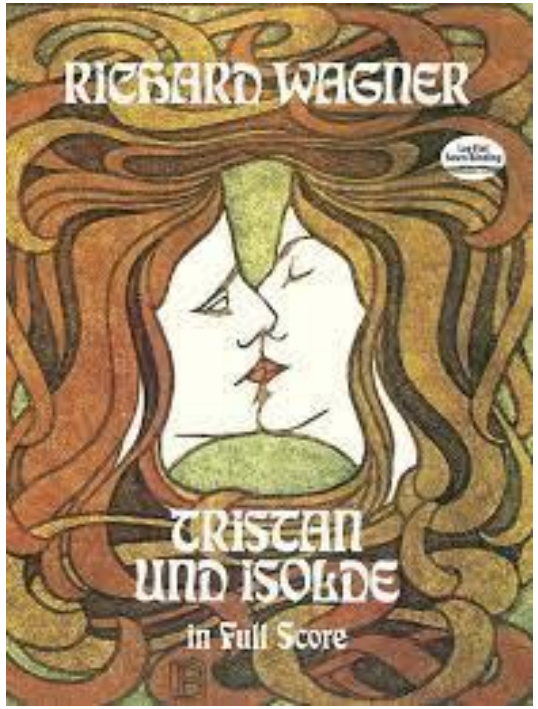
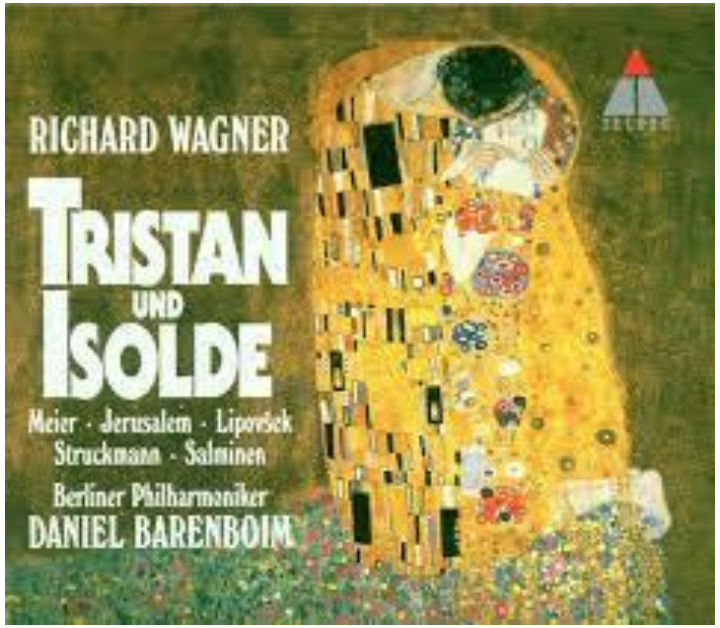
Why TRISTAN needs ISOLDE ?

Move into another dimension…





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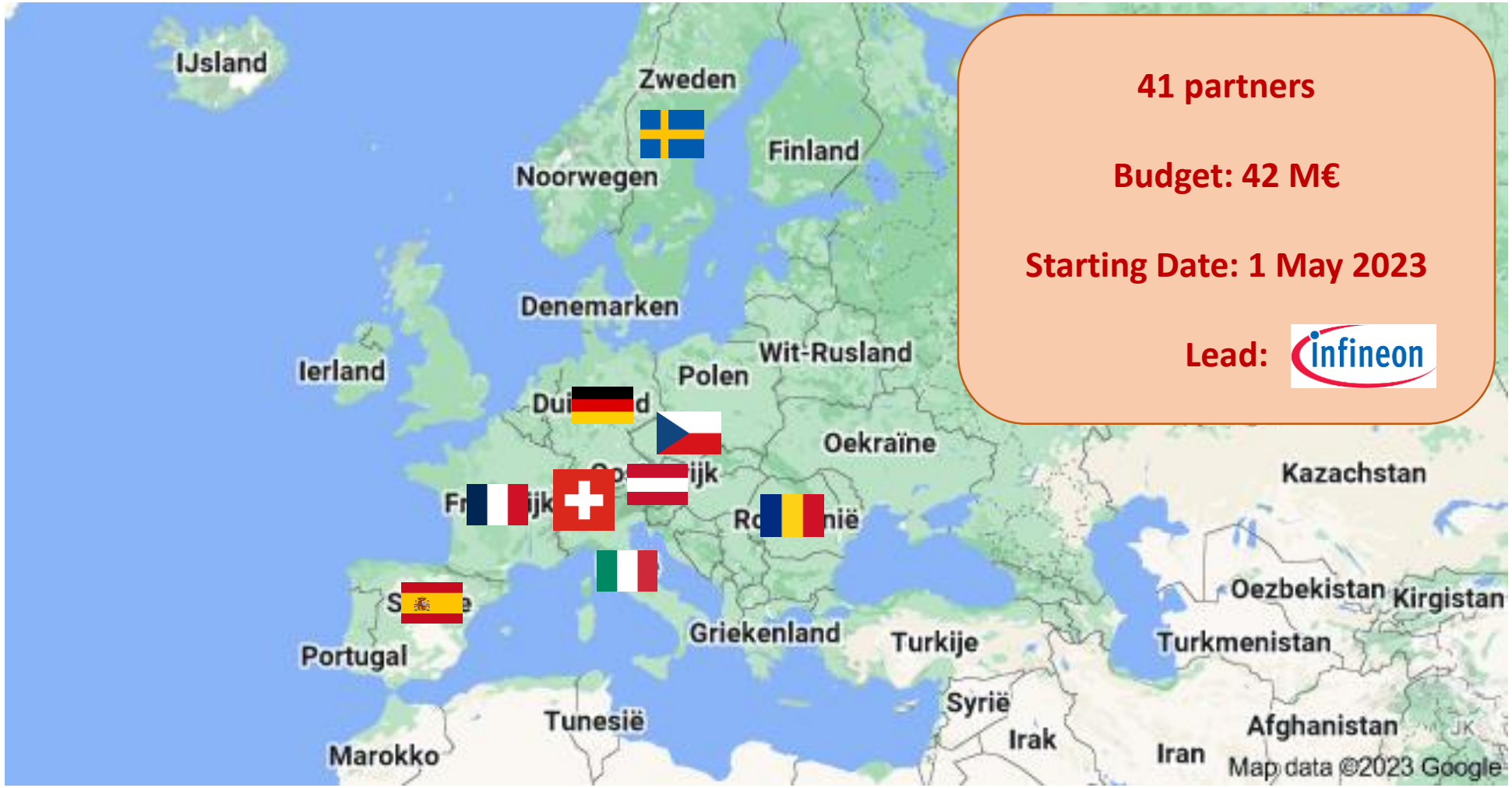
ISOLDE Consortium



41 partners

Budget: 42 M€

Starting Date: 1 May 2023

Lead: Infineon

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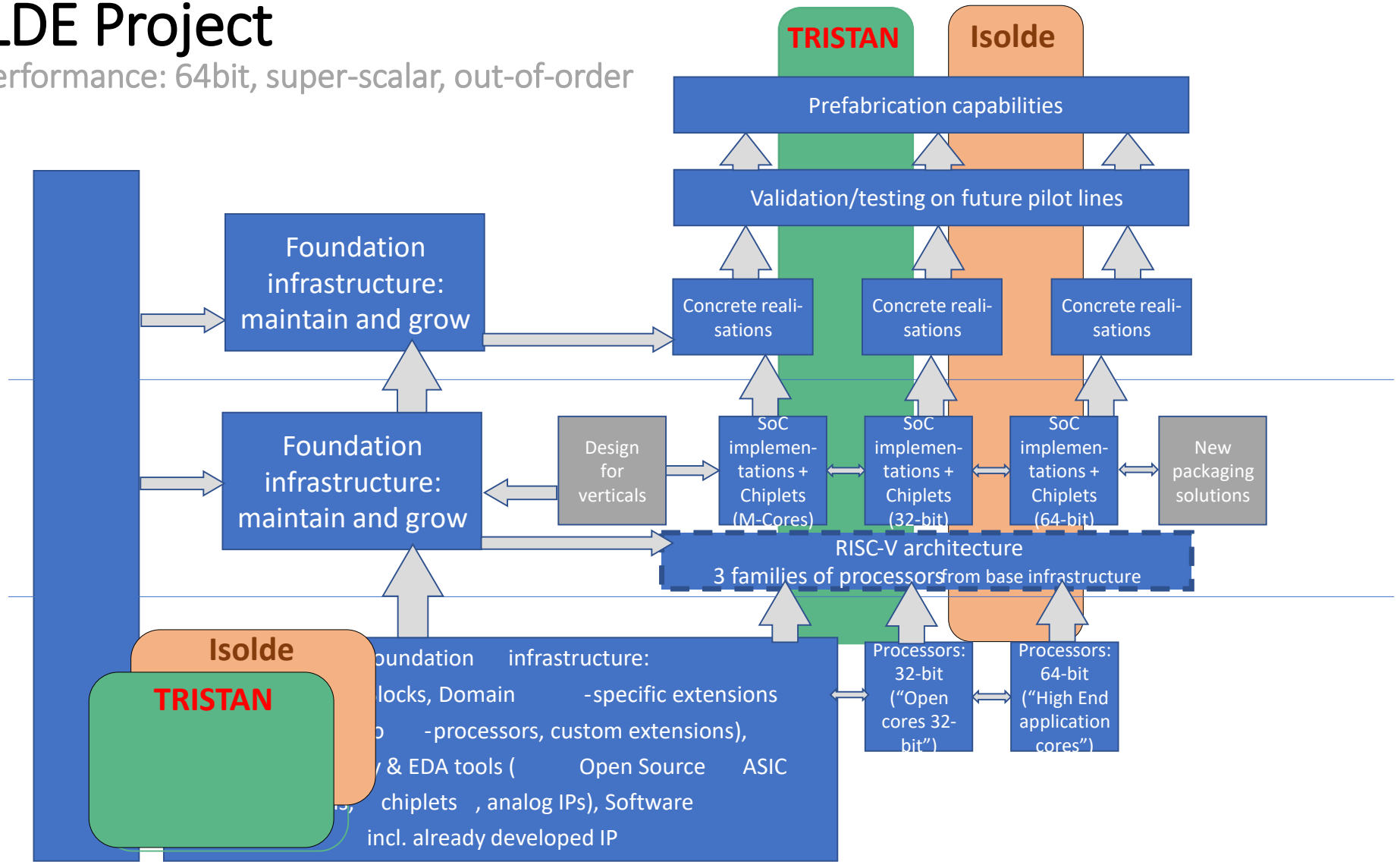
ISOLDE Project

High Performance: 64bit, super-scalar, out-of-order



European Commission

KDT JU
Key Digital Technologies Joint Undertaking

TRISTAN has received funding from the Key Digital Technologies Joint Undertaking (KDT JU) under grant agreement nr. 101095947. The KDT JU receives support from the European Union's Horizon Europe's research and innovation programme and Austria, Belgium, Bulgaria, Croatia, Cyprus, Czechia, Germany, Denmark, Estonia, Greece, Spain, Finland, France, Hungary, Ireland, Israel, Iceland, Italy, Lithuania, Luxembourg, Latvia, Malta, Netherlands, Norway, Poland, Portugal, Romania, Sweden, Slovenia, Slovakia, Turkey

TRISTAN and ISOLDE Project

Synergise, Complement and Build a strong European Network

Item	Tristan	Isolde	Comment
Processor Development	• Decent Performance • CVA6 and Pulp	• High Performance • CVA6, Noel-V	• To be proven in real designs • Isolde strives for super scalar, out of order, 64 bit
Building Blocks for SoC/High Perf, Computing	• SoC Buidling Blocks	• High performance and/or low power accelerators	• In both cases (documentation, RTL, test-bench, drivers, other design artifacts • Industry quality
SoC Development Infrastructure	• Focus on standard peripherals	• Focus on High performance accelerators	• Software stack (e.g., OS, libraries, middleware, and applications) • Software development tools (e.g., compilers, linkers, debuggers) • SoC construction tools (e.g., machine-readable IP block descriptions, automated SoC composition and optimization)
Vendor Indepence	• Validate with different colaterals		• Avoid locking of HW-IP and SW-stack/tools to specific vendor

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TRISTAN and ISOLDE Project

Synergise, Complement and Build a strong European Network

Item	Tristan	Isolde	Comment
Safety/Security		• Especially multi-core • Preparation of certification	• Features enabling Safety and/or Security Certification for high-performance RISC-V Computing
Research		• High Performance Computing research	• ISOLDES‘s focus is high performance compute, TRISTAN‘s focus is SoC building
Open Source (OS)	• Active European OS Hardware Community	• High Quality OS Hardware and Software IP	• Both strive for deliverables given to open source
Demonstration of Building Block Interoperability	• Mainly models and FPGAs • Interoperability between a high number of IPs	• Mainly FPGAs and ASICs • Make OS IPs de factor standard • Focus: Cores and Accelerators	• ASICs and FPGAs are targeted in both projects. Isolde strives for more ASIC demonstrators

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TRISTAN and ISOLDE Consortium

Synergise, Complement and Build a strong European Network

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Agenda

- How it all started…
- The TRISTAN consortium and project
- How TRISTAN contributes to the EU Roadmap on RISC-V and Open-Source
- Why TRISTAN needs ISOLDE ?
- Conclusions

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Conclusion

- TRISTAN & ISOLDE are starting points for creating a **European Eco-System of RISC-V and Open-Source**
- Within 5 years RISC-V CPU's are at no functional disadvantage to establish **competitive & competing architectures**
- TRISTAN & ISOLDE will form the impetus to create low-, mid- and high-end platforms for different **strategic application domains** in Europe...

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The Future : Automotive Platforms based on RISC-V

Delivering on EU strategies in the automotive sector

Aeneas

EPoSS European Technology Platform on Smart Systems Integration

Inside Industry Association

Automotive HW platform (open-source)

EU CHIPS ACT

Open SW-defined vehicle platform (CarOS + Middleware)

Reinforce EU position in strategic market of high-performance central automotive processors

Leverage RISC-V developments to reduce dependencies on non-EU technologies & suppliers

Reduce costs and complexity by working together on non-differentiating features

Ensure level playing field for automotive HW and data-driven cloud-edge applications

NEW INDUSTRIAL STRATEGY

RESEARCH AND INNOVATION POLICY

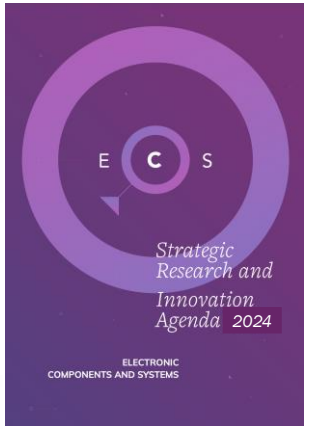
Horizon Europe

DATA STRATEGY

EUROPEAN GREEN DEAL

Fit for 55

European Commission



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From First Idea on TRISTAN to a Europen Success Story...

Two members of the consortium (Davide Schiavone – OpenHW Group & Adrian Evans – CEA) are giving a TRISTAN workshop on Friday morning :
Open-Source Hardware Basic Training : https://riscv-europe.org/side-events.html

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