



# The European Chips Act

## *Enabling Chip Design in Europe*

RISC-V Summit Europe

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# The European Chips Act

# The EU Chips Act - rationale for intervention



# Why this time it's different...

## Before



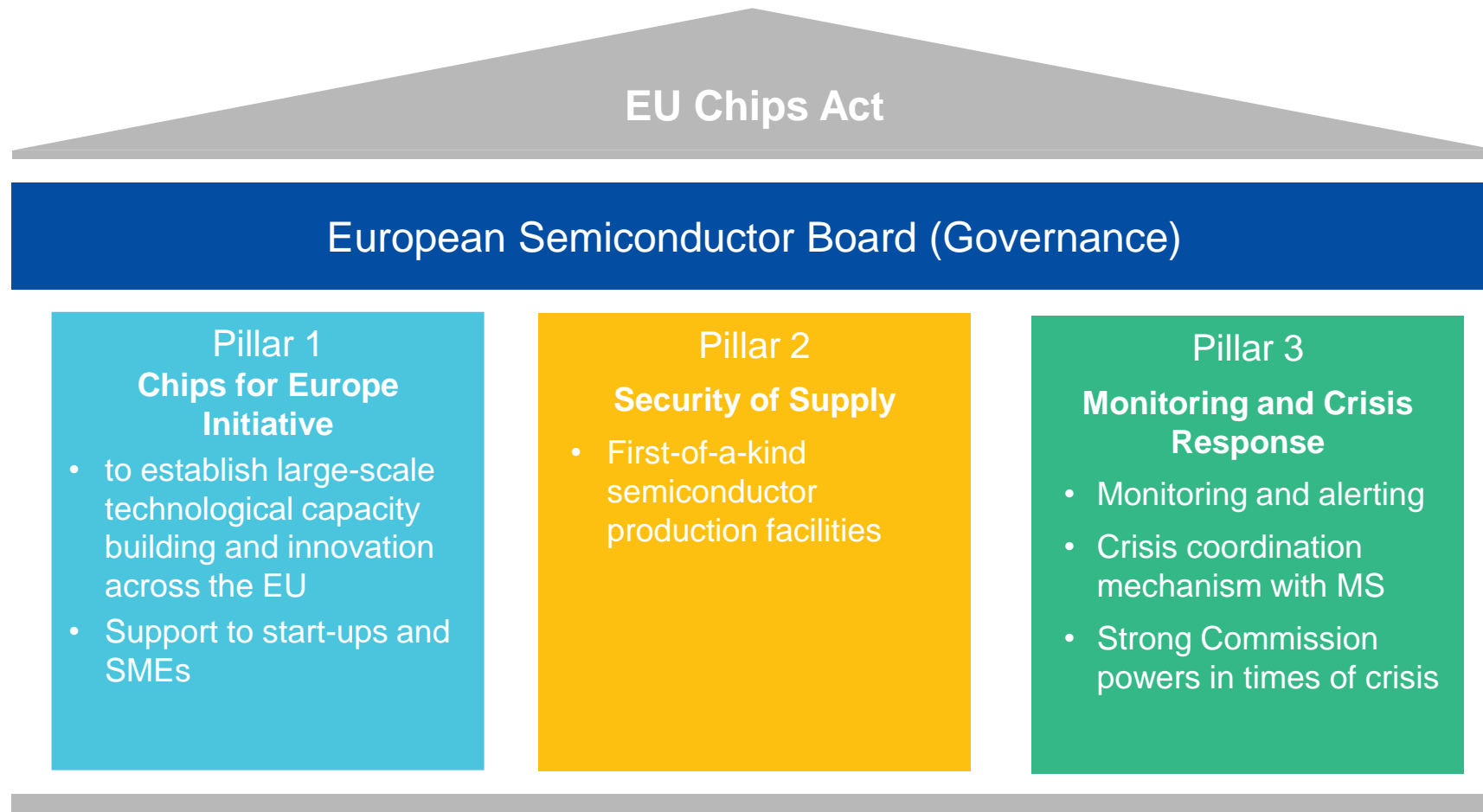
- Focus primarily on R&D
- Below critical mass investment
- Dispersed policy initiatives amongst Member States with no common policy framework
- Limited common European infrastructure

## Post-Chips Act

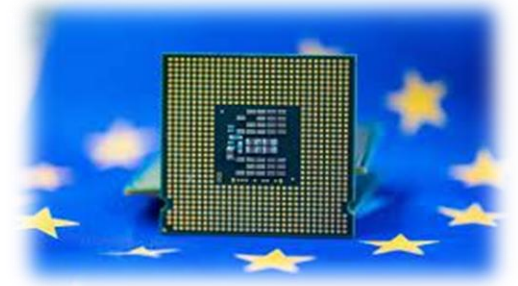


- R&D support with a focus on industrialisation and capacity building
- Reinforced public investment
- A synchronised pan-European approach that allows for complementarity across the Union
- A clear industrial policy for semiconductors that builds on strengths and ventures into new domains

# Three pillars of the Chips Act



# Chips for Europe Initiative



## Problem statement

- The EU's research programmes have largely not driven the conversion of its **excellent research results into industrial innovation**.
- SMEs and start-ups have difficulty **attracting the necessary investment**
- The EU has a limited pool of talent and lacks a workforce with the necessary **skills**.



Measures to help **bridge the gap to market** are required

# Chips for Europe Initiative

Aim: bridging the gap from lab to fab

## 5 Objectives

- 1 Reinforce design capacity by providing a **virtual design platform**
- 2 Enhance existing and developing new **pilot lines**
- 3 Accelerate the development of **quantum chips**
- 4 Expand **skills** and set up a network of **competence centres**
- 5 Facilitate SME access to **equity and loans** through a dedicated **Chips Fund**

Chips JU

EIC  
I-EU

Basic  
Research

Applied  
Research

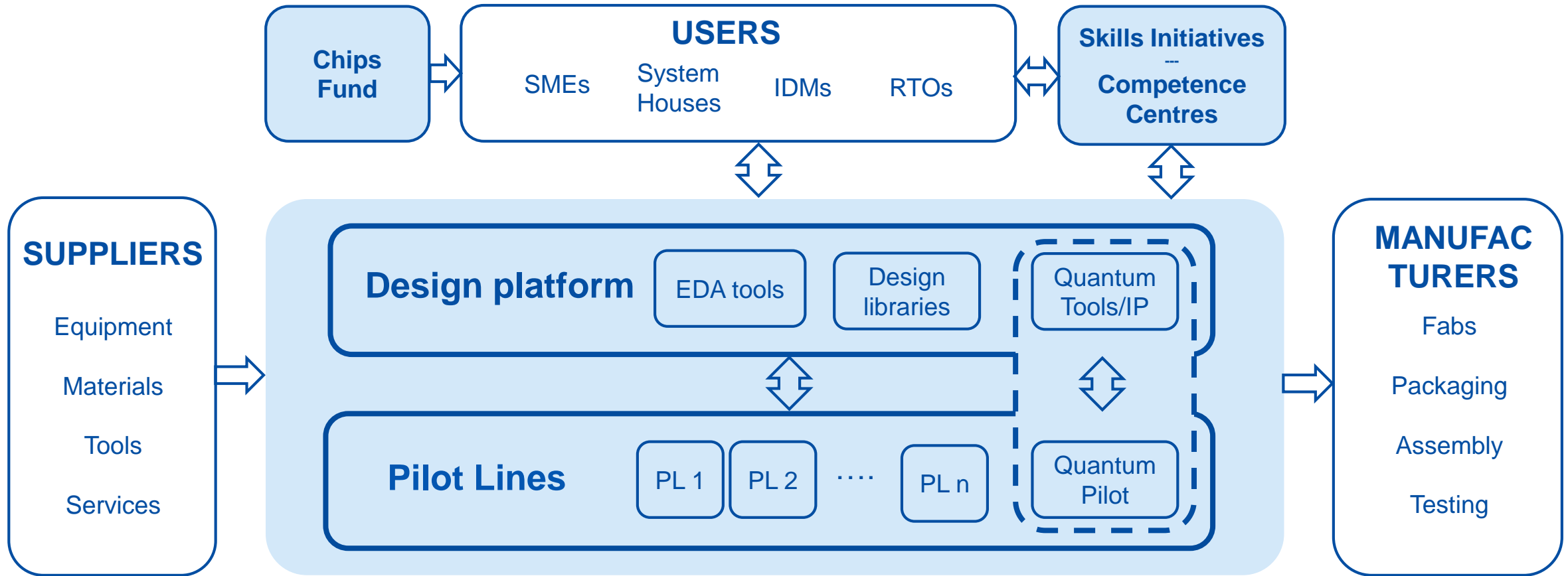
Prototyping

Pilot lines

Production

# Chips for Europe Initiative

## Bridging the gap from lab to fab



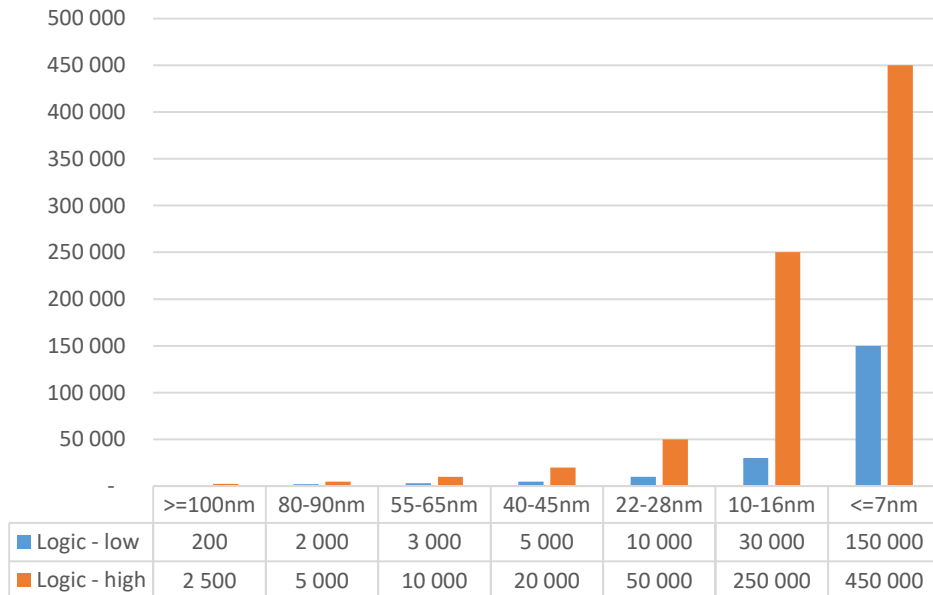


# Design Platform

# Design costs for fabless companies

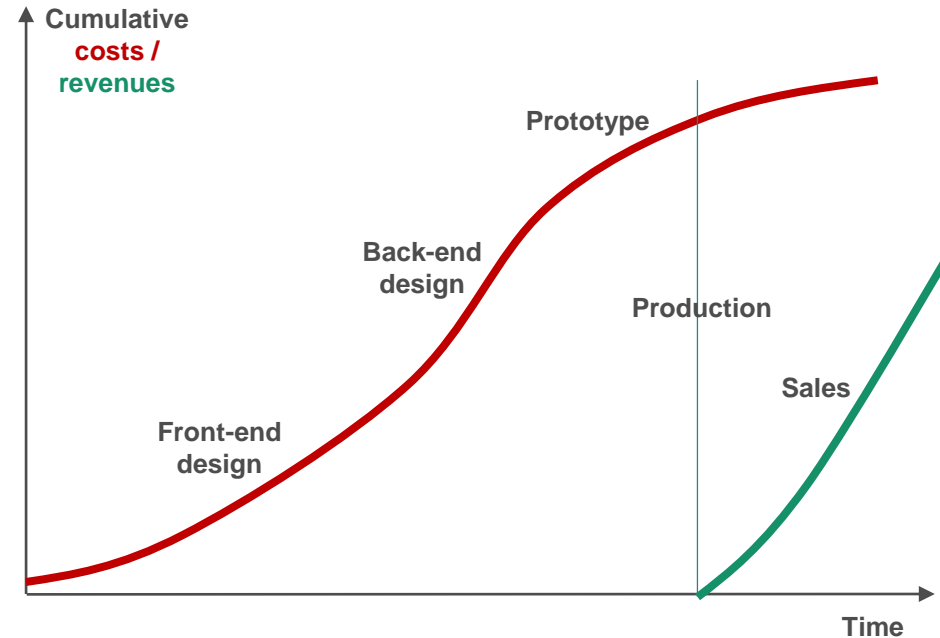
- Chip design is expensive, and soaring in advanced **digital ICs**
- High upfront costs, over 1/3 is not related to development (licensing, prototyping, IT)

## Cost of logic chip design



For low and high complexity digital IC designs

Source McKinsey 2022



Fabless start-ups must face high costs before getting any revenues



# Design platform - scope

## Ambition

Foster the development of the semiconductor **design ecosystem** in EU, reinforcing capacity to innovate and create European IP through IC design

## Main scope

- **Reduce entry barriers** and **admin burden** for EU companies engaging in chip design
- **Facilitate access** to pilot lines and foundries
- Foster **collaboration** among EU stakeholders, also on new IP and tools (incl. open-source, quantum)
- **Access** to network of **competence centres** offering **training** and support to boost design skills



## Instrument



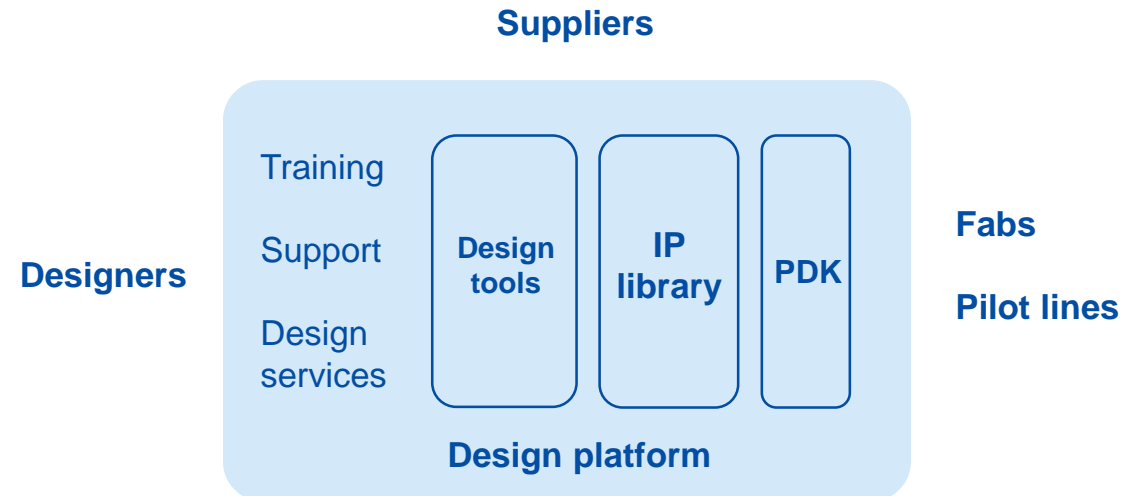
Develop a **virtual design platform**, offering **cloud-based** access to tools, libraries and support services to accelerate development and reduce time-to-market

# Design platform

## Added value



- Easy access to tools & IP on the **cloud**:
  - No upfront CapEx for on-premise IT **infrastructure**
  - Maximum computing **scalability** for simulation and verification
  - High level of **security**, fully audited
- **Streamlined process** with framework agreements
- Access to virtual **prototyping**, **MPW** and foundry services
- **Competence centers** offering training and support



# Design Platform Working Group

## DP Working Group



Includes key stakeholders: **EDA** tools & **IP** vendors, **RTOs**, **IDMs**, **design** houses, system houses  
12 meetings held, including workshop on cloud

### Goal:

- discuss services, architecture, implementation;
- report with recommendations and roadmap, as basis for specifications by technical experts

**Ansys**



**arm**

**cādence**



**DILPHIN**  
DESIGN



**imec**



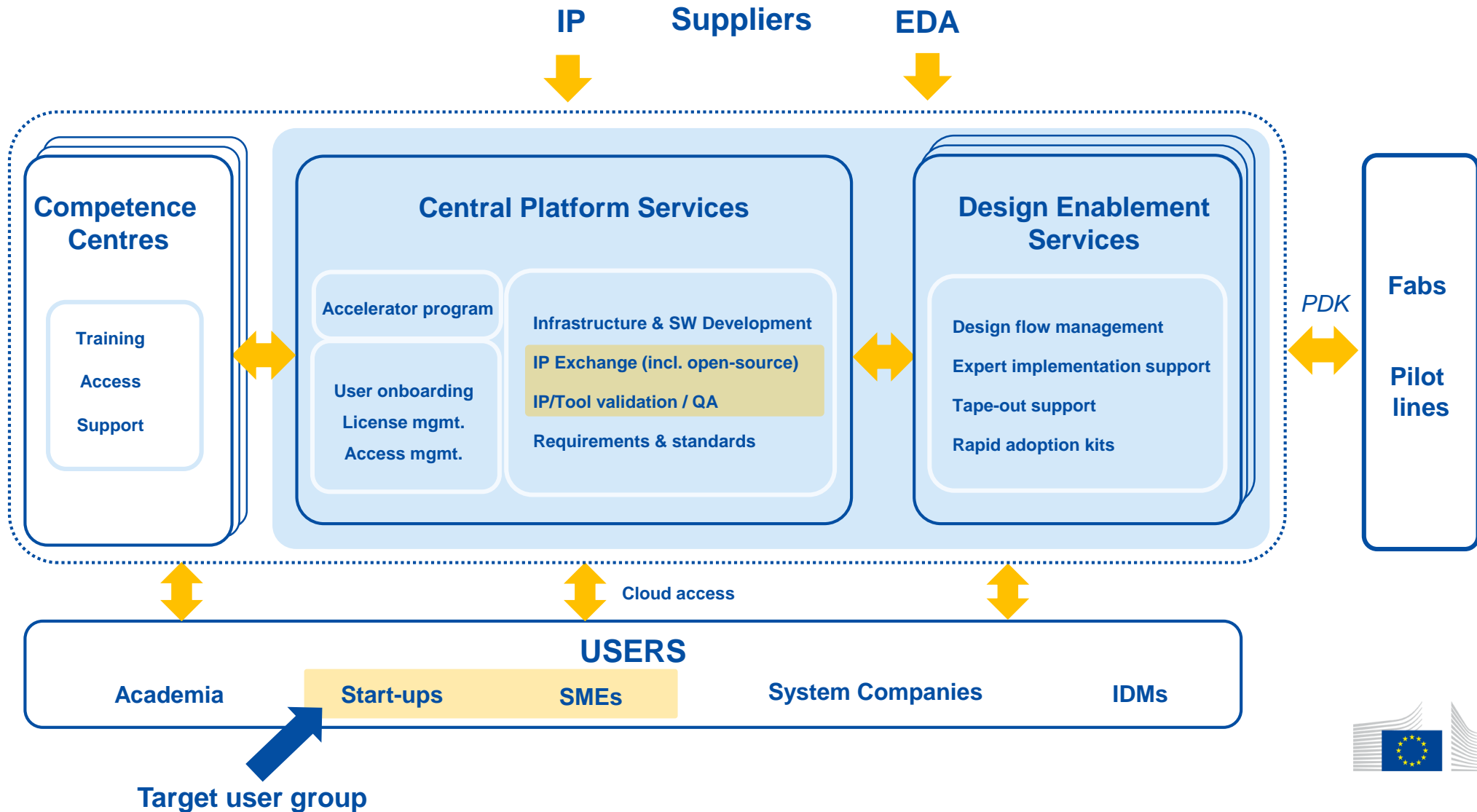
**SIEMENS**



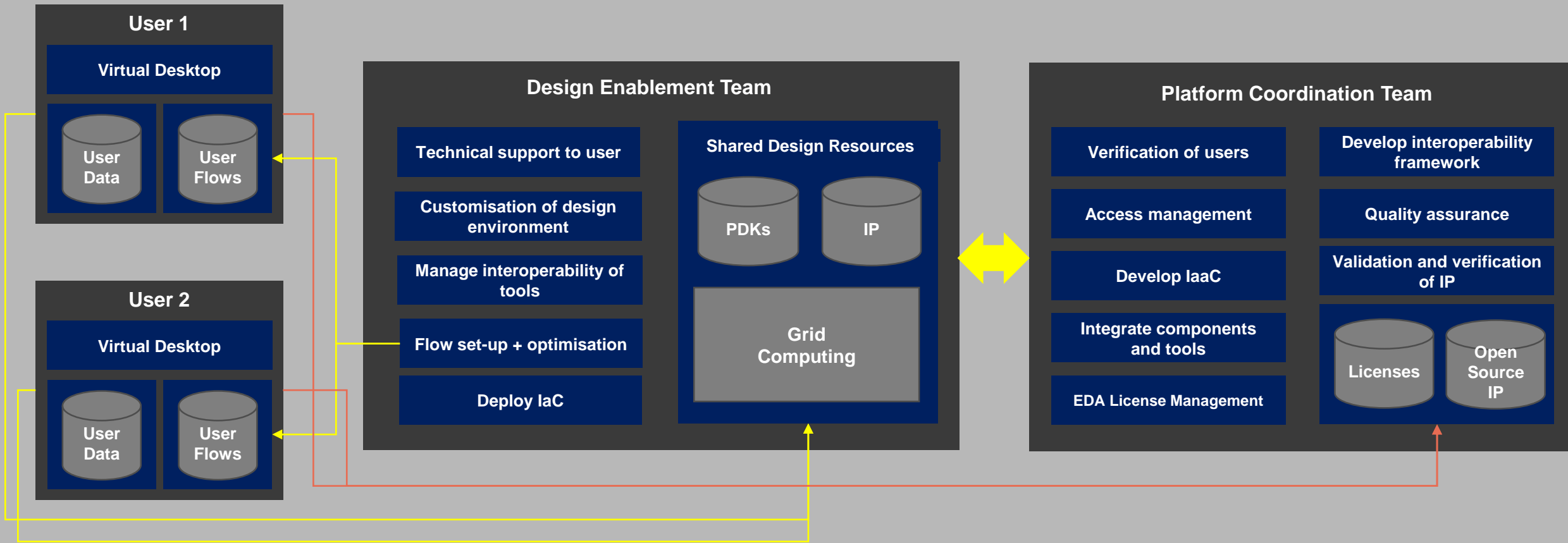
**SYNOPSYS**

# Design platform

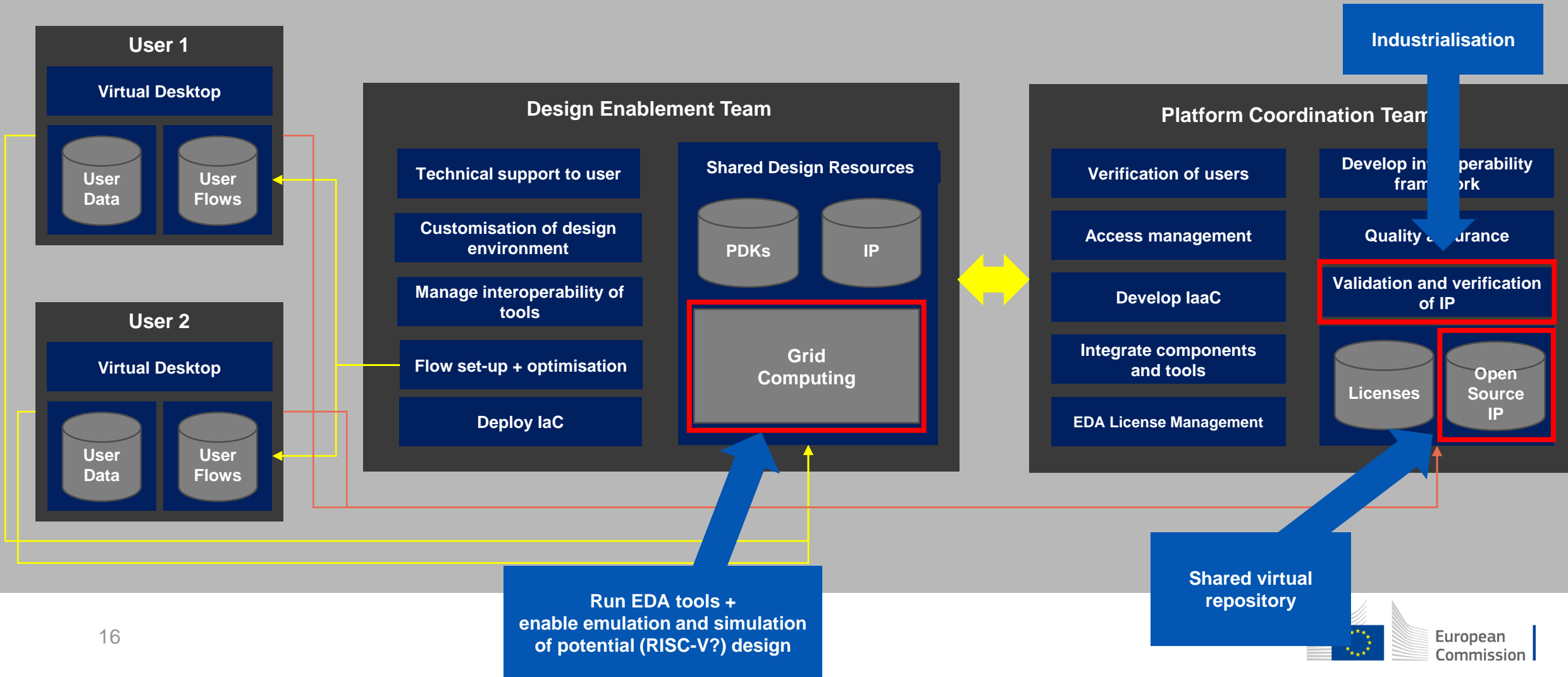
## Working Group Proposal



# Design Platform Proposal – zooming in



# Open Source Hardware in the Design Platform



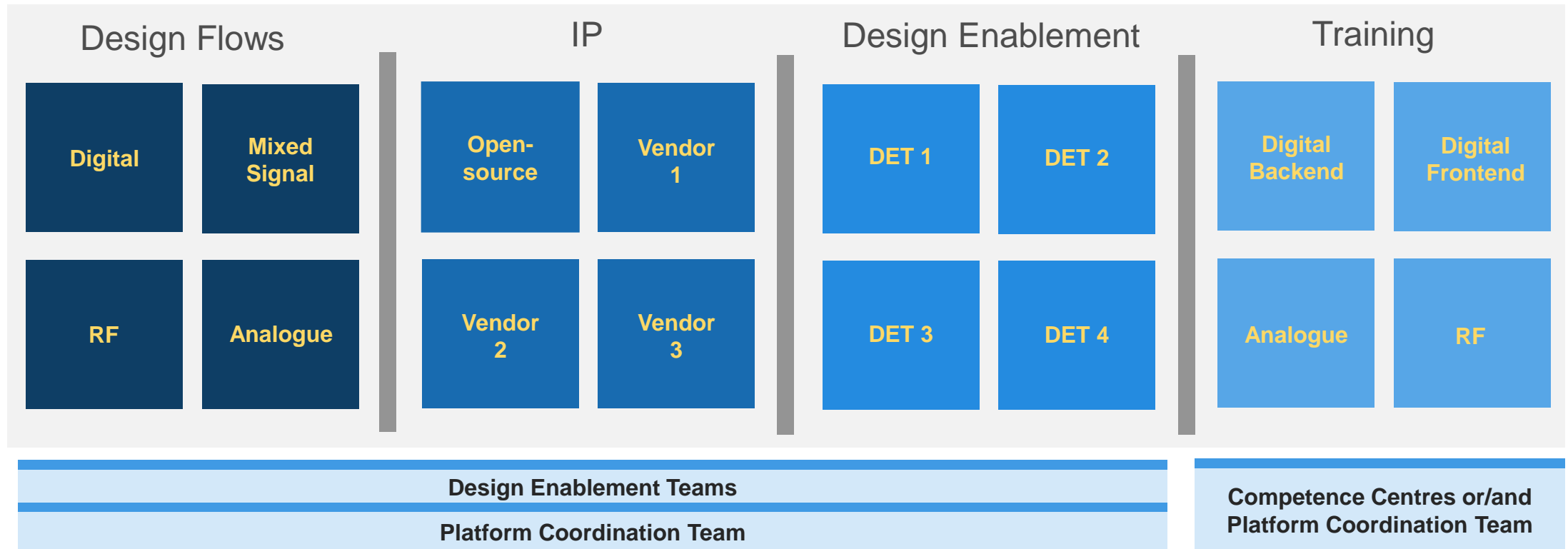


# Supporting SMEs at pre-competitive stages



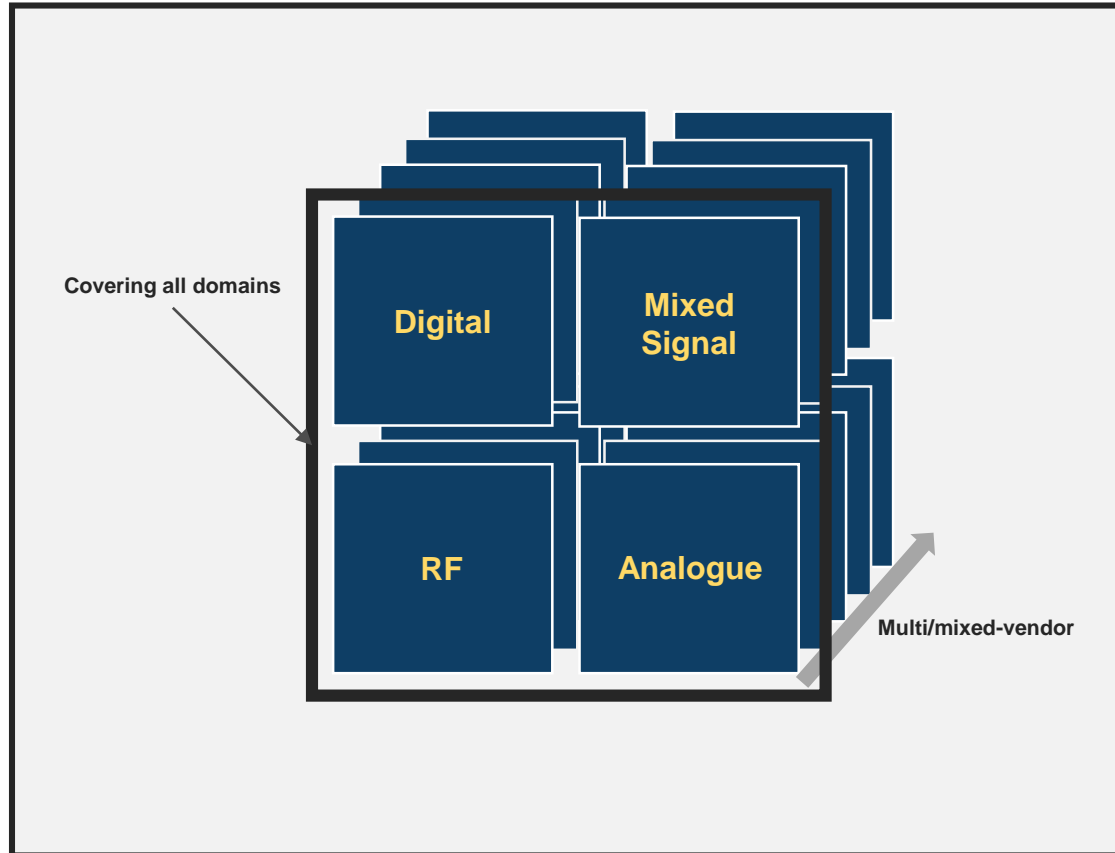
- The platform will offer all SMEs:
  - easy click-through licensing, reducing contract negotiations time
  - scalable computing resources through cloud access
  - easy access to training, expert support, tools, vast IP repository
- ***Accelerator programme:***
  - through Chips JU competitive calls, SMEs with innovative, advanced designs in pre-competitive stages of development can be selected
  - the chosen projects can get ‘vouchers’ for tool/IP licensing, valid up to prototype implementation (*proof of concept*) – thereafter commercial license agreement
  - Member States can allocate budget to support SMEs under the programme

# Enabling users through choice



*Tiles and options are only examples – eventual implementation may include a different number and type of resources.*

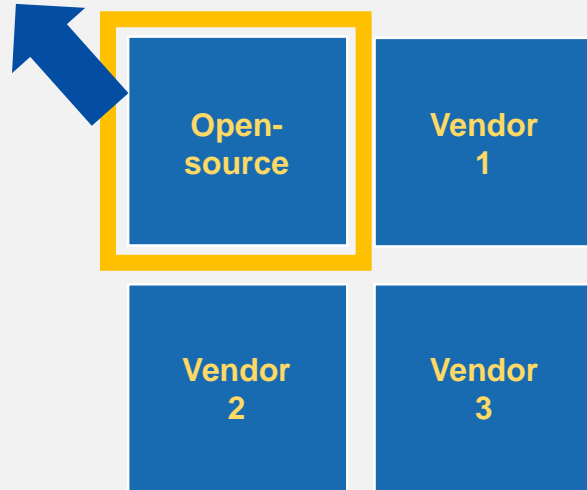
# Design Flows



- Standard and supported, developed by PCT and DETs in sync with EDA vendors.
- To accelerate the design flow selection process for users, the Design Platform will provide a **neutral view on available design flows**, with their supported features and service levels.
- Multi/mixed-vendor and covering all domains.

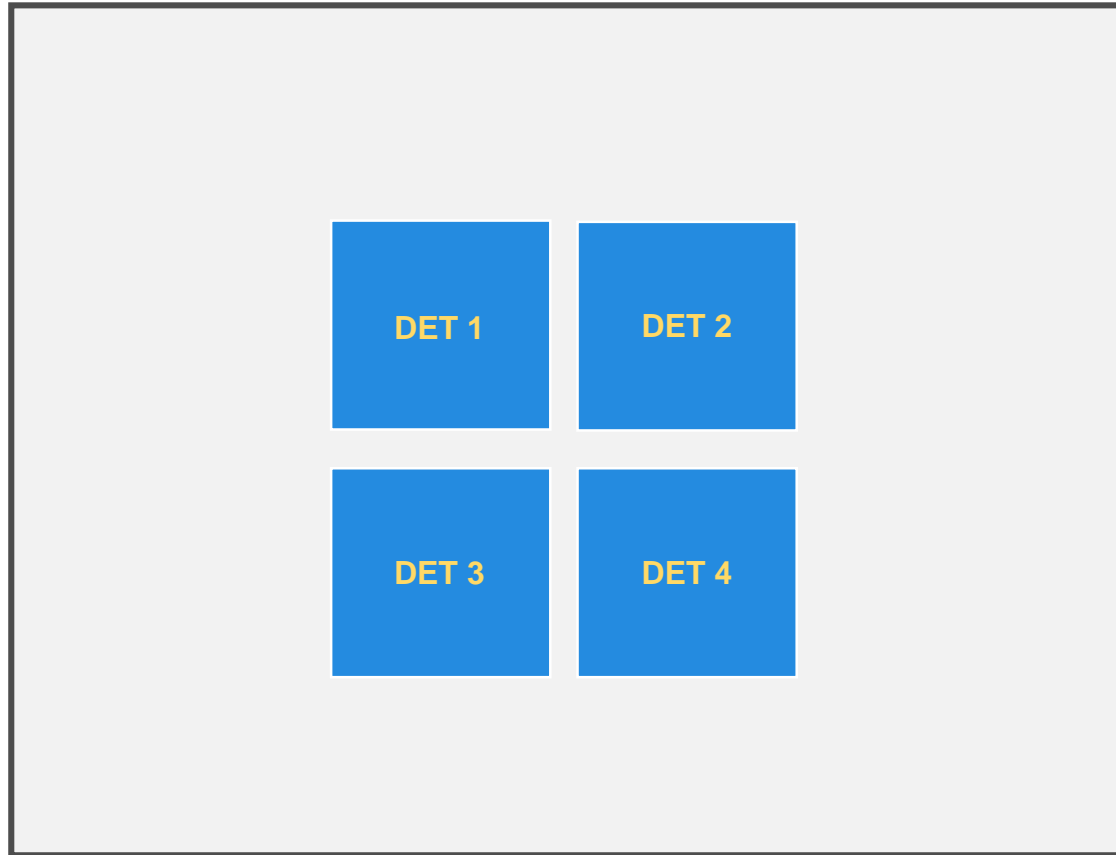
# IP

Platform will include an open and accessible open-source IP repository.



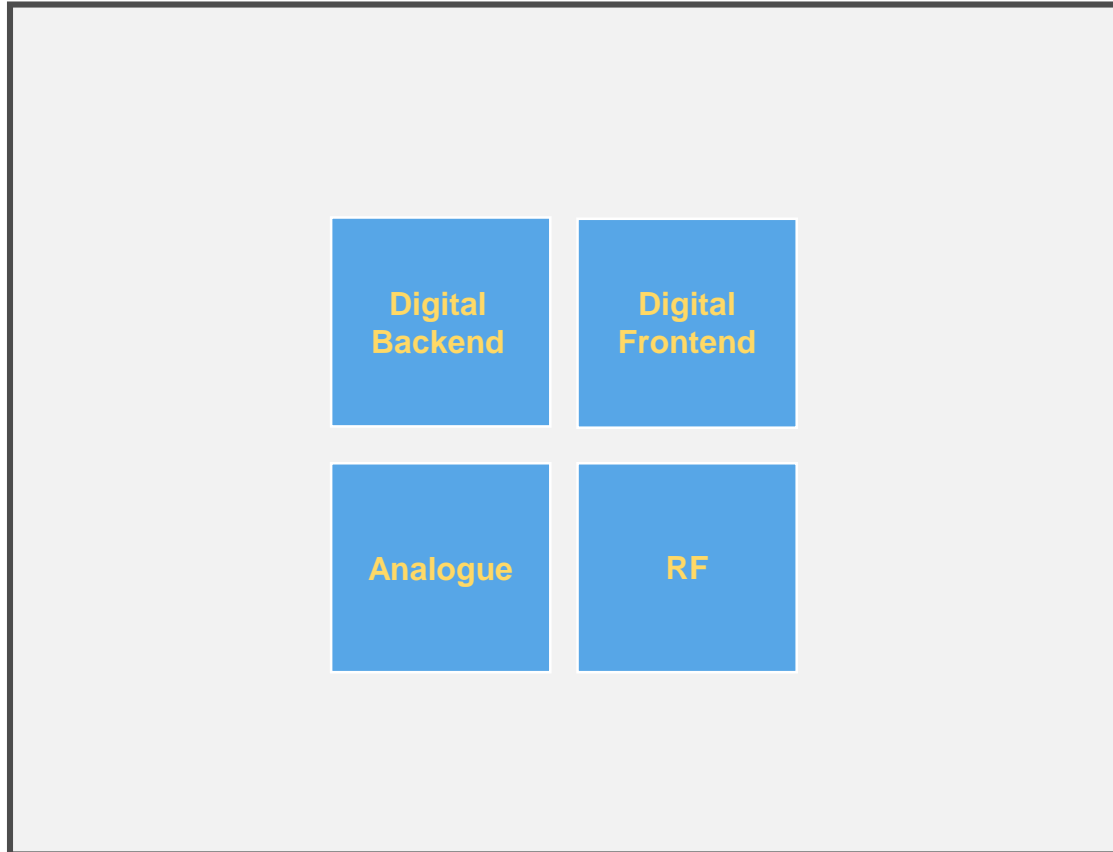
- The platform will offer both commercial grade IP and also other IP contributed by academia and the open-source community.
- Open-source IP can be sourced from **currently ongoing KDT JU projects**, such as TRISTAN, ISOLDE etc. and **other sources**
- Platform will facilitate **verification and validation** of IP.

# Design Enablement



- Facilitate access to PDKs and foundation IP from foundries.
- Ensures rapid design and allows users to have a more customised environment that better suits the needs of the user.
- Contribute to the development and maintenance of technology specific reference design flows and assists users in accessing the supply-chain.

# Training



- Vendors will be enabled to provide tool-specific training via the platform.
- Address re-skilling e.g. of software developers, physicists etc.
- Ensure synergies with Network of Competence Centres and provide a common platform from which users can access training in different Member States.

# EC RISC-V Roadmap

# Recommendations and Roadmap for European Sovereignty in Open-Source Hardware, Software, and RISC-V Technologies



Recommendations  
and Roadmap  
for European Sovereignty  
in Open Source  
Hardware, Software,  
and RISC-V Technologies

Report from the  
Open Source Hardware & Software Working Group

August 2022



## Key outcomes:

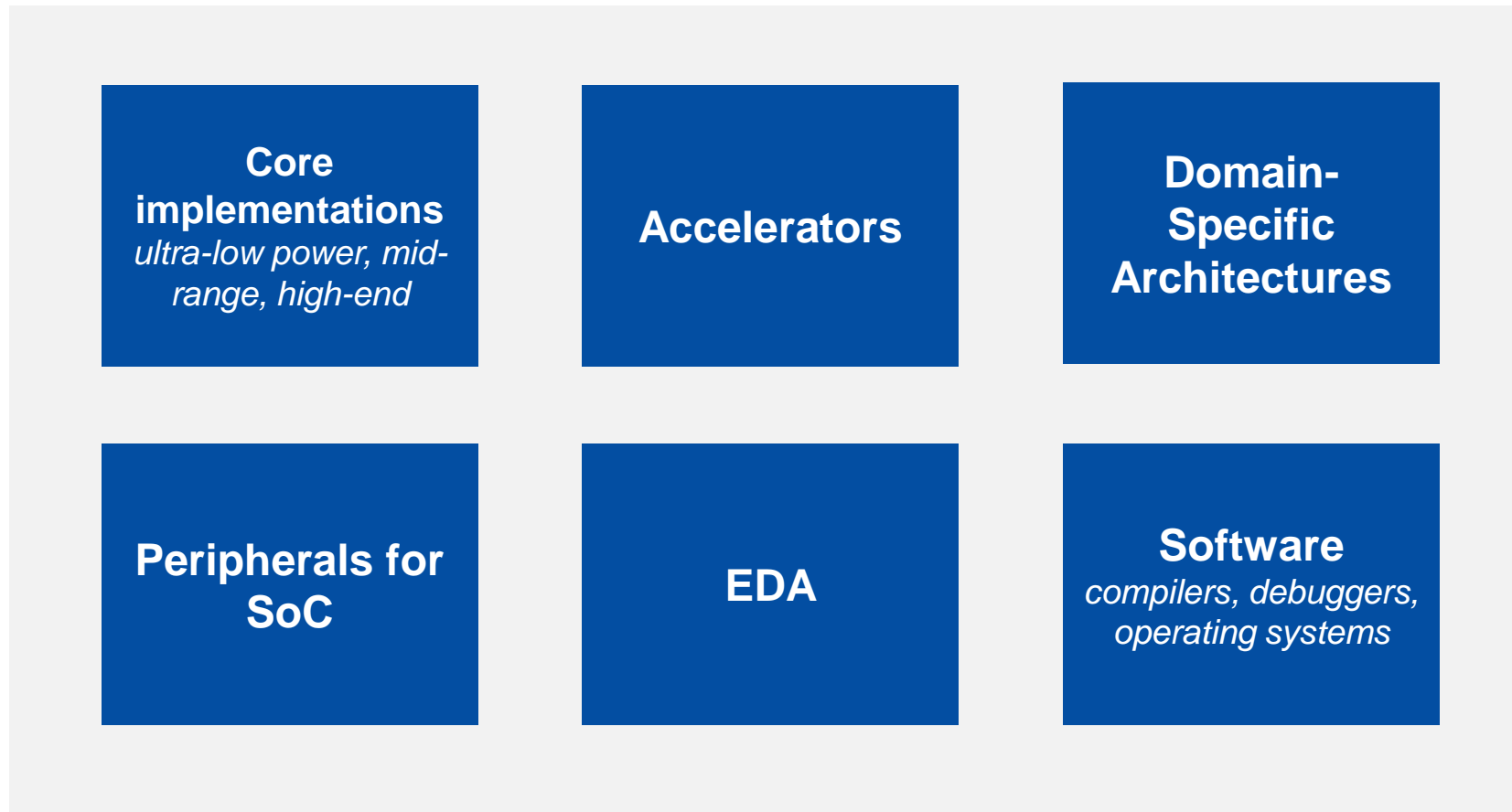
- Build a critical mass of European open-source hardware/software
- Develop both open-source hardware and software as they are interdependent
- Address cross-cutting issues
- Cultivate innovation
- Engage with the open-source community



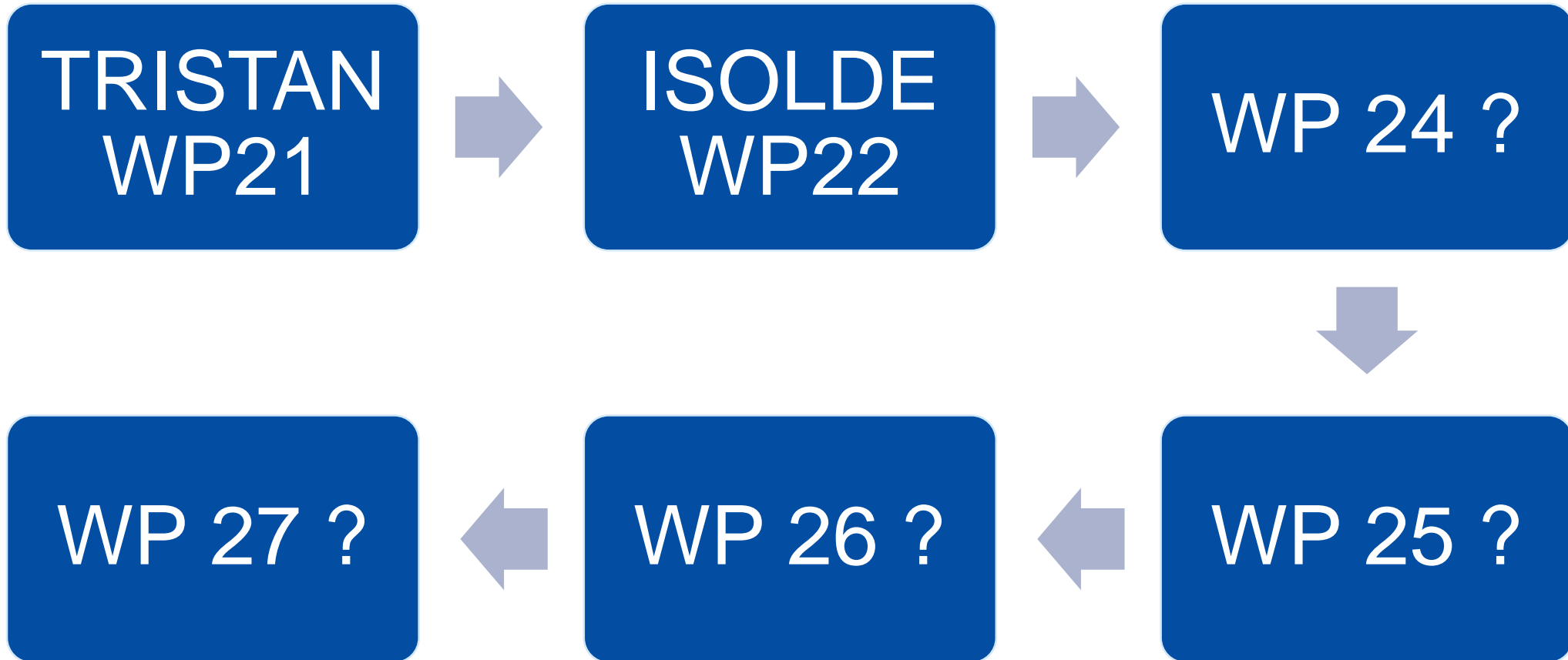
# Recommendations and Roadmap for European Sovereignty in Open-Source Hardware, Software, and RISC-V Technologies

- Open-source hardware is **a key sovereignty tool in line with Chips Act priorities**, providing Europe with an alternative to licensing IPs from non-EU third parties.
- A key success criterion for this is for Europe to develop **a fully blown open-source ecosystem**.
- This report has defined a strategic roadmap considering **short (2-5 years), medium (5-10 years) and long term (>10 years)** goals.
- The success of the roadmap depends on European actors working closely together to **create a critical mass of activities** that enhance and expand the European open-source community and its influence on the world stage.

# Recommendations and Roadmap for European Sovereignty in Open-Source Hardware, Software, and RISC-V Technologies



# Next steps – KDT/Chips JU



# Thank you

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