THALES
Building a future we can all trust

4 years of Open Source RISC-V at Thales

RISC-V Summit Europe, Barcelona, June 8, 2023

Thierry Collette, Ph.D.

Thales Research and Technology

Open HW : New research opportunities

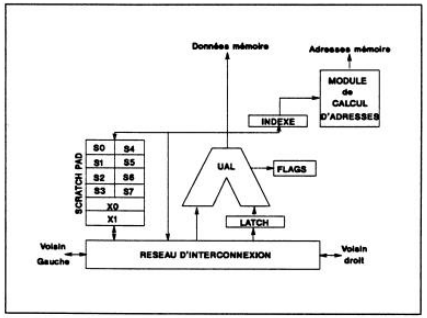
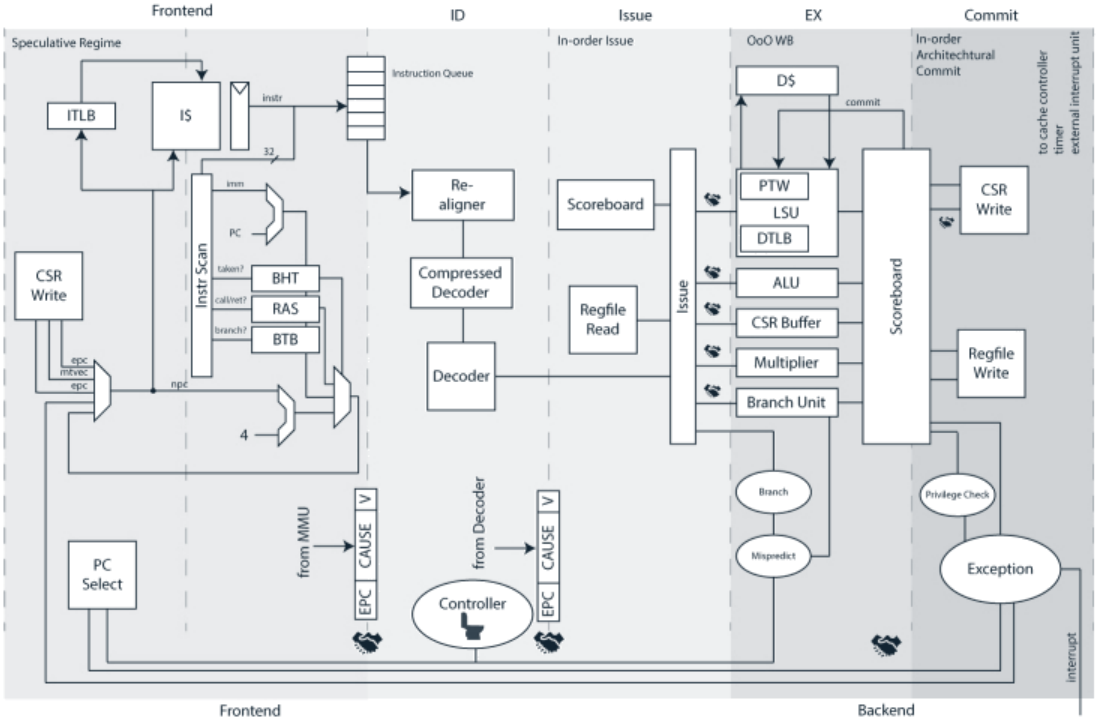


Figure II.1.3 : L'architecture de l'unité de traitement (ou processeur élémentaire) de SYMPATI2. L'unité arithmétique et logique (UAL) contient également un multiplieur. Le chemin interne des données est de 16 bits, les échanges avec les voisins gauches et droits s'effectuant sur un format de 8 bits.

SYMPATI2 : SIMD Processor Architecture

(T. Collette Ph.D.)

CVA6 pipeline architecture & ISA



CV32A6: RV32IMA[F][C]_Zicsr_Zifencei M/S/U [Sv32]

CV64A6 - RV64IMA[F[D]][C]_Zicsr_Zifencei M/S/U[/H] [Sv39]

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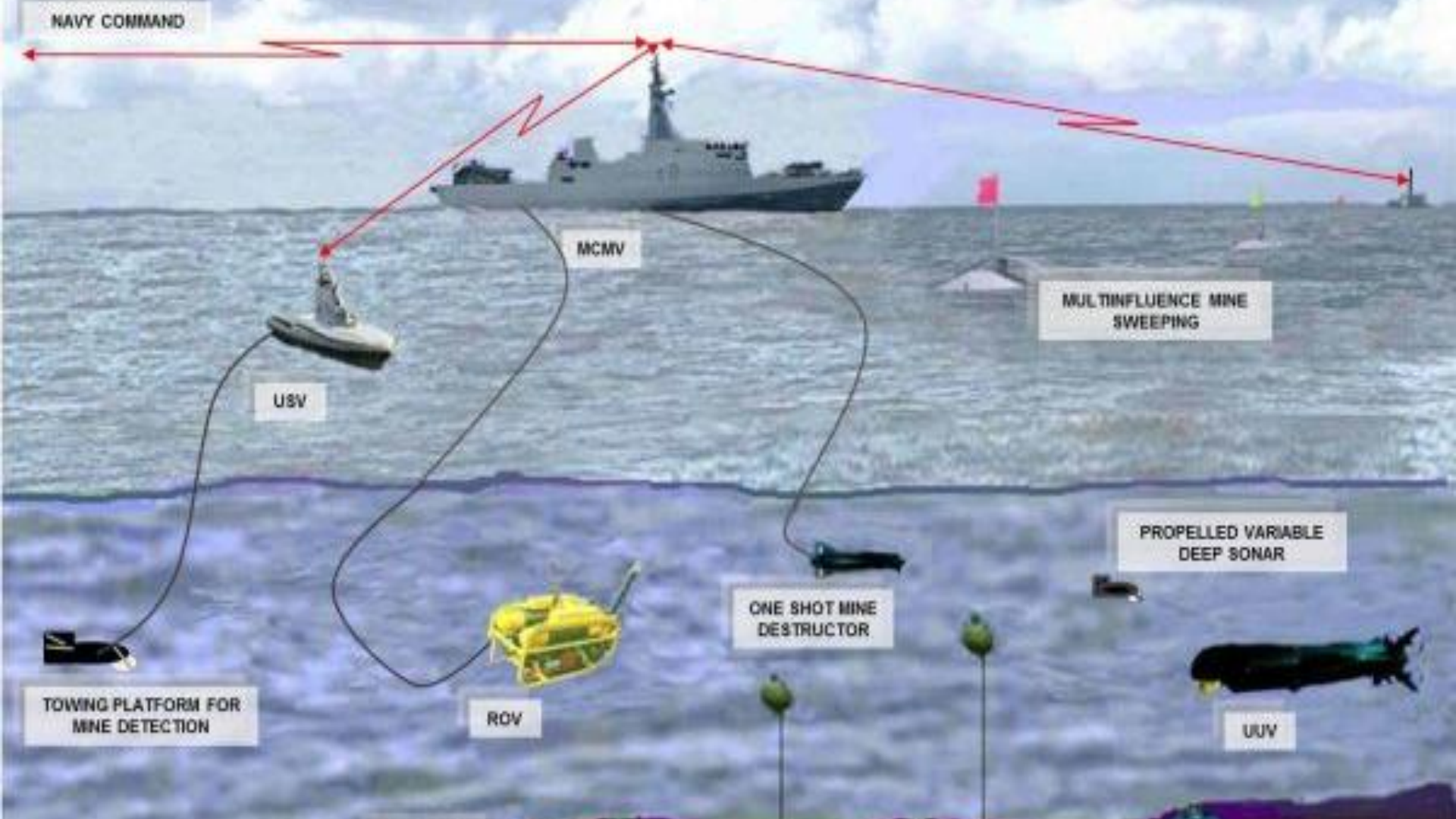
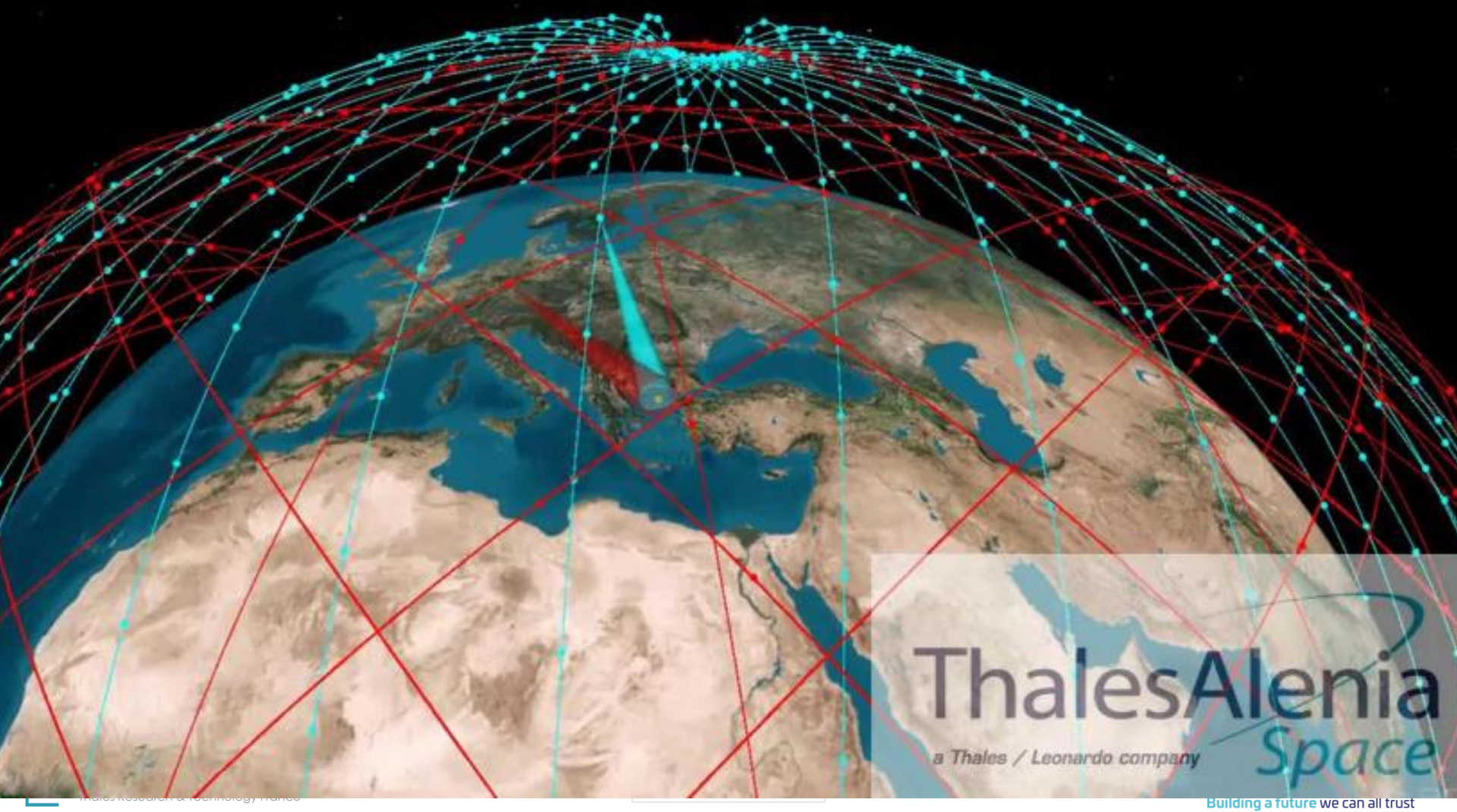
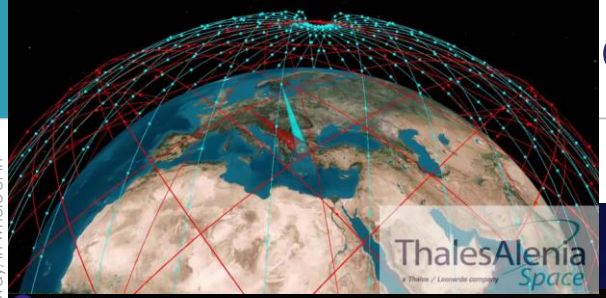

NAVY COMMAND
MCMV
MULTIINFLUENCE MINE SWEEPING
USV
PROPELLED VARIABLE DEEP SONAR
ONE SHOT MINE DESTRUCTOR
TOWING PLATFORM FOR MINE DETECTION
ROV
UUV

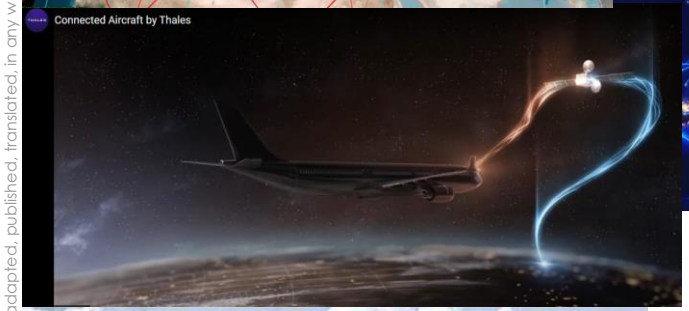

SELF-DRIVING
SEARCH
60 Km
60 Km
75 Km


by Thales

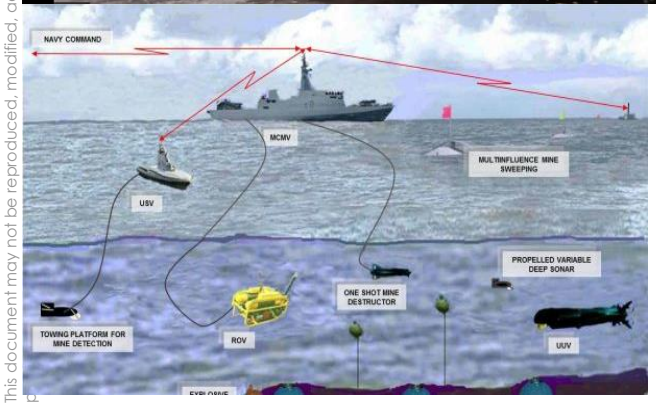

ThalesAlenia
a Thales / Leonardo company
Space

CONTINUOUS & TRUSTABLE COMPUTING SOLUTIONS

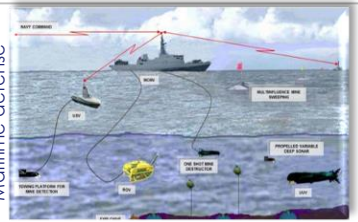




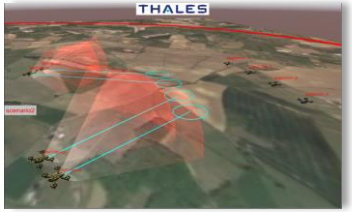
- Autonomy
- Low Power
- Safety
- Cybersecurity
- Interconnection
- Cloud-Edge-IoT



Exemple of AI R&T Challenges


Maritime defense


Collaborative combat



UxV


Aerian Traffic Control

Sensors

Modelization

BigData
Machine Learning

Symbolic AI
(Rules, Constraints…)

Hybrid AI

Simulation / Digital twin

Inference, Optimisation & Decision

Embedded AI

Distributed AI

Trustworthy AI

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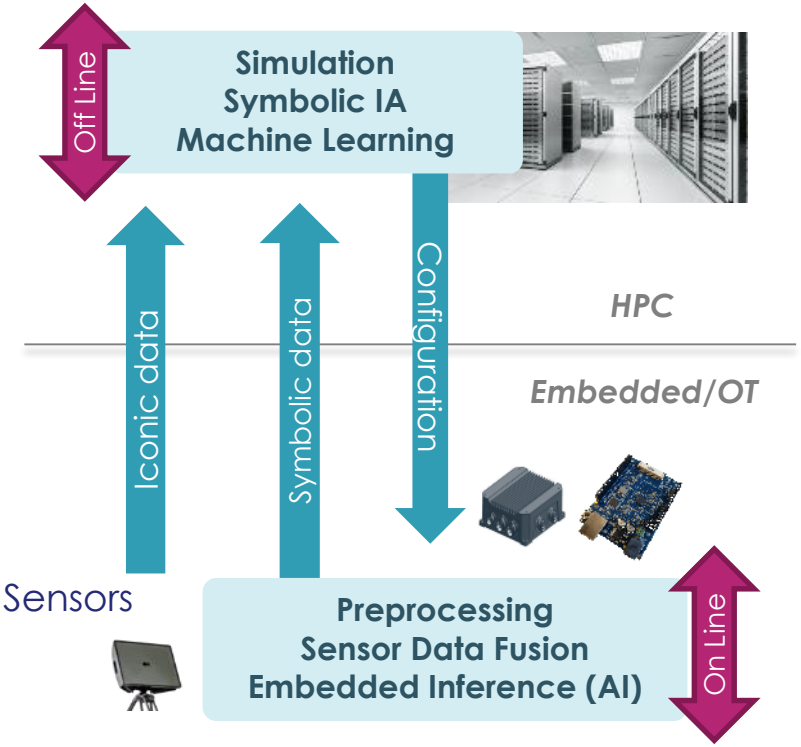
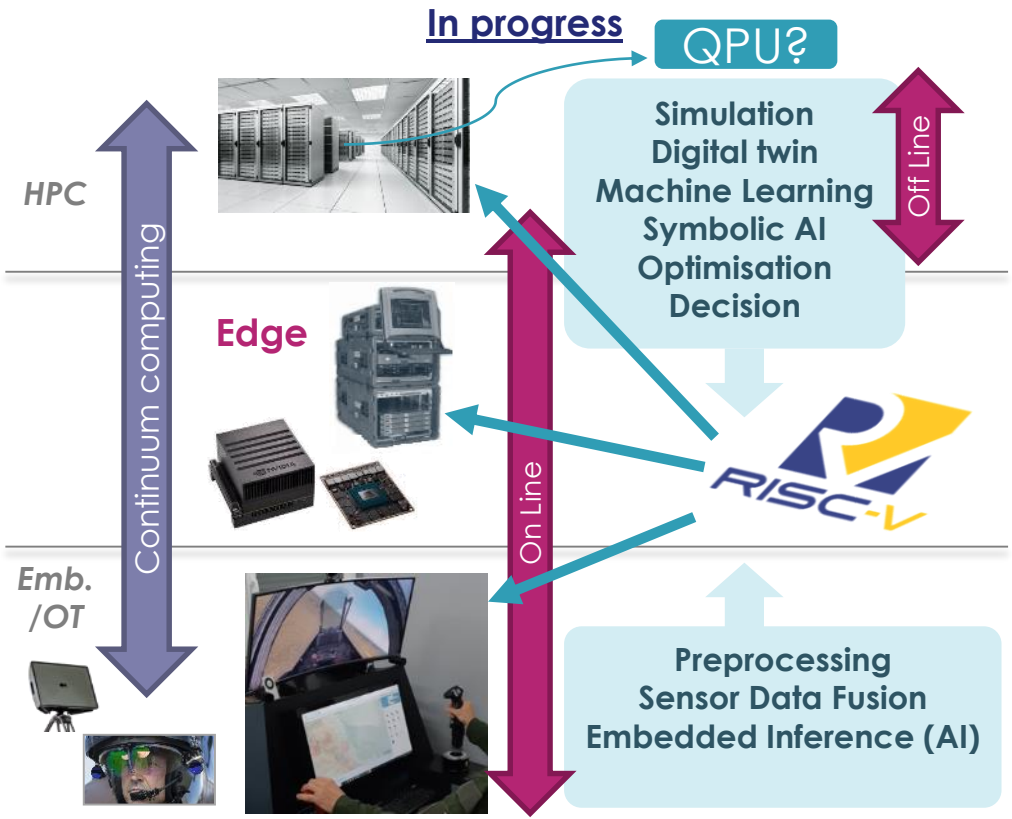
Exemple of R&T challenges for IT – OT convergence

Before



In progress



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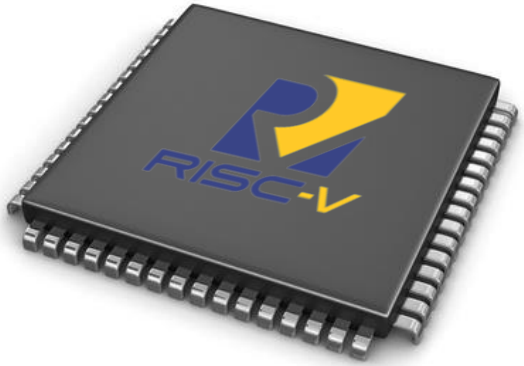
Why Thales invests in RISC-V? Main differentiators :

No vendor-locking & Sovereignty & Share cost instead of purchasing IP

- Open-source community
- Business opportunities for support, customization…
- Possible commercial exploitation without export constraints
- Enable strong EU investment



SWaP & customization & Safety & Security

- Exact fit between features and application needs
- A fully auditable processor
- No black-box

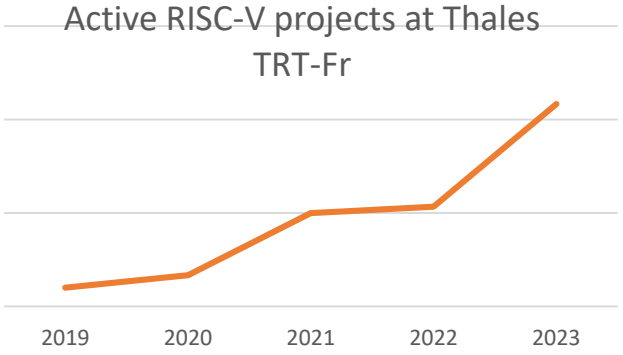
Enablers of RISC-V wave

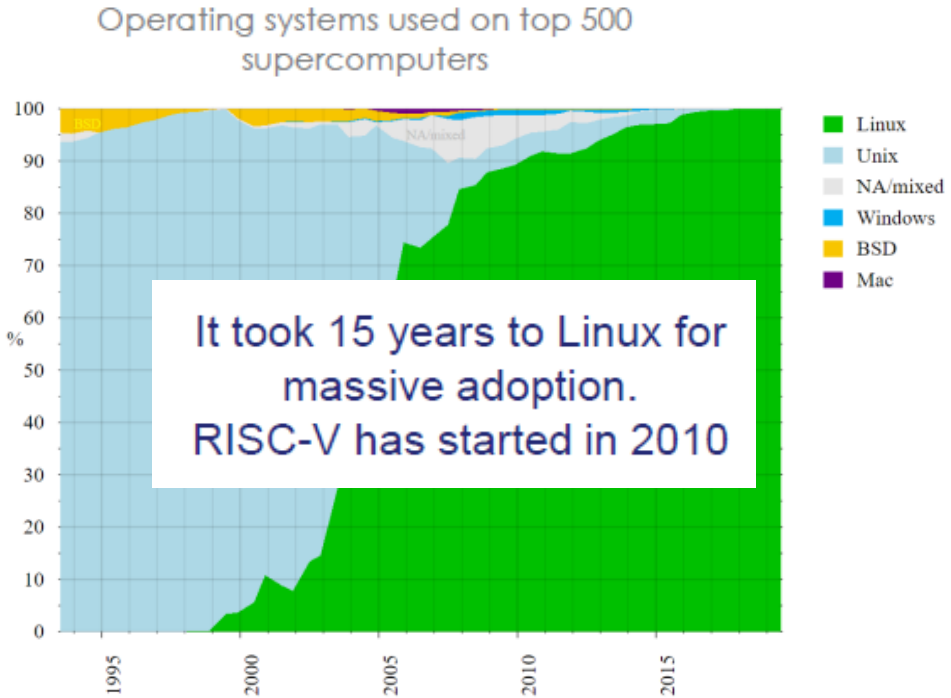
Software and service ecosystem

- Academic and Industrial
- across implementations

Performance

- State-of-the-art processor
- **Minimum mass production**





Our RISC-V communities

RISC-V International (“the Foundation”)

- Specifies the open **RISC-V instruction set**
  - ✓ Simple & modular
  - ✓ 32- or 64-bit
  - ✓ Custom extensions
  - ✓ Covers a wide range of needs, **from MCU to HPC**
- Currently specifying **upcoming optional extensions**
  - ✓ E.g. bit manipulation, crypto…
- Hosts several **special interest groups** (SIG)
- Does not deliver implementations

OpenHW Group

- **Not-for-profit corporation** steered by its members
- Goal: deliver **open-source IP for production SoCs**
  - ✓ RISC-V compatible cores
  - ✓ SoC IP blocks
  - ✓ Verification environment
  - ✓ Supporting SW and tools
- Permissive, open-source, export-friendly **license**

Open-source is suited for industrial use

OpenHW governance

- Not-profit organization steered by its members
- Based on Eclipse Foundation's processes
- Target industrial-grade quality

Participation is encouraged:

- Share IP development costs
- Influence technical content
- Get recognized as a contributor

Apache / Solderpad permissive licences

- Freely use, modify, integrate in proprietary solutions
- No need to publish modifications, no viral effect

Value generation

- Share cost instead of purchasing proprietary IIP
- Customize for own application
- Increase control on your solutions
- Easier white box certification

Business models

- Commercial SW/HW/tooling add-ons
- Maintenance and support offers

Reduced supplier / export risks

- Ability to fork; no end-of-life
- Significantly lower exposition to export control

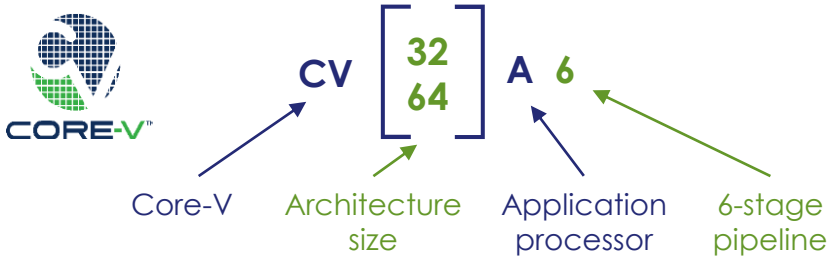
CVA6 core

Open-source RISC-V application core

- Supports rich OSes like Linux

Common source code, two flavors:

- CV64A6
  - 64-bit
  - ARIANE donated by ETH Zürich to OpenHW
- CV32A6
  - 32-bit
  - Compact version designed by Thales



An academic project turning into an industrial-grade CPU core

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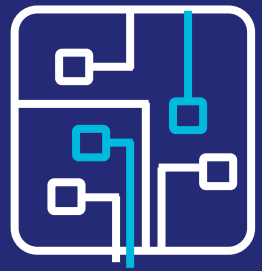
HW implementations

CV32A6	FPGA			
Frequency	125 MHz			
Performance	2.25 CoreMark/MHz 281 CoreMark			
Resources	10,416 LUT	6,313 FF	10 BRAM	4 DSP
Technology	Zynq UltraScale+ -3			
Configuration	RV32IMA, 8K D$ + 8K I$, noFPU, MMU			

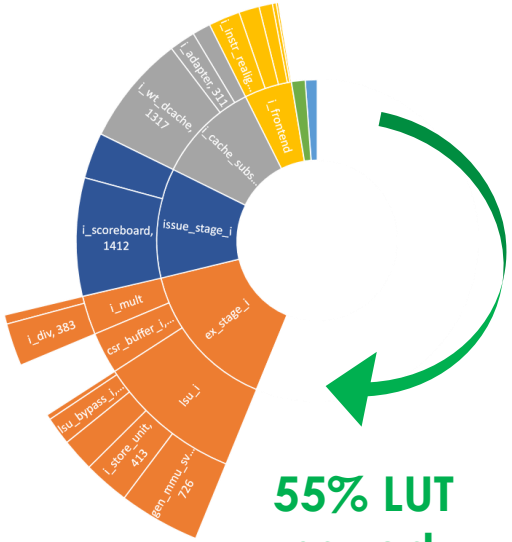
CV32A6	ASIC
Frequency	900 MHz
Performance	2.5 CoreMark/MHz 2250 CoreMark
Resources	80 kgates
Technology	28 nm (worst case corner)
Configuration	RV32IMA, 8K I$ + no D$, noFPU, MMU



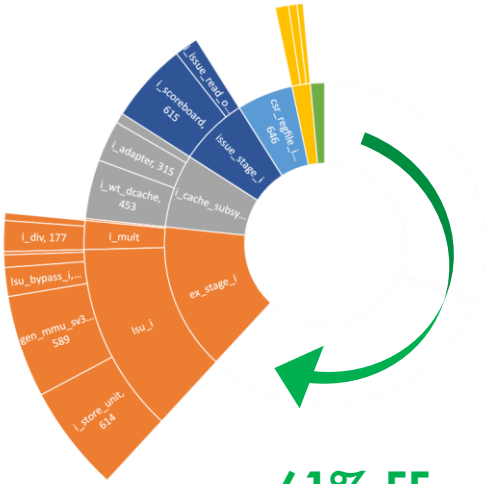
Ongoing work.

More optimizations are coming!

CVA6 2022 results: FPGA optimization



55% LUT saved



61% FF saved

140 MHz

100 MHz

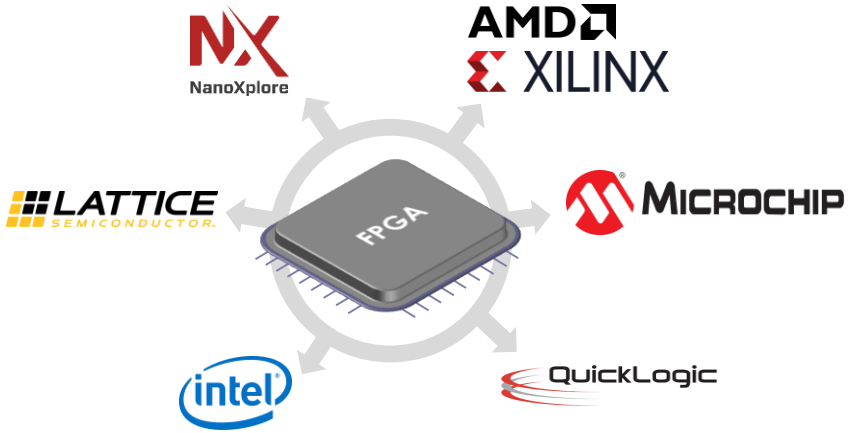
	Original CV32A6	Optimized version	Evolution
Look-up tables	18,103	8,077	−55%
Flip-flops	11,484	4,403	−61%
DSP blocks	4	4	-
Block RAM	36	12	−67%
Max. freq.	100 MHz	140 MHz	+40%
CoreMark/MHz	2.8	2.8	-
CoreMark	280	392	+40%

(Xilinx Kintex7)

Some optimizations are also beneficial for ASIC.

Multi-sourcing

- For **ASIC targets** (32/64 bit)
- For **any FPGAs** (32 bit)

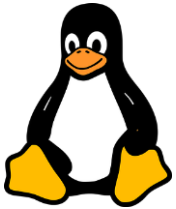


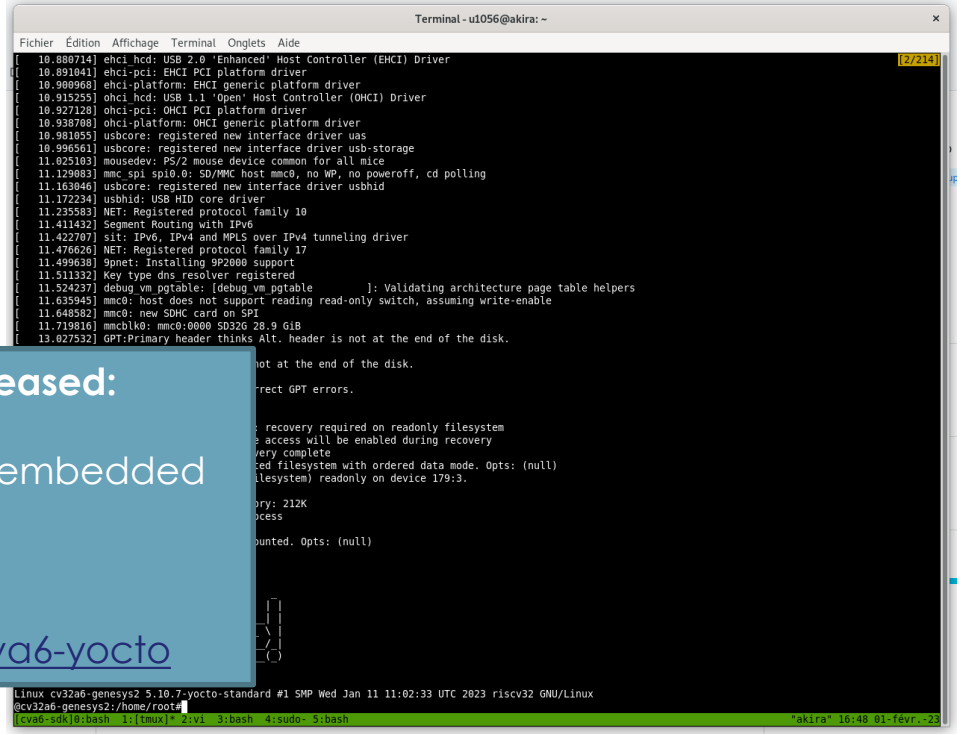
Leverage your investment: reuse your HW/SW architectures throughout your product range (multi-sourcing: any ASIC and FPGA vendors)

CVA6 2022 results: Linux Yocto available

U-Boot

yocto PROJECT





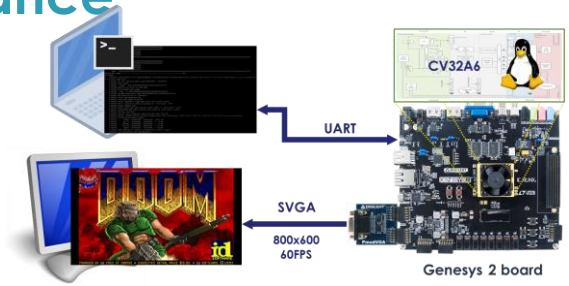
Up-to-date Yocto embedded Linux released:

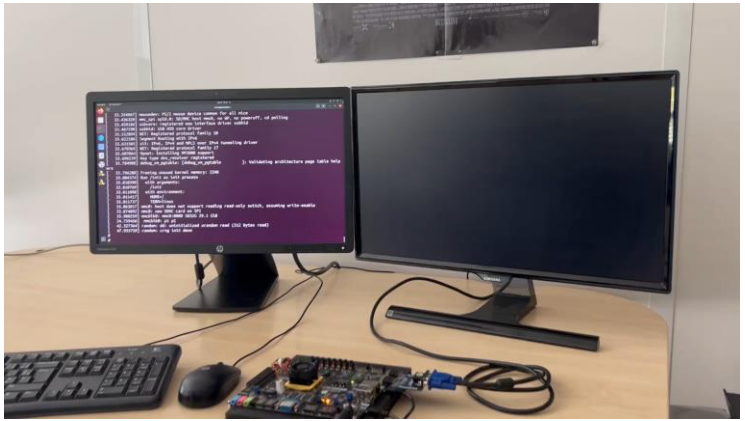
- The most popular distribution generator for embedded systems
- 32- and 64-bit support
- Built upon U-Boot and OpenSBI
- https://github.com/openhwgroup/meta-cva6-yocto

Demonstrator – Doom on CV32A6 soft-core

Demonstrates CV32A6 softcore performance

- Support of high-level software applications
- Implementation on the Genesys 2 FPGA board
  - Kintex 7 (XC7K325T-2FFG900C)
  - DDR3
  - PMOD-VGA connected to a monitor
- Yocto Linux OS running
- VGA framebuffer integration
  - SVGA 800x600 at 60FPS
- Chocolate-doom
  - 15 FPS





Ready for products

- Augmented reality
- Embedded HMI

RISC-V student contest

Organized by

- Prizes sponsored by Thales

Goals

- Promote RISC-V and computer architecture in French education
- Extend RISC-V and OpenHW communities
- Strengthen industry-academy connections

2020-2021: Improve CV32A6 FPGA performance

- 13 teams from 10 universities
- Awarded: Télécom Paris, U. Toulouse III

2021-2022: Improve CV32A6 energy efficiency

- 12 teams from 7 universities
- Bernhard Quendt, Thales CTO, gave out the awards
- Awarded: U. Strasbourg (2 teams), IMT Atlantique

2022-2023: Focus on CV32A6 security

SW ecosystem

OPENHW GROUP
PROVEN PROCESSOR IP

Boot and FW

- **U-Boot**
- **OpenSBI**

U-Boot · yocto PROJECT · freeRTOS

OS support

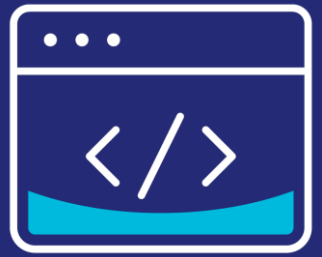
- **Linux:** 32 & 64 bit
- **Yocto** honister, Buildroot 2021.08
- **FreeRTOS:** 32 & 64 bit
- CVA6 compatible with many others

Compiler

- Standard **GCC** (11.2)
- Libraries: **glibc** (2.70) & others
- LLVM on the roadmap

Debug

- HW and baremetal: JTAG probe, OpenOCD, GDB
- Linux-based: GDB server, GDB/Eclipse IDE



Full open-source software ecosystem

Protect your HW investments

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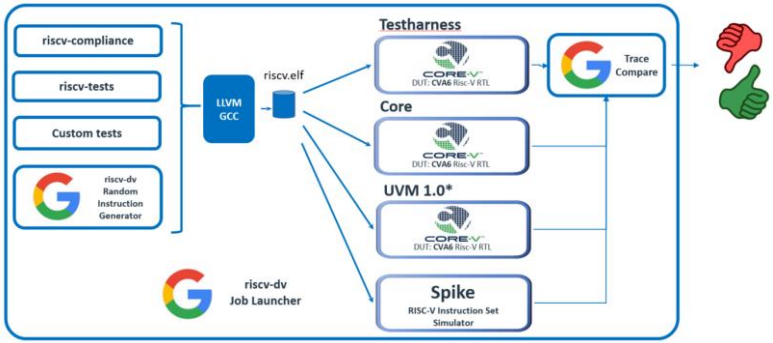
CVA6 verification

Continuous integration (CI)

Leverages Google open-source components and OpenHW methodology

Next steps:

- Complete UVM testbench
- New test sequences
- 100% functional coverage (UVM-based)



Verification artifacts will be available as open-source.

Target is 100% verification coverage.

An extendable core

CV-X-IF interface to extend the CVA6 instruction set

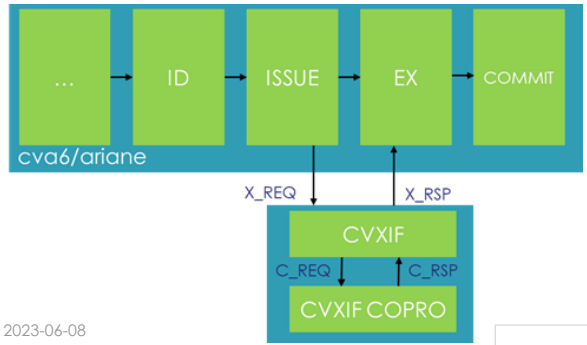
- Current or future RISC-V extensions
- Custom extensions (crypto, DSP, AI…)

CV-X-IF specified by OpenHW Group

- Open specification, can be used off OpenHW
- Reuse coprocessors between CORE-V cores (CVA6, CV32E40X, CVE2)

Compiler support

- Seamless for RISC-V standard extensions
- LLVM should ease the support of custom extensions
- Inline ASM possible for specific processing



Speed up your application with a custom accelerator

Add extensions without fully re-validating the core

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Soft-core roadmap

OPENHW GROUP
PROVEN PROCESSOR IP

2020

CVA6 initially designed for ASIC & in 64 bits

2021

- **32-bit CVA6 version** (ASIC & FPGA)
- First optimized **FPGA soft-core**
- Support of **Linux**
- Dual-core version running Linux SMP

2022

- Optimizations **(+50% freq**. and **-30% area**)
- U-Boot, OpenSBI, **Yocto**

202x

More optimizations to come!

An industrial roadmap for an open-source soft-core

Conclusion

Join the development of an industrial-grade open-source processor

- Get funding from the HE, KDT JU and ESA for IoT and Edge and EuroHPC JU for HPC and Edge
  - EU institutions are strongly supporting RISC-V sovereign technologies
- Influence next developments for your future products

Participate in the next open-source revolution

- The next “Linux” for hardware CPUs

Use the CVA6 in your future products

- For ASIC and FPGAs
- With a strong open SW ecosystem

And we will success with a sustainable Ecosystem and Mass Production

Thanks to the Thales Teams :

- DIS/INVIA,
- Thales INDIA,
- TRT-Fr.