IMPLEMENTATION OF A RISC-V ENABLED EDGE-COMPUTING ARCHITECTURE FOR NFC COMMUNICATIONS

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Introduction

About myself

- Senior Digital Design Engineer, working at NXP Semiconductor Austria in Gratkorn (Austria)
- Responsible for Concept, Design, Implementation & Verification of DSP modules for NFC Signal Processing
- Team Technical Coordinator

About my Unit

- PL focussed of integrated solutions for NFC Secure Embedded Transactions & Identifications
  - Mobile Wallet, Transit, Wireless Charging and IoT
- Gratkorn Team responsible for NFC Digital Modem development
- Partnership with European Universities (Masters, PhD, Internships)
- Research activity funded by EU TRISTAN KDT-JU project

BL
SECURE CONNECTED EDGE

PL
SECURE EMBEDDED TRANSACTIONS

SOC/DIP UNIT
NFC MODEM GROUP

NXP Semiconductors Austria *(Graz, Austria)*

Facts & Stats about NXP Austria

Based in Steiermark, 10 km away from Graz city center;

Founded in 1987 as Start-Up Mikron;

Acquired by Philips in 1995, became NXP in 2006;

700+ employees from over 50 nations;

130+ students (interns, master, PhD) from all European Universities;

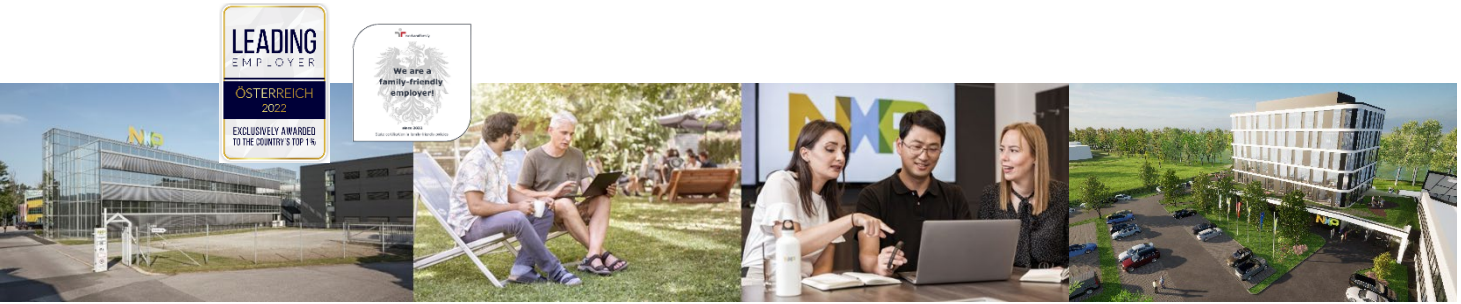
Site awarded multiple times as ***Leading Employer*** in Austria and ***Family Friendly Employer***.

Business Areas & Functions

- 5 Product Lines focusing on Automotive, IoT and Security
- Competence Center Crypto & Security, Battery Mgt Systems
- Marketing & Product Management
- Customer Application Support

Collaboration & Cooperation

- Leading Universities and Research Institutes
- Semiconductor Cluster Industries
- National & European Funded Programs



SECURE CAR ACCESS

NFC & RAIN RFID ICS

TRANSPORT TICKETING

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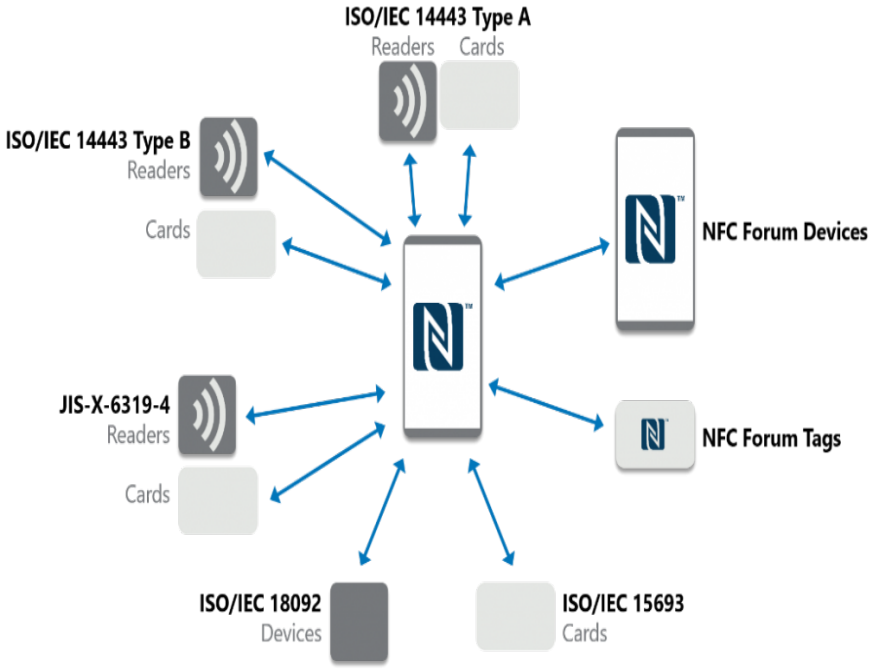
BATTERY MANAGEMENT

www.nxp.com/careers

NFC in a nutshell

What is NFC?

- Radio Frequency Identification (RFID) technology, operating at 13.56MHz
- Set of protocols to enable close-proximity (>2cm) communication between two devices
- Currently deployed in billions of IoT devices worldwide:
  - Mobile payment
  - Secure Identification & Access
  - Wireless charging, etc.



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NFC in a nutshell

How does NFC work?

- Communication actors are “Initiator” and “Target” devices
- “Initiator” generates the carrier field and starts the communication
- “Target” responds to the “Initiator” commands and can operate:
  - Passive: “Initiator” responds by modulation the carrier field
  - Active: “Initiator” responds by generating its own RF field

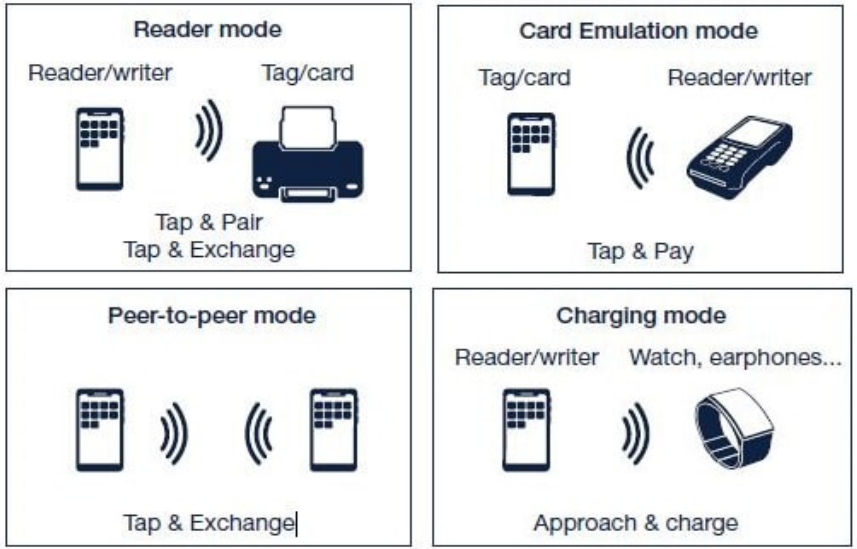

Fig1. NFC main use-cases

Problem statement

NFC devices state of the art

- Considerable amount of analogue and digital signal processing
  - High performance and robust communication in different operative conditions
  - Support multiple communication standards
- Signal modulation/demodulation is performed with custom analogue and digital circuitry
  - Tx chain: digital circuitry activates the analog drivers to operate the RF field
  - Rx chain: analog circuitry brings the RF field frequency in band and generates an ADC stream for reception in the digital domain

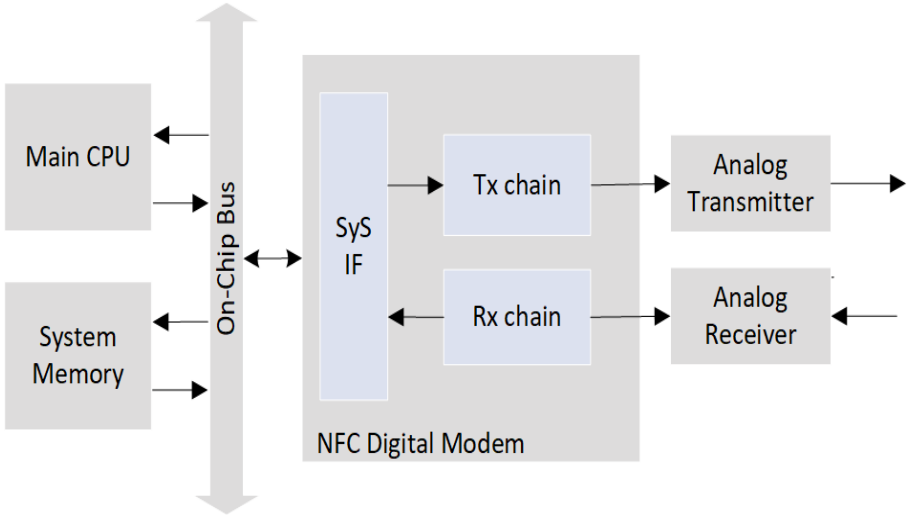

Fig2. high level block diagram representation of an NFC IC. The picture is not meant to be detailed and/or used as a reference for NFC IC developments.

Problem statement

Drawback

- Limited functional flexibility on silicon
  - ➢ E.g.: new standards and/or features cannot be supported
- Limited bugs mitigation actions on silicon
- High pre-silicon design/verification effort required
  - Might hindering end product evolution
  - Might be unacceptable on a business standpoint

Proposed solution - Overview

Overview

- NFC edge-computing architecture, based on RISC-V core
- RISC-V core to execute real-time DSP operations
- Advantage:
  - Enhanced on silicon flexibility
  - Lower pre-silicon engineering cost
- Disadvantage:
  - Potentially higher resource usage (e.g. memory demand)
  - Higher clock rate to ensure (pseudo-) real-time operations execution

Related works

- To the best of the authors' knowledge, no other similar work is currently published
  - Drawback of using custom digital/analog logic to perform DSP operation in wireless communication and the advantage of using an edge-computing architecture were analysed in many IEEE publication

Proposed solution – Architecture

Architecture proposal

- Microprocessor unit integrated within the NFC digital modem
- Microprocessor unit in charge of performing DSP operations in the Rx chain
- Microprocessor unit clocked with higher clock (e.g., x4, x8) wrt the NFC digital modem
- Microprocessor unit formed by the following main blocks:
  - Dedicated IF to exchange selected signals with the NFC digital modem
  - DMAC
  - On-chip bus manager and subordinate connections
  - Interrupt controller and timer units

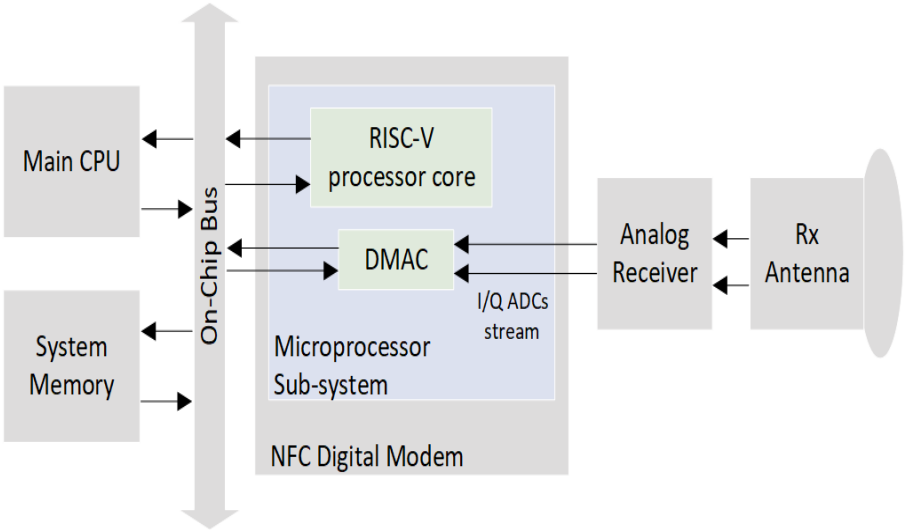

Fig3. high level block diagram representation of the proposed NFC edge-computing architecture. The picture is not meant to be detailed and/or used as a reference for NFC IC developments.

Proposed solution – Current Status

The activity is proceeding following a 2 steps approach:

- (1) Implementation of a microprocessor unit based on an NXP proprietary RISC-V core
  - Microprocessor unit integrated within an existing NFC digital modem prototype
  - Selected RISC-V core instances an FPU unit to improve DSP operations precision
  - Microprocessor unit to execute auxiliary DSP tasks for Rx
  - Microprocessor unit clocked at x4 the NFC modem main clock frequency
  - PoC: real-time monitoring of an RF field shape for tag detection within the RF field generated by the reader

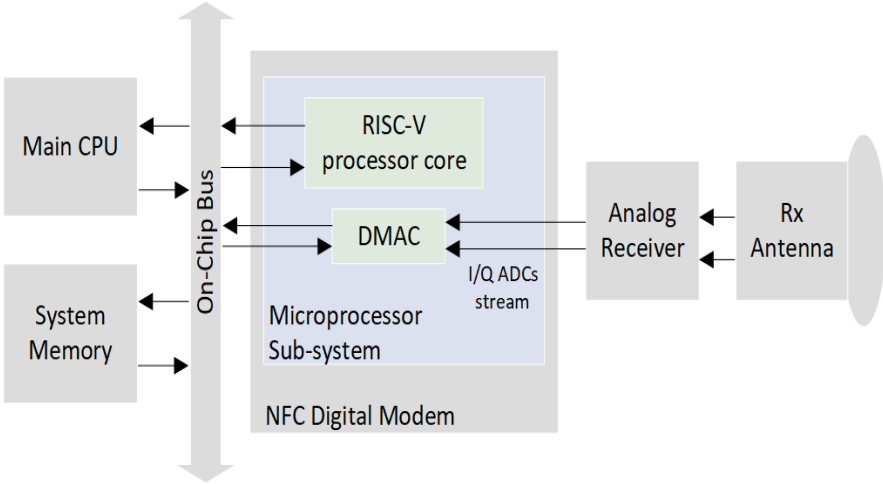

Fig4. high level block diagram representation of the proposed NFC edge-computing architecture. The picture is not meant to be detailed and/or used as a reference for NFC IC developments.

Proposed solution – Current Status

The activity is proceeding following a 2 steps approach:

- (2) Implementation of a microprocessor unit based on an OpenHW RISC-V core

  - Microprocessor unit prototype is currently under development
  - Selected RISC-V core is the CV32E40X (ISA extension port)
    - Committed activity under TRISTAN focuses on RISC-V ISA extensions
    - RISC-V ISA extension supported by an ad-hoc compiler tool
  - Microprocessor unit to execute real-time Rx message demodulation
  - PoC: ISO 1443-2 typeA 106kBd message demodulation of a “tag” response
  - Early stage results:
    - RISC-V core supported by a co-processor unit to enhance performance
    - The co-processor module implements a MAC unit a supports SIMD instructions
    - Microprocessor unit successfully demodulates a typeA 106kBd “tag” response
    - Total number of instructions per sample is around 75; ADCs samples refresh frequency is 13.56MHz (73.74ns); downsampling by a factor of 2 => Required clock frequency is around 500MHz (540MHz to account for some margin) to perform real-time operations (unfeasible for the target use case)

*Used equation:

$$\text{required frequency} = 1/(73.74\text{ns}*2/75)$$

Proposed solution – Current Status

- (2) CV32E40X Extension Interface
- 6 bus interfaces:
  - Compressed
  - Issue
  - Commit
  - Memory
  - Memory result
  - Result

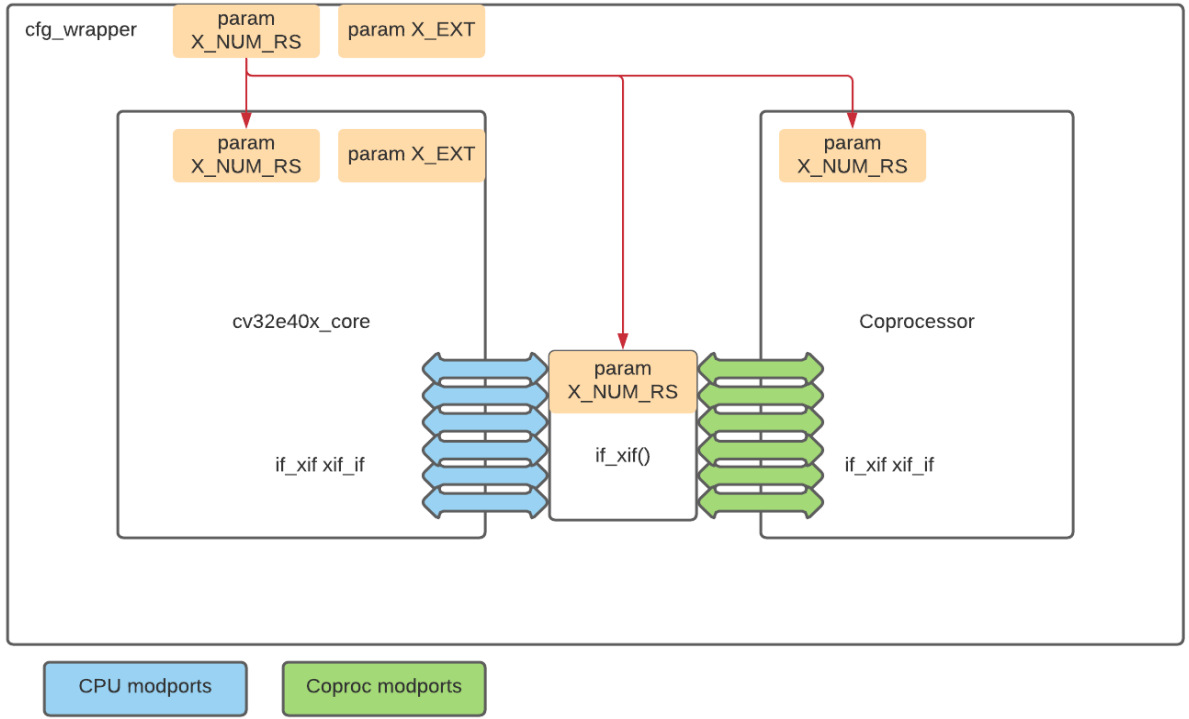

Fig5. CV32E40X Extension Interface

Proposed solution – Current Status

- (2) Co-Processor Architecture

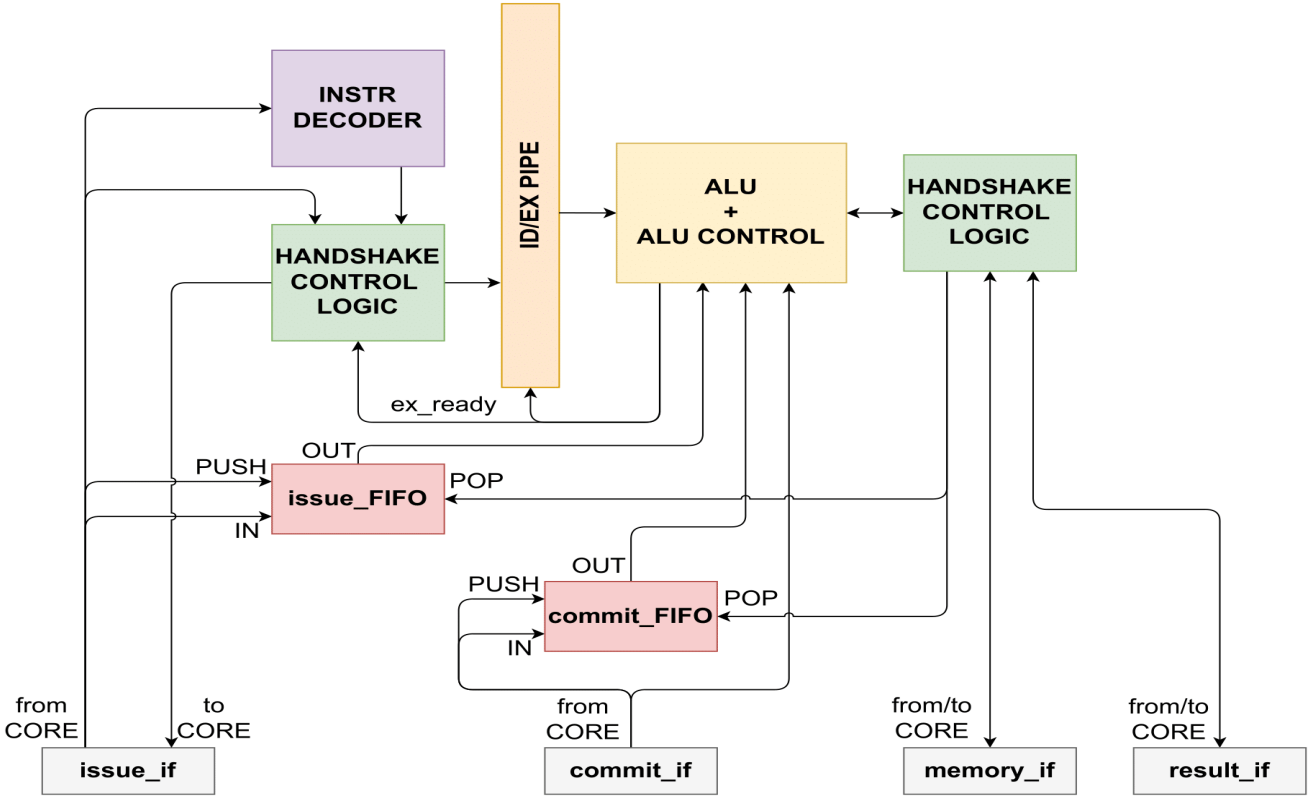

Fig6. Co-Processor Architecture

Proposed solution – Current Status

- (2) MAC Architecture

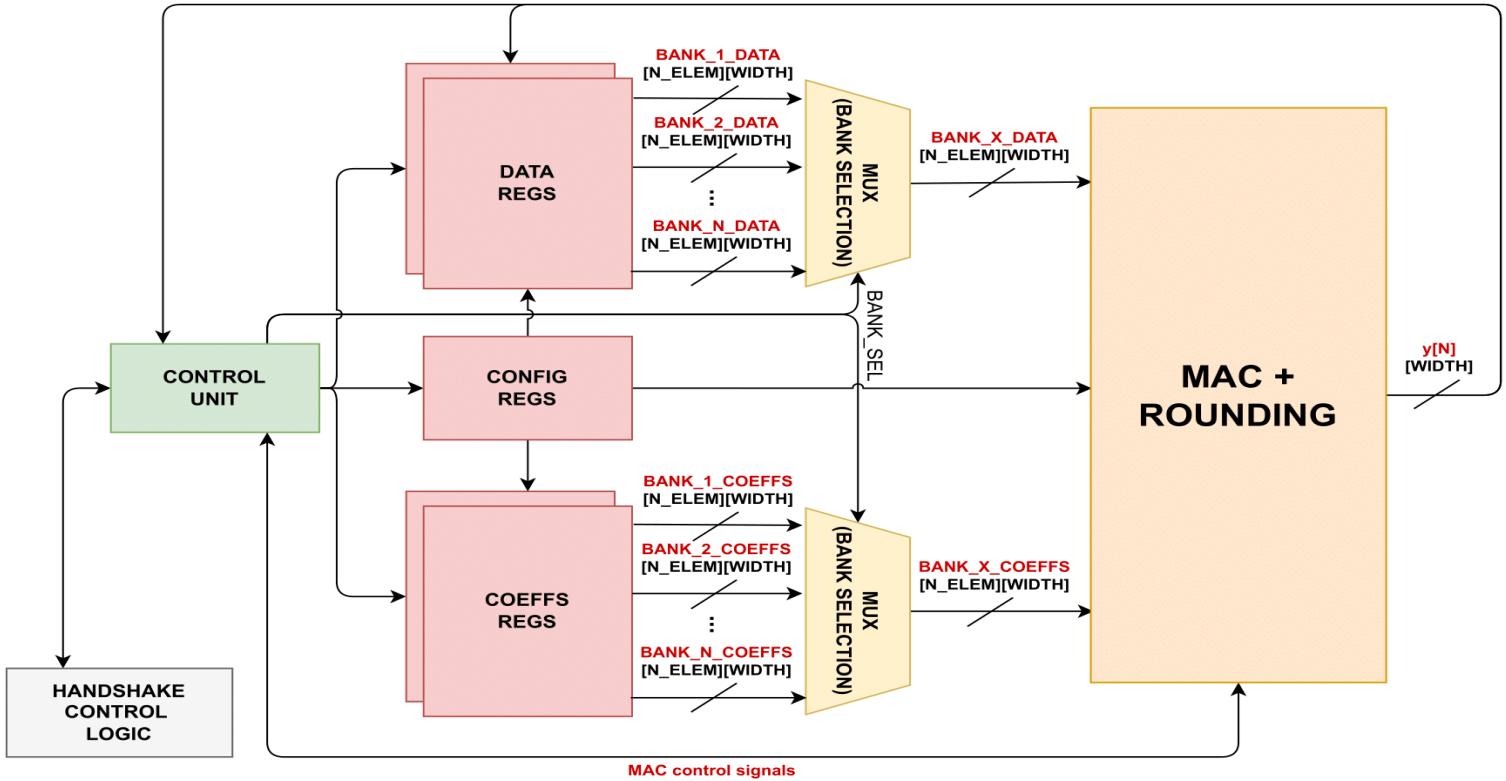

Fig7. MAC Architecture

Future ambition

- Short term ambition is to demodulate a Type-A 106kBd “tag” response with:
  - Feasible clock constraints
  - Feasible area and memory requirements
  - Focus in 2023: enhance HW/SW architecture
  - Focus in the incoming years: integrate the proposed solution in an existing NFC IC
  - This activity is committed in the scope of TRISTAN project

- Long term ambition is:
  - To demodulate a “tag” response of all NFC forum supported standards
  - To demodulate a “reader” command of all NFC forum supported standards
  - In short, the microprocessor unit becomes compliant to the layer2 of the NFC forum
  - To adapt to new standards and/or new features
  - This activity is committed as **optional** in the scope of TRISTAN project

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