Building commercially relevant open source silicon

The many aspects of Ibex

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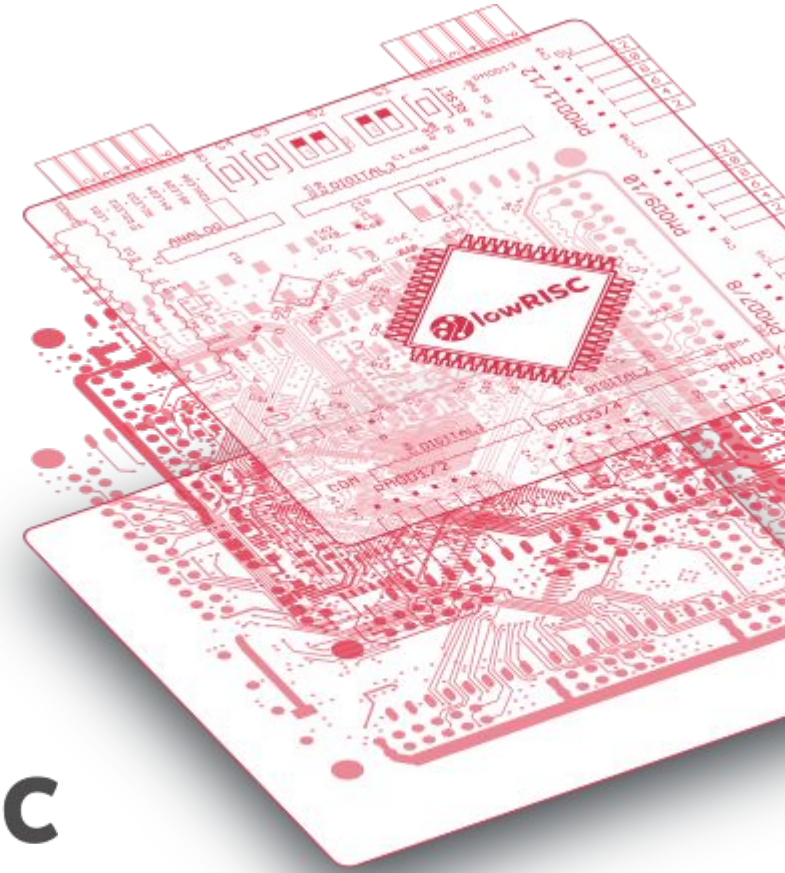
opentitan

lowRISC



OpenTitan

- OpenTitan - An open-source silicon root of trust for industry
  - Multiple security/cryptography related accelerators (such as AES, OTBN, KMAC)
  - Various peripherals such as SPI, USB, I2C, UART
  - Discrete chip (RTL frozen May 2023 in preparation for tapeout) and Integrated variants (under development, using Discrete chip as a base)
  - www.github.com/lowrisc/opentitan
  - www.opentitan.org
- And OpenTitan needed a secure CPU…

Ibex

- lowRISC takes responsibility for zero-riscy from ETH Zürich and renames it Ibex
- An open-source RV32IMCB core, w/ additional extensions for Security, IoT and embedded applications
  - ePMP, debug, instruction cache, 2 or 3 stage pipeline
  - Dual core lockstep for fault detection and a variety of other security features (for use in OpenTitan)
  - Highly configurable
  - www.github.com/lowrisc/ibex
- Comprehensive documentation and DV

So What?

So What?

- RTL is only one aspect of what is required for designs viable for commercial usage
- Comprehensive DV, with full code and functional coverage is vital
- RTL needs to be consumable
  - Usable by a variety of EDA tools
  - Uniform style and adherence to SystemVerilog best practices for synthesis
  - Lint clean
- DV needs to be credible
  - Complete test plans and coverage plans
  - Nightly regressions with published results
- Project must be active and maintained
  - Code review and CI employed to ensure standards are met
- Silicon Commons framework

DV Strategy

- Major focus of recent Ibex work
- Randomized programs generated by RISC-V DV https://github.com/chipsalliance/riscv-dv
- UVM testbench with configurable sequences for constrained randomised stimulus
  - Instruction and data memory
  - Interrupts and debug requests
- Co-simulation with Spike ISS for checking
  - Includes checking of all data memory accesses
- Functional coverage divided into two
  - **Architectural coverage** Instructions executed and different cases of those instructions
  - **Micro-architectural coverage**
    - Specific Ibex behaviour, such as stalls and hazards
    - Doesn't look at specific instructions, but instruction *categories* (Such as ALU or memory)
    - Cross coverage for combinations
    - PMP configurations and behaviour including corner cases
- Test plan specifying tests focussed on different scenarios enabling us to achieve full code coverage and functional coverage
- Directed tests used for hard to hit scenarios (mostly PMP related)

Current Status and Nightly Regression

- Regular regressions run by lowRISC
- Vital to demonstrate project health and life
- Monitored with failures triaged and fixed
- A key part of Silicon Commons working practices
- https://ibex.reports.lowrisc.org/opentitan/latest/report.html

Total	1288	1380	93.3%

Coverage

Functional	Block	Branch	Statement	Expression	Toggle	FSM	Assertion
93.6%	94.6%	90.5%	94.6%	91.4%	97.1%	100.0%	98.1%

Test Failure Details

```
riscv_rand_jump_test.2585
-------------------------
binary:          test.bin
rtl_log:         rtl_sim.log
rtl_trace:       trace_core_00000000.log
iss_cosim_trace: spike_cosim_trace_core_00000000.log
[FAILURE] Simulation ended gracefully due to timeout [1800s].
---------------*LOG-EXTRACT*---------------
    101: UVM_INFO /home/azure/_work/1/s/ibex/dv/uvm/core_ibex/tests/core_ibex_base_test.sv(315) @ 20
    102: UVM_INFO /home/azure/_work/1/s/ibex/dv/uvm/core_ibex/common/ibex_mem_intf_agent/ibex_mem_int
    103: UVM_INFO /home/azure/_work/1/s/ibex/dv/uvm/core_ibex/common/ibex_mem_intf_agent/ibex_mem_int
    104: UVM_INFO /home/azure/_work/1/s/ibex/dv/uvm/core_ibex/tests/core_ibex_new_seq_lib.sv(65) @ 2(
    105: core_ibex_tb_top.dut.u_ibex_tracer.printbuffer_dumpline.unmblk1: Writing execution trace to
[E] 106: UVM_FATAL /home/azure/_work/1/s/ibex/dv/uvm/core_ibex/tests/core_ibex_base_test.sv(326) @ 2(
    107:
    108: --- RISC-V UVM TEST FAILED ---
    109:
    110: UVM_INFO /nas/lowrisc/tools/cadence/xcelium/21.09-s006/tools/methodology/UVM/CDNS-1.2/sv/sr
-----------------------------------------------
```

Ibex Regression Results

Date/Time run: Thursday 25 May 2023 04:10 UTC

Git Commit: a31c043

Test Name	Passing	Total	Pass Rate
riscv_arithmetic_basic_test	10	10	100.0%
riscv_machine_mode_rand_test	10	10	100.0%
riscv_rand_instr_test	10	10	100.0%
riscv_rand_jump_test	9	10	90.0%
riscv_jump_stress_test	10	10	100.0%
riscv_loop_test	10	10	100.0%
riscv_mmu_stress_test	9	10	90.0%
riscv_illegal_instr_test	15	15	100.0%
riscv_hint_instr_test	10	10	100.0%
riscv_ebreak_test	10	10	100.0%
riscv_debug_basic_test	9	10	90.0%
riscv_debug_triggers_test	4	5	80.0%
riscv_debug_stress_test	15	15	100.0%
riscv_debug_branch_jump_test	7	10	70.0%
riscv_debug_instr_test	24	25	96.0%
riscv_debug_wfi_test	10	10	100.0%
riscv_dret_test	3	5	60.0%
riscv_debug_ebreak_test	14	15	93.3%
riscv_debug_ebreakmu_test	11	15	73.3%
riscv_debug_sca_entry_test	10	10	100.0%

Free Fully-Verified IP? Fantastic!

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Yes - but there's more to it

Why Open Source?

- It's a mistake to just see it as 'Free IP', it's a different development model with distinct advantages
- Tweakable and customizable, can close DV rapidly on modified design provided existing testbench and collateral, like test plans and coverage plans, are open too
- Multiple contributing partners can build a better design with less resource compared to doing it all in-house
- No commercial pressure to gate-keep improvements behind yearly releases
- Freedom to configure as you want, no marketing and sales need for lots of model numbers and bundled features
  - It's not Ibex-A478-S or Ibex-A480-B, just Ibex, with many possibilities
- Contributing partners are vital, open source isn't free!
- Using Ibex already? Interested in supporting our work or helping drive development?
  - Get in touch - info@lowrisc.org

Thank you

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