

# Proteus

An Extensible RISC-V Core for Hardware Extensions

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WiP

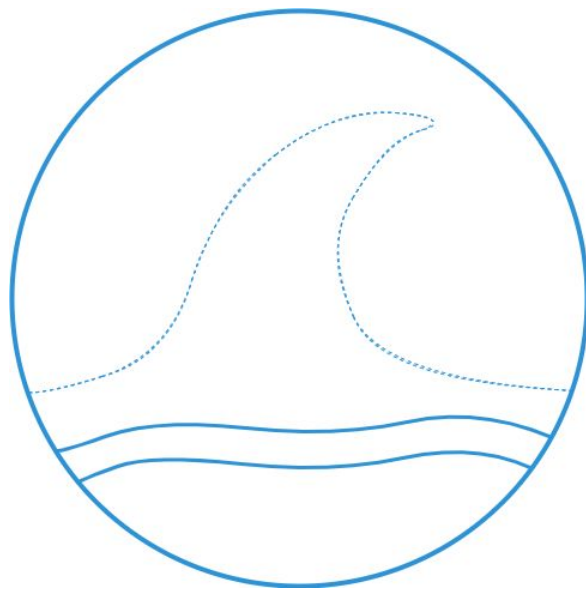
# RISC-V

- Easy-to-extend ISA
  - New instructions
  - New control and status registers
  - Also official extensions: SIMD, vector operations, hypervisor, ...
- Let's build easy-to-extend hardware as well!

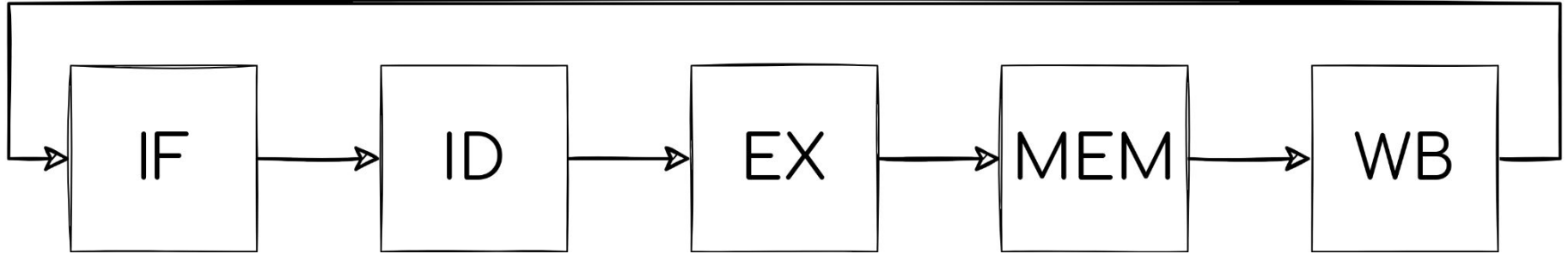


# Proteus

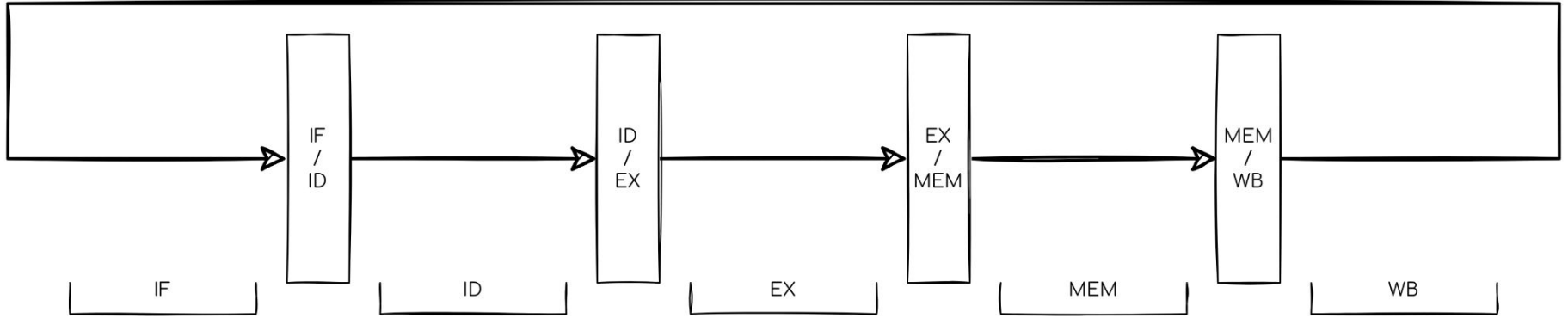
- Free and open-source RISC-V softcore
- Focus on extensibility, ease of development
- Written in SpinalHDL
- Based on a plugin system (💕 VexRiscv)
- Implementing RV32IM + Zicsr
- Comes with two implementations
  - In-order pipeline
  - Out-of-order pipeline
- Both passing the official RISC-V unit tests
- Newlib board support package



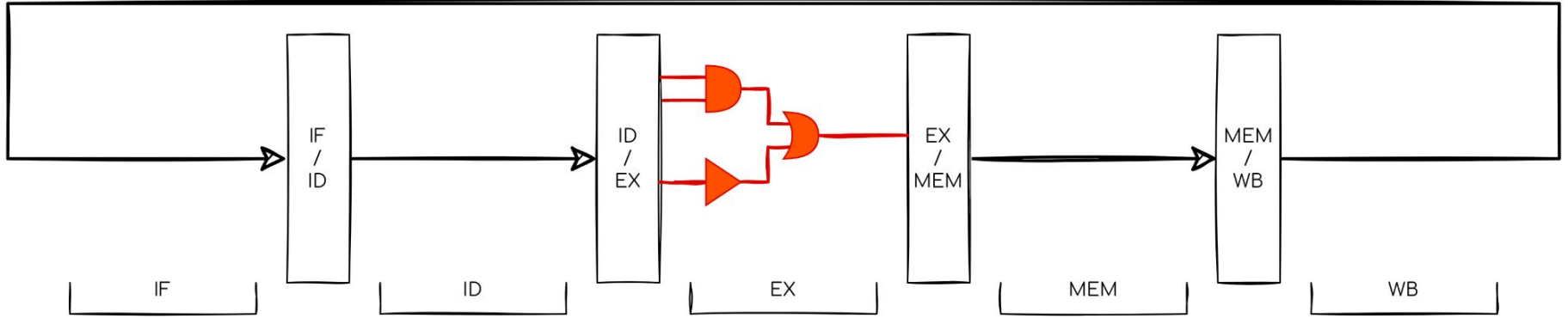
# In-order pipeline



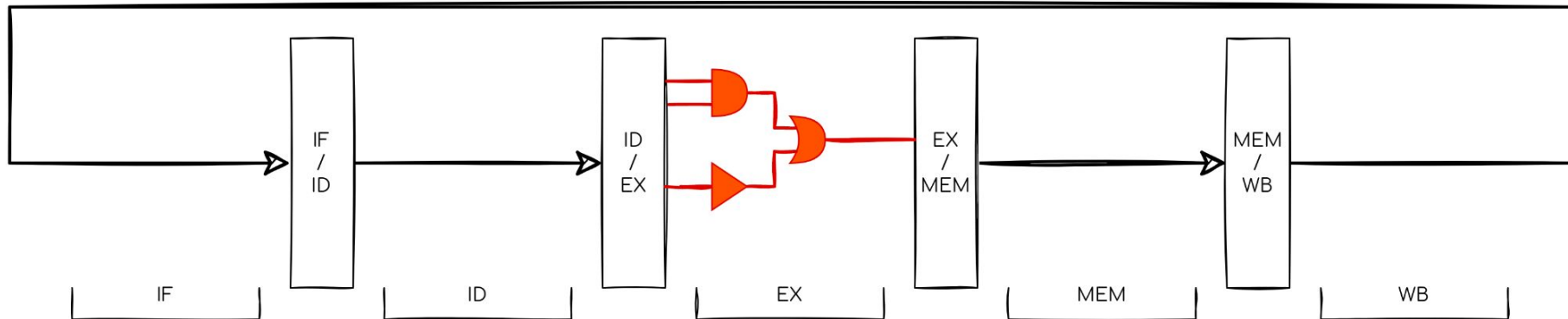
# In-order pipeline



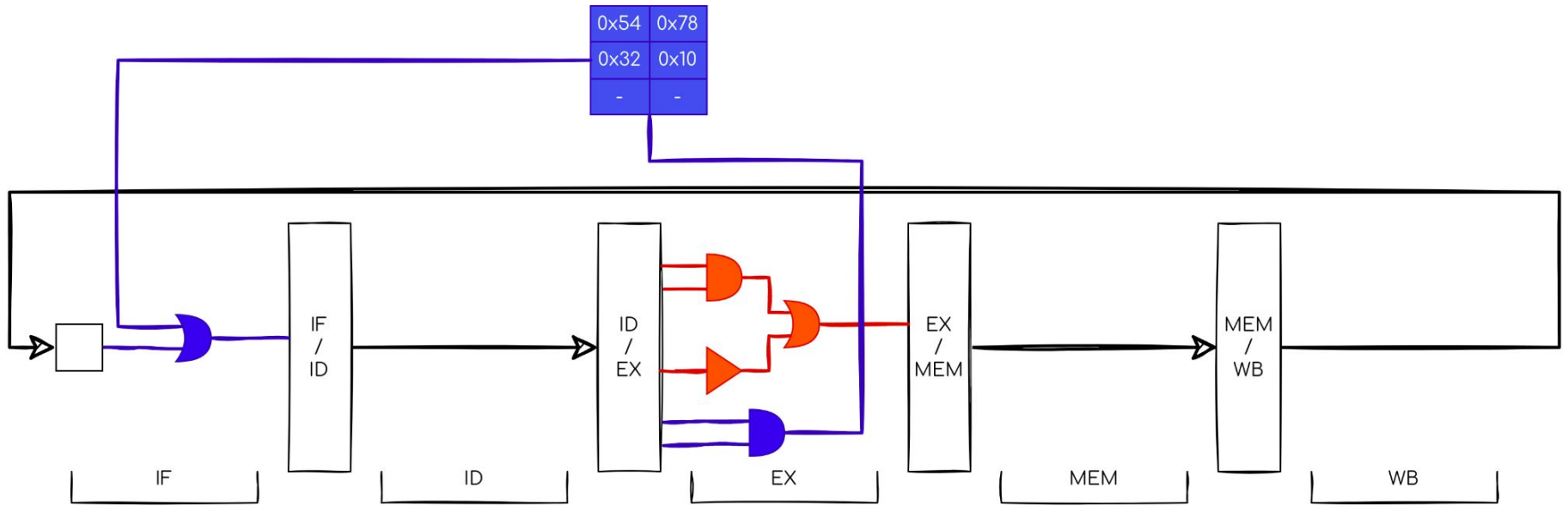
# In-order pipeline + plugins



# In-order pipeline + plugins



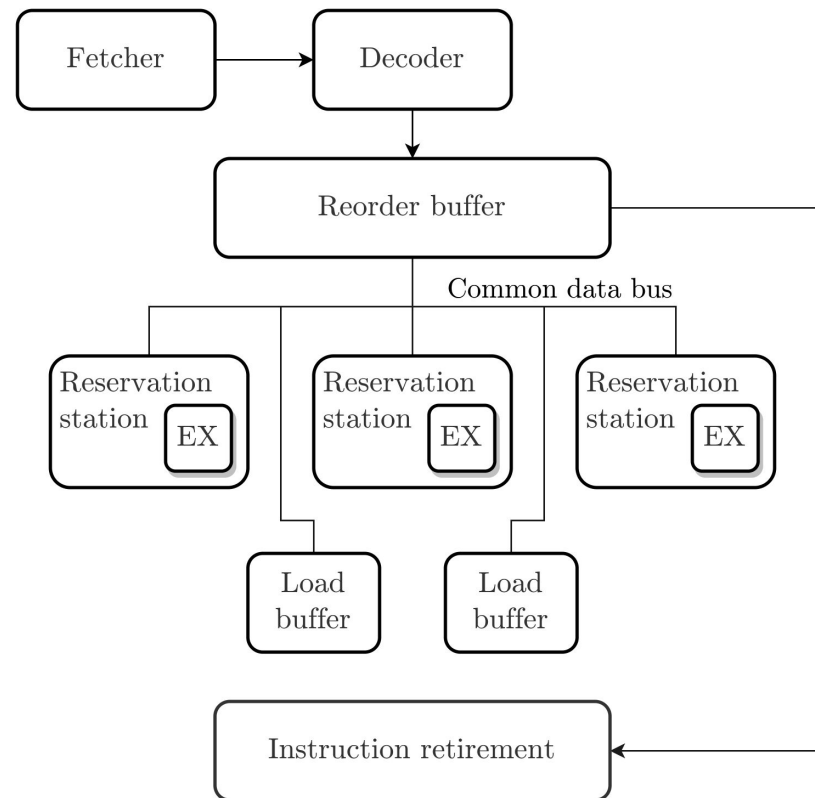
```
val op = input(Data.ALU_OP)
switch(op) {
  is (AluOp.SUB) {
    result := src1 - src2
  }
}
when (input(Data.ALU_COMMIT_RESULT)) {
  output(pipeline.data.RD_DATA) := result
  output(pipeline.data.RD_DATA_VALID) := True
}
```





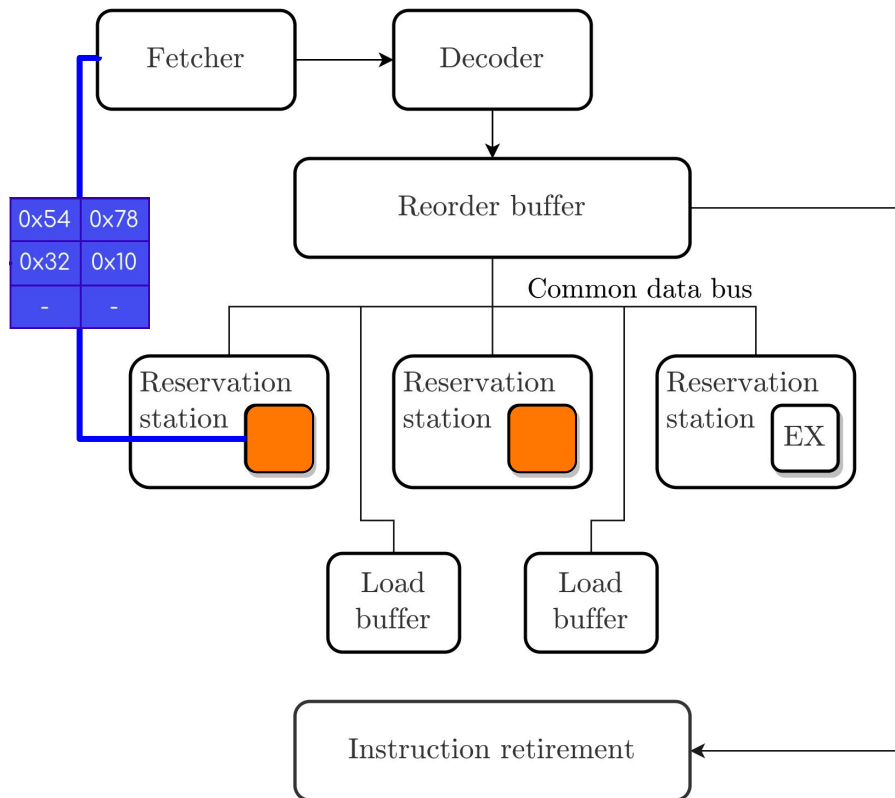
# Out-of-order pipeline

- Tomasulo's algorithm
- Textbook implementation, but close to real hardware
- Reusing many of the in-order plugins
- Configurable
  - Number of reorder buffer entries
  - Number of reservation stations
  - Types of execution units
  - Branch predictor

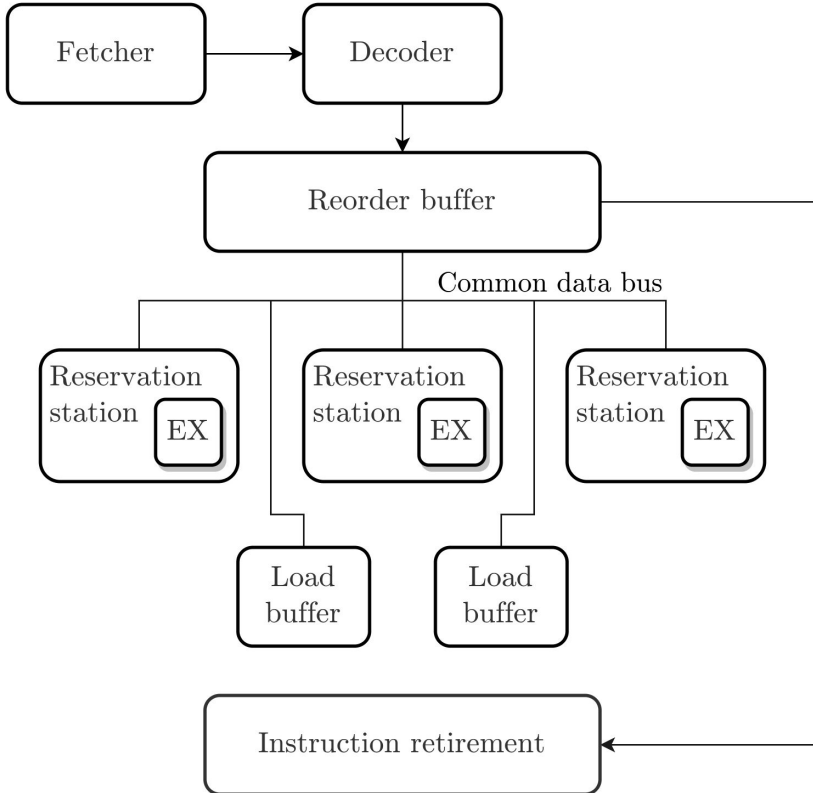
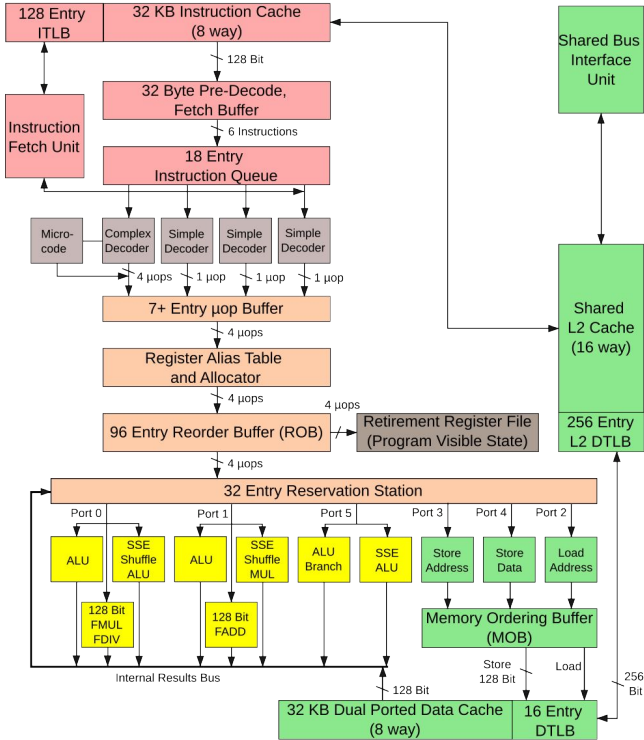


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# Real-world relevance



Intel Core 2 Architecture

[https://commons.wikimedia.org/wiki/File:Intel\\_Core2\\_arch.svg](https://commons.wikimedia.org/wiki/File:Intel_Core2_arch.svg)

# Extensions

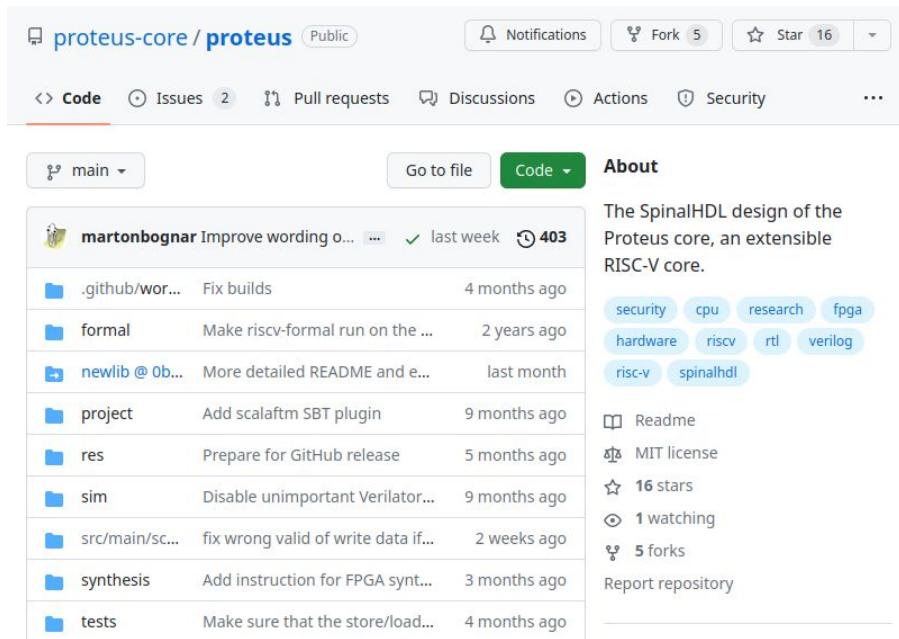
- Swapping out certain plugins:
  - New branch prediction algorithm
- Writing new plugins, adding extra functionality:
  - In-order pipeline: CHERI, CHERI-TrEE (hardware capabilities)
  - Out-of-order pipeline: ProSpeCT (secure speculation) → See ORSHIN talk on Friday!
  - Non-security proposals
- Future work:
  - Improving the modularity of the out-of-order pipeline → Gaining more experience!
  - Experimenting with performance, optimizing for FPGA/ASIC
  - Booting Linux

# Get involved!

<https://github.com/proteus-core>

- Docker playground
- RISC-V unit tests
- Synthesis instructions
- Newlib BSP
- Example code
- Extensions

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The screenshot shows the GitHub repository page for `proteus-core / proteus`. The repository is public and has 5 forks and 16 stars. The main branch is selected. The repository description is "The SpinalHDL design of the Proteus core, an extensible RISC-V core." The repository includes several tags: `security`, `cpu`, `research`, `fpga`, `hardware`, `riscv`, `rti`, `verilog`, `risc-v`, and `spinalhdl`. The repository also has a README, MIT license, 16 stars, 1 watching, and 5 forks.

| File/Folder                    | Description                         | Last Commit  |
|--------------------------------|-------------------------------------|--------------|
| <code>.github/workflows</code> | Fix builds                          | 4 months ago |
| <code>formal</code>            | Make riscv-formal run on the ...    | 2 years ago  |
| <code>newlib @ 0b...</code>    | More detailed README and e...       | last month   |
| <code>project</code>           | Add scalafm SBT plugin              | 9 months ago |
| <code>res</code>               | Prepare for GitHub release          | 5 months ago |
| <code>sim</code>               | Disable unimportant Verilator...    | 9 months ago |
| <code>src/main/sc...</code>    | fix wrong valid of write data if... | 2 weeks ago  |
| <code>synthesis</code>         | Add instruction for FPGA synt...    | 3 months ago |
| <code>tests</code>             | Make sure that the store/load...    | 4 months ago |