GreenRio: A Linux-Compatible RISC-V Processor Designed for Open-Source EDA Implementations

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RISC-V International open-source Laboratory

Outline

- Background and Motivation
- GreenRio Development History
- User Experience of Open Toolchains
- Design Space Exploration in RISC-V Chips and OpenEDA

Background

Over 20 years ago..

Designing a 3GHz, 130nm, Intel ® Pentium® 4 Processor

Daniel Deleganes, Jonathan Douglas, Badari Kommandur, Marek Patyra
Intel Architecture Group
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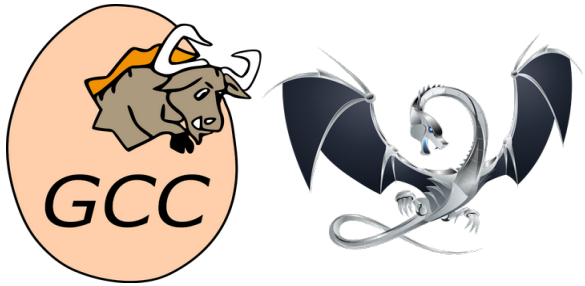
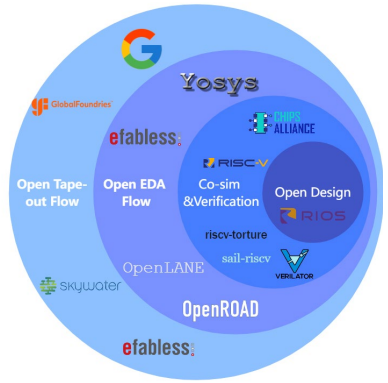
- Increasing complexity of IC design leads to high demand on EDA flow
- Traditional fabrication methods Vs Open source toolchains and open PDKs
- Open source projects prevent EDA licenses' limitations

software industry → hardware landscape





Motivation

- Few designs are developed with open fabrication flow
- Existing open chips are too simple to push the boundary of open EDA toolchains

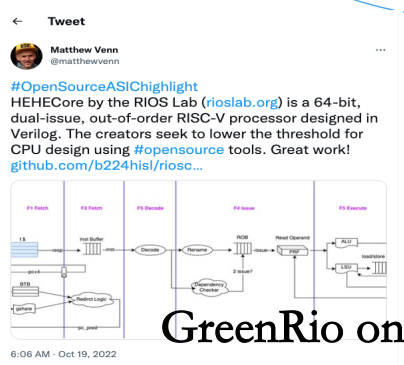
Current RISC-V cores serving as example designs in the OpenEDA repository:

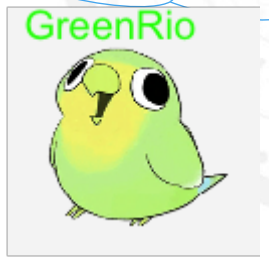
Design	EH1	IBEX	Count	biriscv	GreenRio1.0	GreenRio2.0
Properties	RV32	RV32	RV32	RV32	RV64	RV64
Pipeline stage	6	2 or 3	2 or 3	6 or 7	7	7
Issue Width	single	single	single	dual	dual	dual
Out-of-Order	✓	×	×	×	✓	✓
Gate count (K)	17	10	20	67	60	250

Linux compatible

The most complex design among 600+ OpenMPW submissions

efabless.com
Sponsored by Google





GreenRio on Twitter

Motivation

Optimize the OpenEDA along with the RISC-V CPU together
& Put explorations in the flow at various stages

GreenRio:

1. Build a RISC-V processor from scratch that is fully compatible with the Open flow
2. Drive the growth of both chips and EDA tools through a real and reasonable design
3. Conduct researches in Open-Chip field through a meaningful and non-toy-like design instance
4. Facilitate chiplets and multi-physics through innovation in both fabrication flow and models

OpenEDA's iteration
RISC-V chip's development
→ Continued Semiconductor Innovation

back

GreenRio Development History

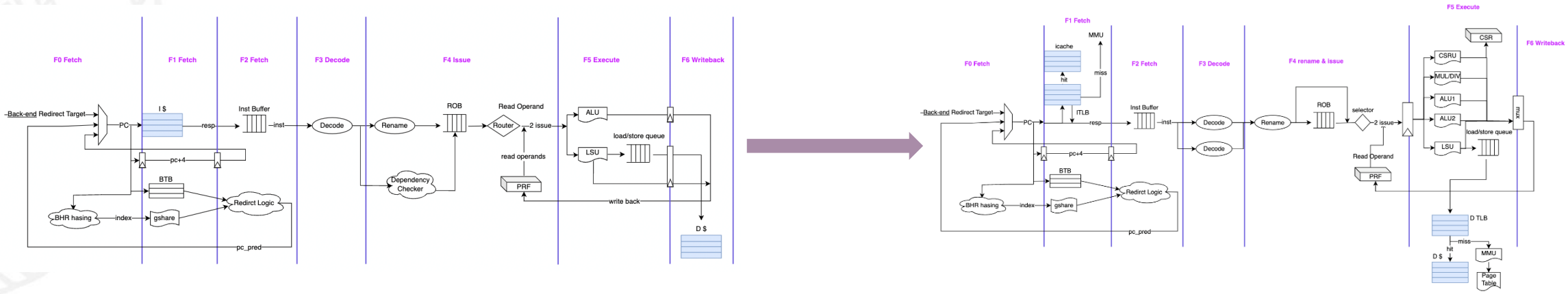
- With modern processors characteristics

GreenRio 1.0

RISC-V I extension | M mode | Dual issue | Register renaming | In-order issue & Out-of-order execution
Reorder Buffer | Precise exception | Branch prediction | Non-blocking data cache

GreenRio 2.0

RISC-V ICMA extension | U, S, and M mode | Dual issue | Register renaming | TSO memory model
Our-of-order issue & out-of-order execution | Reorder Buffer | Precise exception | Branch prediction
Non-blocking data cache | MMU with sv39 mode | Linux | Cache coherent



GreenRio Development History

- Milestone of Greenrio

GreenRio1.0

- Tape out in the OpenMPW-7 program, skywater 130nm process

- Related works are accepted by WOSET

WOSET 2022 Schedule

November 3, 2022

Papers 1

Time (PST)	Duration (Minutes)	Article #	Author(s)	Title
8:00 AM	20	12	Wijerathne, Li, Karunarathne, Mitra, Peh	Morpher: An Open-Source Integrated Compilation and Simulation Framework for CGRA
8:20 AM	20	20	Xu, Xiao, Luo, Liang	A MLIR-Based Hardware Synthesis Framework
8:40 AM	20	2	Euphrosine	Accelerate Silicon Design with Jupyter Notebooks
9:00 AM	20	10	Zhu, Yin, Wang, Tan	GreenRio: A Modern RISC-V Microprocessor Completely Designed with An Agile Open-source EDA Flow
9:20 AM	20	5	Goldstein, Edwards	Accessibility of Chip Design to the Non-Professional
9:40 AM	20	18	Liang, Edwards	IRSIM: A Switch-Level Simulator and Dynamic Power Analysis Tool

- Share the experience in RISC-V Days Tokyo 2022 Autumn

RISC-V Days Tokyo2022 Autumn

Nov. 16 (Wed.) – 18 (Fri.), 2022

RIOS and Google OpenEDA Team
@ Yokohama Japan, 11/2022

GreenRio Development History

GreenRio2.0

- Benchmark in the OpenEDA domain
- Inspire the RISC-V community and drive growth for open-source semiconductor fabrication
  GreenRio1: https://github.com/b224hisl/rioschip
  GreenRio2: https://github.com/0616ygh/GreenRio2
- Future Work:
  Enhance the performance and scalability of GreenRio while further optimizing EDA tools

IEEE SSCS Open-Source Ecosystem "Code-a-Chip" Travel Grant Awards at ISSCC'23

List of Accepted Notebooks:

Name	Affiliation	Notebook Title
Yihai Zhang	Tsinghua-Berkeley Shenzhen Institute, Tsinghua University China	GreenRio 2: A Linux-compatible RISC-V Processor Developed with A Fully Open-Source EDA Flow
Anawin Opasatian	University of Tokyo (Japan)	Bernstein-Yang Modular Inversion with XLS/OpenLane
Mauricio Montanares	University of Concepción (Chile)	Sonar On Chip Project
Nealson Li	Georgia Institute of Technology (USA)	Coordinate Rotation Digital Computer (CORDIC) with OpenLane
HyungJoo Park	Hanyang University (South Korea)	Scan Register layout generation using laygo2
Ali Hammoud	University of Michigan (USA)	OpenFASoC: Digital LDO Generator
Nimish Shah	KU Leuven (Belgium)	DPU: DAG Processing Unit for probabilistic ML and sparse matrix algebra

Note: Many thanks everyone for your participation! We recommend to resubmit your Notebooks to the next code-a-chip Notebook competition with revisions. Stay tuned!

The International Solid-State Circuits Conference (ISSCC) 2023 Code-a-Chip Travel Grant Award is created to:

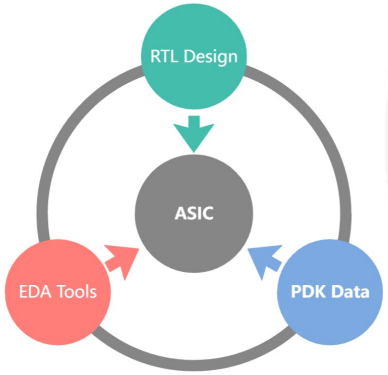
1. Promote *reproducible* chip design using *open-source* tools and *notebook-driven* design flows and
2. Enable up-and-coming *talents* as well as seasoned *open-source enthusiasts* to travel to the Conference and interact with the leading-edge chip design community.

back

User Experience of Open Toolchains

Focus: the gap between open and proprietary EDA tools in terms of quality of results (QoR)

- Open-source backend EDA tools
  - OpenLane: An automated flow performing full ASIC implementation
  - OpenRoad: Enable no-human-in-loop, 24-hour design to remove the barrier to hardware innovation
- Open-source PDK
  - Skywater 130nm (Sky130A & Sky130B)
- Open-source external IP
  - SRAM blocks compiled by OpenRAM
- Open-source silicon production
  - Open Multi Project Wafer (OpenMPW)
  - Efabless Chipignite



User Experience of Open Toolchains

What is missing?

About the open PDK

1. Sky130A techlef lack cut layer

sky130A techlef lack cut layer

```
LAYER poly
    TYPE MASTERSLICE ;
END poly

LAYER licon1
  TYPE CUT ;

  WIDTH 0.17 ;                # Licon 1
  SPACING 0.17 ;              # Licon 2
  ENCLOSURE BELOW 0 0 ;       # Licon 4
  ENCLOSURE ABOVE 0.08 0.08 ; # Poly / Met1 4 / Met1 5
END licon1
```

2. Open lib is not complete enough

lib in 40C has the richest cases:

```
(base) [yzhu@server1 lib]$ls sky130_fd_sc_hd__*_n40C*
sky130_fd_sc_hd__ff_n40C_1v56.lib          sky130_fd_sc_hd__ff_n40C_1v95.lib  sky130_fd_sc_hd__ss_n40C_1v44.lib
sky130_fd_sc_hd__ff_n40C_1v65.lib          sky130_fd_sc_hd__ss_n40C_1v28.lib  sky130_fd_sc_hd__ss_n40C_1v60_ccsnoise.lib
sky130_fd_sc_hd__ff_n40C_1v76.lib          sky130_fd_sc_hd__ss_n40C_1v35.lib  sky130_fd_sc_hd__ss_n40C_1v60.lib
sky130_fd_sc_hd__ff_n40C_1v95_ccsnoise.lib sky130_fd_sc_hd__ss_n40C_1v40.lib  sky130_fd_sc_hd__ss_n40C_1v76.lib
```

lib in 25C only has one case

```
(base) [yzhu@server1 lib]$ls *25C*
sky130_fd_sc_hd__tt_025C_1v80.lib
```

- slow lib set for setup time analysis
- fast lib set for hold time analysis

3. Lack capacitance table and qrctech file
   - RC scaling factor
   - ICT file for em_module

Correspodning to Innovus/ICC's MMMC file:
simultaneously analyzes and optimizes the time sequence of all views, and selectively optimizes the area and power consumption

4. Missing 'pg_pin' on level shifter cells

```
**ERROR: (TECHLIB-702): No pg_pin with name 'VNB' has been read in the cell 'sky130_fd_sc_hd__lpflow_lsbuf_lh_hl_isowell_tap_1'. The attribute 'related_bias_p
specified for the pg_pin 'VGND' is being ignored. (File /work/stu/yzhu/OpenROAD-flow-scripts/flow/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/
sky130_fd_sc_hd__tt_025C_1v80.lib, Line 82148)
**ERROR: (TECHLIB-702): No pg_pin with name 'VNB' has been read in the cell 'sky130_fd_sc_hd__lpflow_lsbuf_lh_hl_isowell_tap_2'. The attribute 'related_bias_p
specified for the pg_pin 'VGND' is being ignored. (File /work/stu/yzhu/OpenROAD-flow-scripts/flow/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/
sky130_fd_sc_hd__tt_025C_1v80.lib, Line 82282)
**ERROR: (TECHLIB-702): No pg_pin with name 'VNB' has been read in the cell 'sky130_fd_sc_hd__lpflow_lsbuf_lh_hl_isowell_tap_4'. The attribute 'related_bias_p
specified for the pg_pin 'VGND' is being ignored. (File /work/stu/yzhu/OpenROAD-flow-scripts/flow/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/
sky130_fd_sc_hd__tt_025C_1v80.lib, Line 82416)
**ERROR: (TECHLIB-702): No pg_pin with name 'VNB' has been read in the cell 'sky130_fd_sc_hd__lpflow_lsbuf_lh_isowell_tap_1'. The attribute 'related_bias_pin'
specified for the pg_pin 'VGND' is being ignored. (File /work/stu/yzhu/OpenROAD-flow-scripts/flow/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/
sky130_fd_sc_hd__tt_025C_1v80.lib, Line 82693)
**ERROR: (TECHLIB-702): No pg_pin with name 'VNB' has been read in the cell 'sky130_fd_sc_hd__lpflow_lsbuf_lh_isowell_tap_2'. The attribute 'related_bias_pin'
specified for the pg_pin 'VGND' is being ignored. (File /work/stu/yzhu/OpenROAD-flow-scripts/flow/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/
sky130_fd_sc_hd__tt_025C_1v80.lib, Line 82827)
**ERROR: (TECHLIB-702): No pg_pin with name 'VNB' has been read in the cell 'sky130_fd_sc_hd__lpflow_lsbuf_lh_isowell_tap_4'. The attribute 'related_bias_pin'
specified for the pg_pin 'VGND' is being ignored. (File /work/stu/yzhu/OpenROAD-flow-scripts/flow/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/
sky130_fd_sc_hd__tt_025C_1v80.lib, Line 82961)
```

User Experience of Open Toolchains

About the toolchain itself

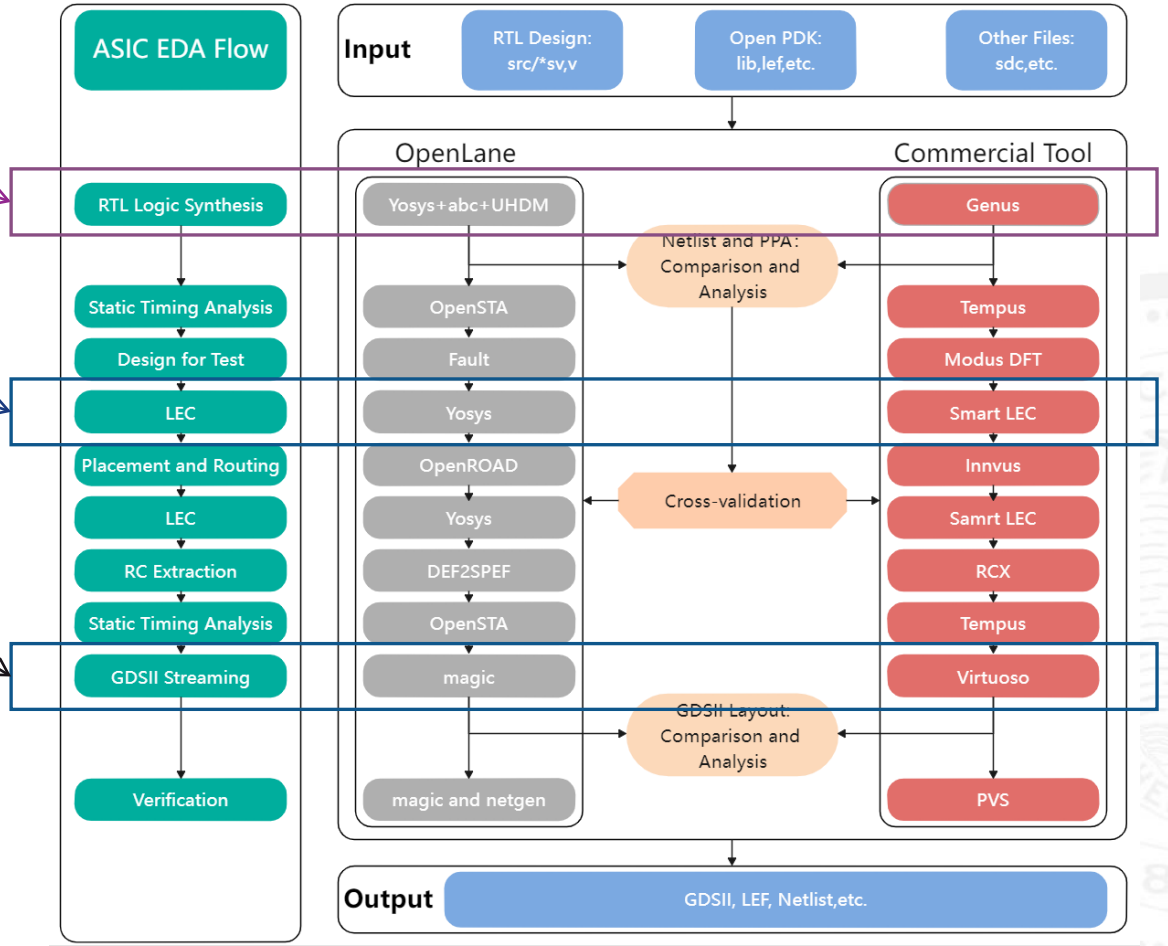
1. Complete support for System Verilog
   - Prevent extensive ip usage
2. Logic equivalence check (LEC) & Error checking
   - Don’ t do checking at the last stage

```
Presto compilation completed successfully. (rvj1_caravel_soc)
Error: Width mismatch on port 'cpu2dmux_we' of reference to 'rvj1_caravel_soc' in 'top'. (LINK-3)
Information: Building the design 'core_empty'. (HDL-193)
Presto compilation completed successfully. (core_empty)
Error: Width mismatch on port 'meip' of reference to 'core_empty' in 'top'. (LINK-3)
Information: Building the design 'l1icache_32' instantiated from design 'top' with
    the parameters "VIRTUAL_ADDR_LEN=32,WB_DATA_LEN=32". (HDL-193)
```

3. Engineering Change Order (ECO)
   - Adjust the netlist after the RTL is freezing
4. Multi-thread acceleration
   - Only routing stage can use multiple cores
5. Optimation algorithms
   - Advanced algorithm integration into OpenEDA
   - better timing/area, higher density,...
6. Online user guide

```
innovus 1> man TECHLIB-702
TECHLIB-702(20.15)                                  TECHLIB-702(20.15)


NAME
       TECHLIB-702 (error)

SUMMARY
       No  pg_pin with name '%s' has been read in the cell '%s'. The attribute
       '%s' specified for the %s '%s' is being ignored.

DESCRIPTION
       This   message   is   issued   when   the   pg_pin   specified   with
       related_power_pin/related_ground_pin/related_bias_pin does not exist at
       cell level. These attributes will be ignored. To  fix  the  issue,  re-
       characterize the library with appropriate settings, such that the unde-
       fined pg_pin is not used.


                                                    TECHLIB-702(20.15)
```

What is missing?



User Experience of Open Toolchains

We utilized the proprietary tools and OpenLane/OpenRoad in the sign-off flow of GreenRio

QoR and Runtime

Logic Synthesis

Comparison: Open vs Proprietary

https://github.com/YosysHQ/yosys
https://github.com/berkeley-abc/abc

GreenRio 1.0: Skywater 130nm, 80MHz
Sram Macro: sky130_sram_1kbyte_1rw1r_32x256_8
Without mult-core acceleration

SYNTH_STRATEGY	Strategies for abc logic synthesis and technology mapping Possible values are `DELAY/AREA 0-4/0-3`; the first part refers to the optimization target of the synthesis strategy (area vs. delay) and the second one is an index. (Default: `AREA 0`)

Tool/Features	Runtime(s)	Synthesis Strategy	Gate Count	Gap	Cell Area (mm²)	TNS	WNS	Leakage Power (nW)	Internal Power (W)	Clock Gating Optimization
Open	435	ABC: DELAY 4	50226	1.69	0.57	0.00	0.00	215.00	0.04	Null
	611	ABC: DELAY 3	53136	1.79	0.60	-4.68	-0.38	217.00	0.05	
	529	ABC: DELAY 2	53982	1.82	0.61	-2.76	-0.15	219.00	0.04	
	544	ABC: DELAY 1	54379	1.83	0.61	-0.33	-0.33	219.00	0.04	
	202	ABC: DELAY 0	52421	1.77	0.60	-4.72	-0.35	217.00	0.04	
	219	ABC: AREA 3	61749	2.08	0.63	0.00	0.00	239.00	0.04	
	910	ABC: AREA 2	50626	1.70	0.56	-260.60	-2.28	208.00	0.04	
	685	ABC: AREA 1	50904	1.71	0.56	-207.37	-1.78	210.00	0.04	
	334	ABC: AREA 0	48496	1.64	0.54	-125.13	-2.21	208.00	0.04	
Proprietary	543	SYN_EFF low MAP_EFF low OPT_EFF low	29657	1.00	0.30	-65.40	-1.65	130.82	0.03	Yes (sky130_fd_sc_hd__sdlclkp_1)

default

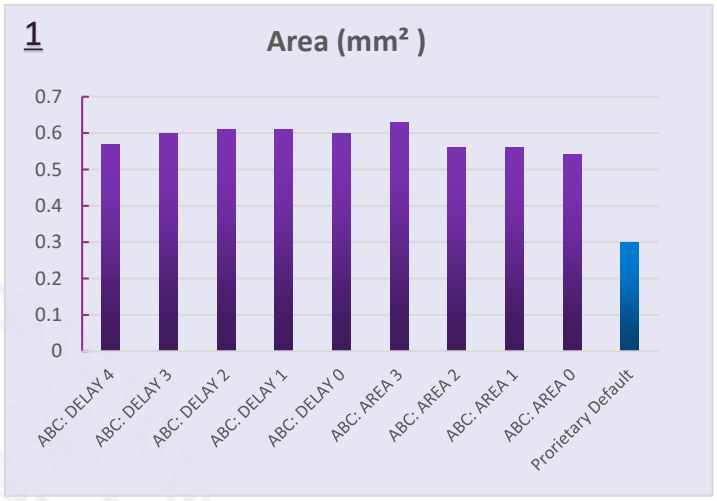
User Experience of Open Toolchains

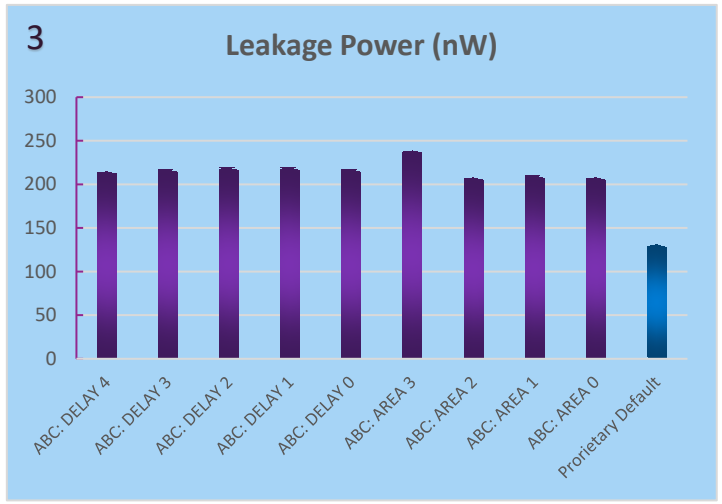
RIOS

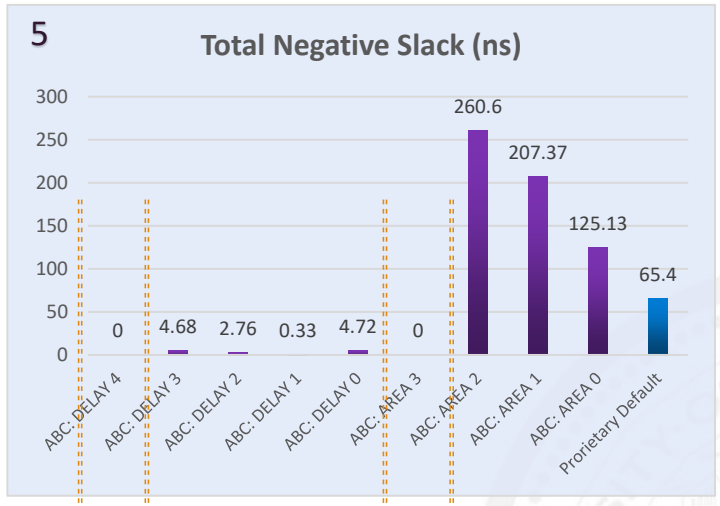
Logic Synthesis

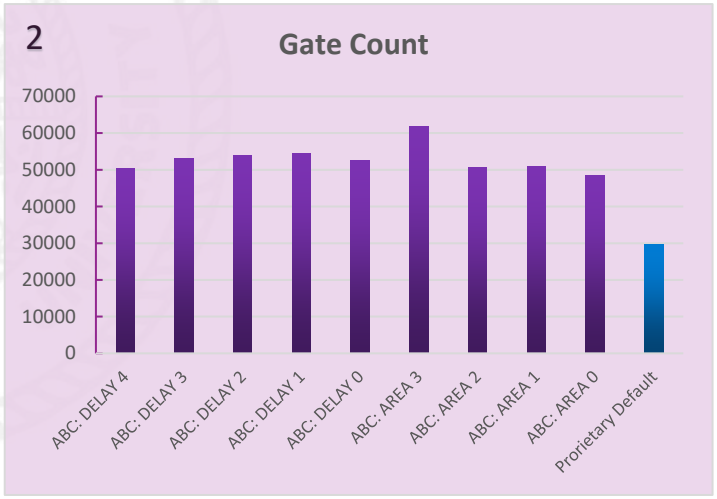
QoR and Runtime

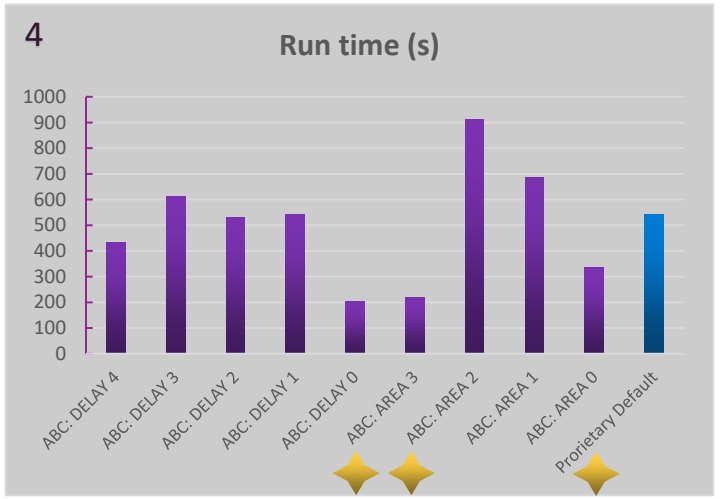
open > proprietary

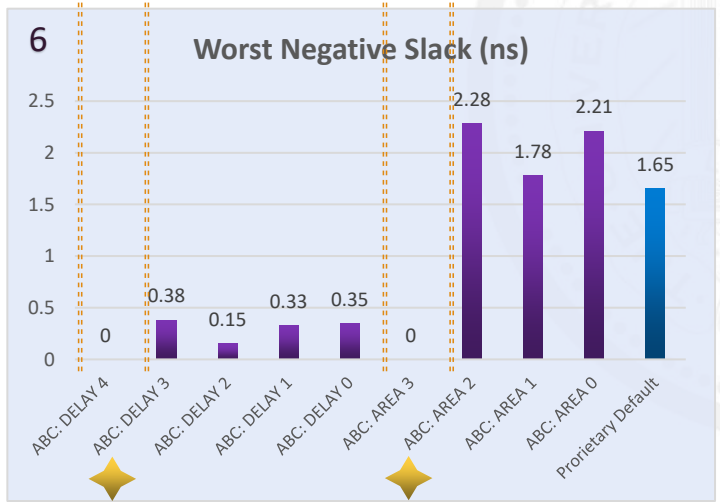












open < proprietary

User Experience of Open Toolchains

We utilized the proprietary tools and OpenLane/OpenRoad in the sign-off flow of GreenRio

QoR and Runtime

Physical Implementation

https://github.com/The-OpenROAD-Project/OpenROAD

Comparison: Open vs Proprietary

GreenRio 1.0: Netlist generated by Yosys
clean gds withou drc/lvs

- Harden the design with 1 core

Stages	Features	Open	Proprietary
Floorplan	Core Utiliation	0.35	0.35
	Area (mm2)	5.94	5.97
	Run Time (s)	93	64
Placement	Density	0.6	0.6
	Run Time (s)	385	2365
Clock Tree Synthesis	Run Time (s)	149	48
Routing	Wire Length (um)	3432810	2601926
	Run time (s)	8253	763
Total Runtime (h:min:s)		2:41:40	1:37:07

Gap: 0.75

- Do floorplan with higher utilation → can't fit all the cells

```
[INFO GPL-0020] StdInstsArea: 641853088000
[INFO GPL-0021] MacroInstsArea: 1528626000000
[ERROR GPL-0302] Use a higher -density or re-floorplan with a larger core area.
Given target density: 0.60
Suggested target density: 0.70
Error: global_place_skip_io.tcl, 30 GPL-0302
```

\	Proprietary
Core Utiliation	0.5
Area (mm^2)	4.18
Placement Time (s)	3195
Routing Time (s)	1558

- Higher density will easily lead to routing congestion

```
[INFO GRT-0111] Final number of vias: 214085
[INFO GRT-0112] Final usage 3D: 1023424
[ERROR GRT-0118] Routing congestion too high.
Error: groute.tcl, 69 GRT-0118
```

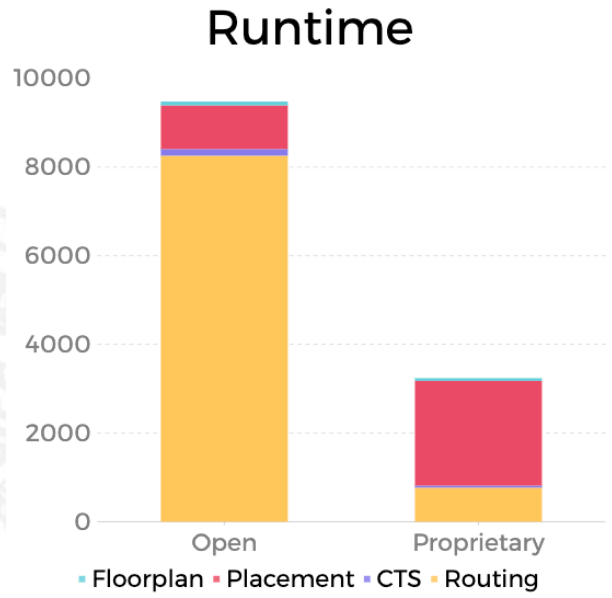
- Route with 8 cores

\	Open	Proprietary
Routing Time (s)	983 (x0.12)	127(x0.17)

OpenRoad has potential in mult-thread acceleration

User Experience of Open Toolchains

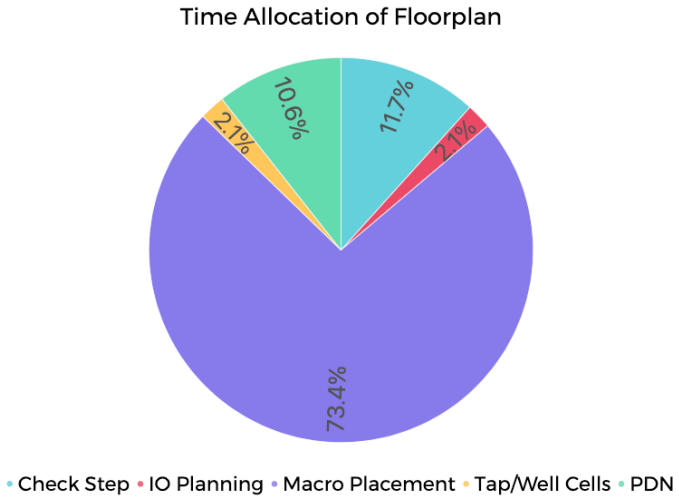
Physical Implementation

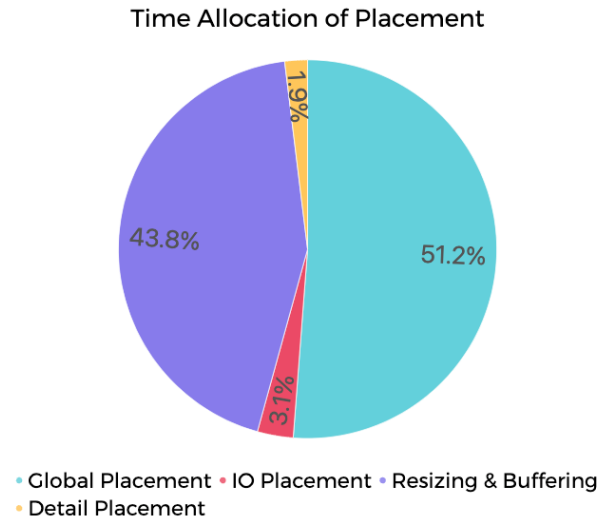


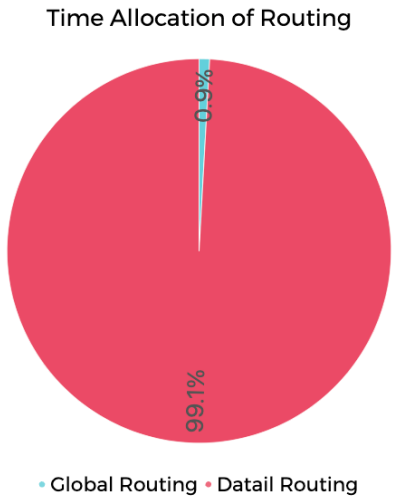
From proprietary tools:

A scientific placement may lead to easiler routing convergence

Runtime



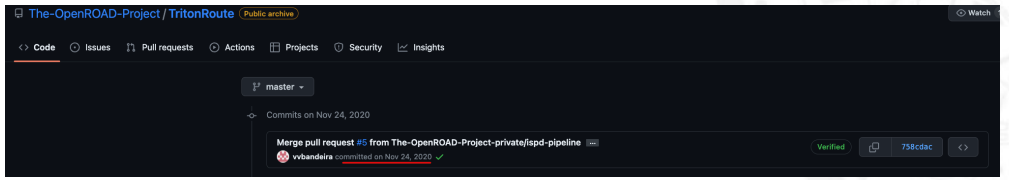




For open tools:

- Routing is the most time-consuming task

- Spend a lot of time on detail routing (TritonRoute)



- Determining the location of macro also costs much

User Experience of Open Toolchains

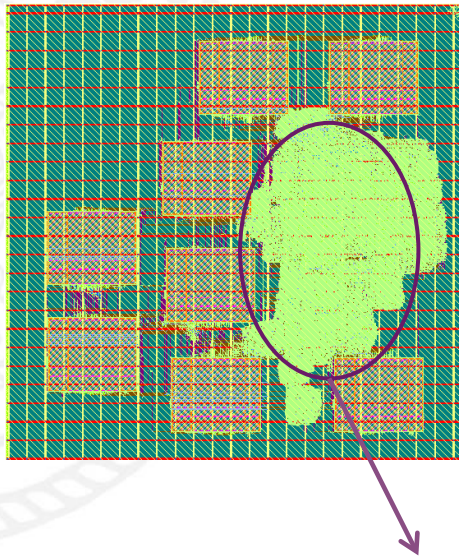
- Other Comparisons

  - Netlists don't contain module's hierarchical information

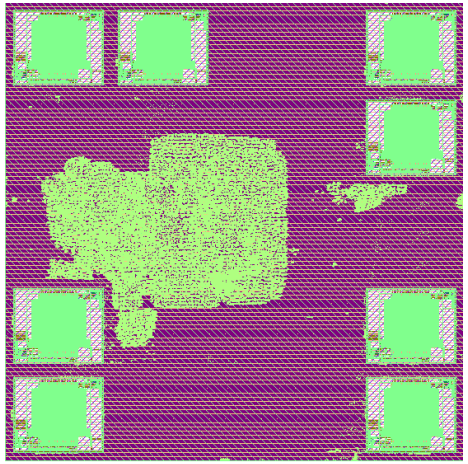
```
ERROR: Command syntax error: Unknown option or option in arguments.
> write_verilog -hierarchy
>                ^
ERROR: Command syntax error: Unknown option or option in arguments.
> write_verilog -hier
>                ^
```

  - Different macro placement

GDS generated by Innovus



GDS generated by OpenRoad

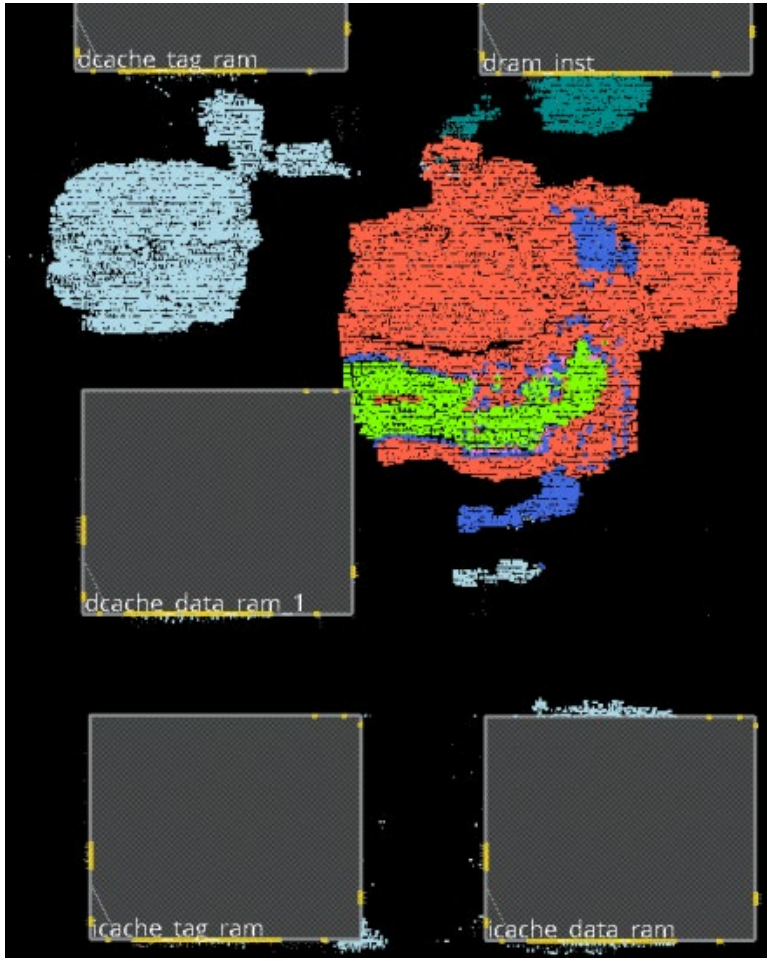


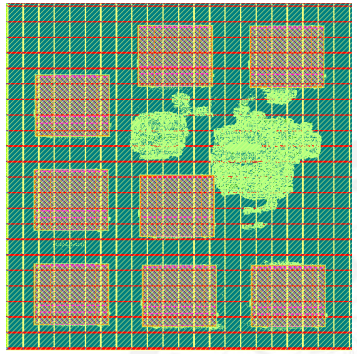
what happens here?

QoR

- Design brower

use the netlist generated by Synopsys Design Compiler (with hierarchical modules)





Nonblocking cache
CPU_backend
CPU_frontend
CSR
SOC

back

Design Space Exploration in RISC-V Chips and OpenEDA

- The design complexity of GreenRio has revealed the **convergence difficulty** in the Open-Chip flow

For Better area and timing and shorter wirelength

Integrate Flowtune[1] into OpenRoad

```
8.26.2. Analyzing design hierarchy..
8.27. Printing statistics.
8.28. Executing CHECK pass (checking for obvious problems).
ENTERING FLOWTUNE PROCESS
9. Executing BLIF backend.
10. Executing BLIF frontend.
11. Executing OPT pass (performing simple optimizations).
11.1. Executing OPT_EXPR pass (perform const folding).
```

Through this process, we also found the ASAP-7nm PDK is not complete enough

```
abc 01>       read /workspace/0penROAD-flow scripts/flow/results/asap7/gcd/base/output.blif
                Line 10: Cannot find gate "DFFHQNx1_ASAP7_75t_R" in the library. Reading network from file has failed.
```

For better user experience, especially for beginners:

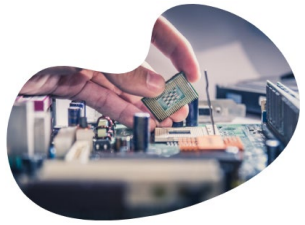
Bulid a solution-inspiring error log system

- Eg1 : fail in detail placement

```
[INFO DPL-0035]  _399_
[ERROR DPL-0036] Detailed placement failed.Maybe increasing the diea area or placement density,or changing placement strategy can solve this problem.
Error: detail_place.tcl, 10 DPL-0036
Command exited with non-zero status 1
Elapsed time: 0:09.70[h:]min:sec. CPU time: user 9.67 sys 0.02 (99%). Peak memory: 101656KB.
```

- Eg2 : fail in global routing

```
[INFO GRT-0101] Running extra iterations to remove overflow.
[INFO GRT-0103] Extra Run for hard benchmark.
[INFO GRT-0197] Via related to pin nodes: 1080
[INFO GRT-0198] Via related Steiner nodes: 57
[INFO GRT-0199] Via filling finished.
[INFO GRT-0111] Final number of vias: 2425
[INFO GRT-0112] Final usage 3D: 13527
[ERROR GRT-0118] Routing congestion too high. Decrease placement density or reduce bus widths maybe work. For more infomation, check the congestion heatmap
GRT-0118
```



Excellent Efford Award in OpenRoad 7nm Contest

[1] https://github.com/Yu-Utah/FlowTune

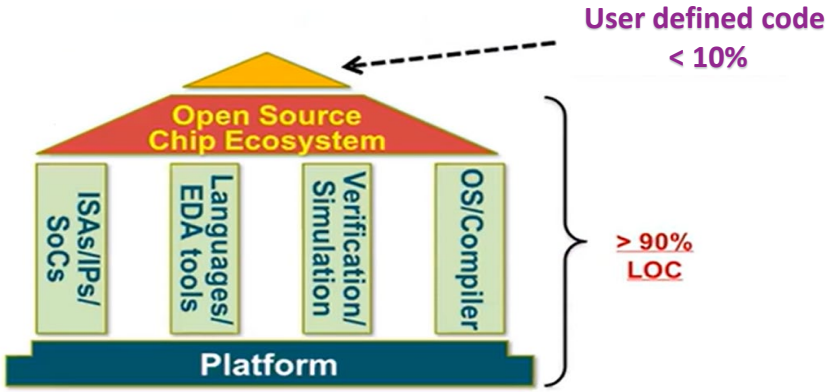
Design Space Exploration in RISC-V Chips and OpenEDA

- Optimize OpenEDA along with RISC-V Chips together

OpenEDA RISC-V

Complex Design -----> Boundary of tools

More advanced toolchain -----> Designs with more features



- ☐ Accelerate the customized chip development
- ☐ Leverage the power of open-source community
- ☐ Push the frontiers of hardware innovation

In future…

- Keep iterating GreenRio; Keep narrowing the gap between open and properitary backend softwares
- AI based ASIC
  - advanced algorithms
  - open-source data-set for RISC-V VLSI CAD

RIOS

Thank you