# Software Hardware Co-processing in RISC-V using OpenVX™ for Embedded Vision Applications

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## Introduction

Accelerating embedded computer vision applications using general purpose CPUs is very inefficient to meet real time criteria.

Certain computation intense portions of an algorithm can be offloaded to acceleration hardware like FPGAs.

Coprocessing some portions of algorithm in software(CPU) and some other in hardware remains a challenge due to lack of proper C function calling like techniques.

We present a novel methodology of wrapping an RTL IP into a C like function and is usable as a computational node in a bigger algorithm chain in OpenVX™ framework.

## Hardware-Software Interactions

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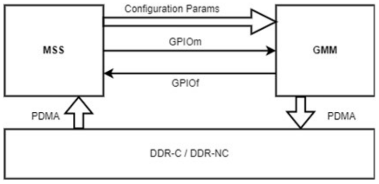


Fig 1: MSS and GMM interface

**MSS**

- MPFS250T PolarFire® SoC with 4 RISC-V U54
- Capable of running Linux®

**GMM**

- Generic Matrix Multiplier – An RTL IP to accelerate 2D convolutions

Mimicking a software function call

- Parameter configuration: A memory mapped region accessed thru *devmem* from Linux user space using APB interface.
- Control logic: MSS triggers and gets acknowledgments thru GPIO using *libgpiod*
- Data transfers: Using PDMA to transfer between DDR cached and non-cached regions

## GMM as OpenVX™ Node

A well-defined C interface can be a run function to a user defined node in OpenVX™ framework.

Conv2D user kernel with appropriate input/output validators and GMM as run function is coded in C.

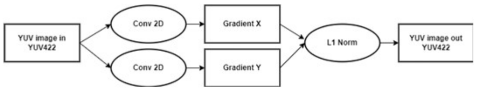


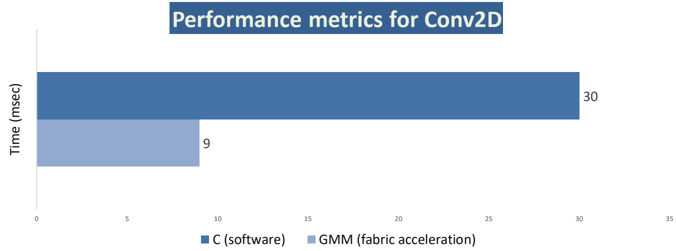
Fig 2: Sobel edge detector graph running in RISC-V with fabric coprocessing.

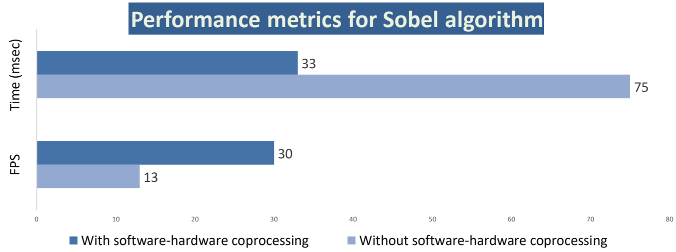
## Results

For HD (1280x720) resolution image the GMM takes about 9 msec to perform 2D convolution whereas the same in software i.e., in C it takes about 30 msec using four threads.

The L1 norm which is run in C takes about 15 msec.

Overall Sobel magnitude takes 33 msec (9+9+15) when the 2D convolution is performed using GMM and takes 75 msec (30+30+15) when the 2D convolution is performed in C.





## Conclusion

An unconventional approach of giving a C interface to fabric IP (GMM) and integrating it into OpenVX™ framework is realized.

This facilitates the reuse of FPGA IPs very identical to user space C libraries.

## Discussion

Complex use cases like stereo vision are better suitable for this approach.

For instance, the disparity estimation which involves lot of bitwise operations can be done in fabric and other computations on the processor.

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## References

1. https://www.khronos.org/openvx
2. M. Ali Altuncu, Taner Guven, Yasar Becerikli, Suhap Sahin, "Real-time system implementation for image processing with hardware/software co-design on the Xilinx Zynq platform", IJIEE, November 2015, 473-477
3. Wang Chong, et.al., "Hardware/software co-design of embedded image processing system using systemc modeling platform," 2011 International Conference on Image Analysis and Signal Processing, 2011, pp. 524-528
4. Adler, Felix et.al., "A new versatile hardware platform for digital real-time simulation: Verification and evaluation", 2012 IEEE 13th Workshop on COMPEL
5. https://www.microchip.com/en-us/developmenttool/MPFS250-VIDEO-KIT

**RISC-V Summit Europe 2023, 5-9 June 2023, Barcelona, Spain**