Falcon: A Dual-Core Lockstep Microprocessor Based on RISC-V ISA

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Abstract

Functional safety is a crucial consideration in the development of road vehicles. Microcontrollers (MCUs) that operate in high-safety automotive systems typically incorporate lockstep mechanisms to detect errors and enhance safety. In this study, we introduce Falcon, a dual-core lockstep automotive MCU that utilizes the RISC-V ISA. Falcon employs a lightweight, off-core-level Sphere of Replication (SoR) that necessitates minimal modifications to the original microarchitecture. It assesses certain critical signals of the primary and checker cores to identify possible soft errors while avoiding potential spatial-temporal coupling failures. The main core supports RV32IMAFDC with 6 execution units and is compatible with AHB/AXI interfaces. Falcon also incorporates an interrupt controller. This study demonstrates that RISC-V ISA-based MCUs can have a wide-ranging application space in the high-safety automotive processor field.

Introduction

With the development of the Internet of Things (IoT) and the increasing demand for embedded systems, microcontrollers (MCUs) have become an important component of many intelligent devices. In the automotive industry, MCUs are widely used in various control systems, such as engine control units, anti-lock braking systems, and airbag systems [1].

To meet the requirements of high reliability and safety in the automotive industry, microcontrollers need to have a lockstep architecture that can ensure the correctness of the program execution. A lockstep architecture can detect and correct errors by running two identical processor cores in parallel and comparing their outputs. This redundancy can provide a high degree of fault tolerance, making lockstep MCUs an ideal choice for safety-critical applications in the automotive industry [2].

Recently, RISC-V has emerged as a new open-source instruction set architecture (ISA) that offers flexibility, scalability, and extensibility. RISC-V MCUs are gaining popularity in various embedded systems due to their open architecture, low power consumption, and customizable features. However, the lack of mature lockstep solutions for RISC-V MCUs has limited their adoption in safety-critical applications.

To address this issue, we propose a lockstep RISC-V MCU Falcon, which is based on a dual-core architecture with a redundant level. Falcon is designed to meet the stringent requirements of automotive applications and provide high reliability and safety. In this paper, we present the design and implementation of Falcon and evaluate its performance through simulation and verification on an FPGA platform.

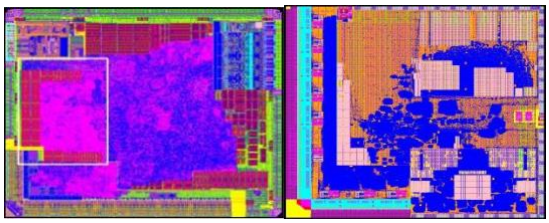

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Figure 1：Single-Core Development Roadmap. Figure 1-1 is the original single core. Figure 1-2 is the Dual core version with a Convolutional Neural Network Accelerator.

Proposed Implementation

Single-Core Microarchitecture

The single-core of Falcon is a 32-bit dual-issue in order RISC-V processor, which has been verified by SMIC40nm tape-out several times with various co-processors, as shown in Figure 1. It supports RV32IMAFDC instruction extensions, employs a 6-stage pipeline architecture, in-order dual-issue, branch prediction technology, and low-power design techniques. The internal microarchitecture integrates a memory management unit, a physical memory protection unit, and instruction and data cache units, and provides effective support for interrupts, debugging, off-chip memory, and peripherals. When using the AXI4 interface and DDR4 DRAM Devices, Falcon achieves a performance of 1.81 DMIPS/MHz in Dhrystone, 2.88 Coremark/MHz in Coremark, and 0.86 WMIPS/MHz in Whetstone, with a frequency of 600MHz. It supports 64 external interrupts, 1 timer interrupt, and 1 software interrupt. Both I-cache and D-cache are 32KB.

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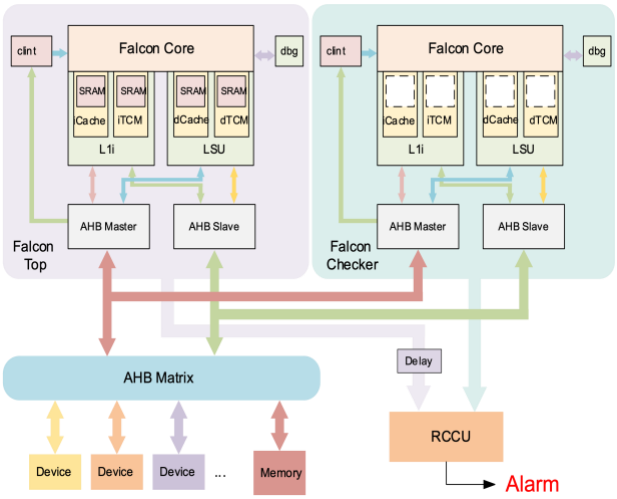

Figure 2: Illustration of Dual-Core Lockstep Microarchitecture.

Dual-Core Lockstep Microarchitecture

Building on the single-core microarchitecture, as shown in Figure 2, Falcon replaces the AXI4 interface with the AHB interface for compatibility with peripherals and adds 16KB Instruction Tightly Coupled Memory (ITCM) and 64KB Data Tightly Coupled Memory (DTCM) for the real-time requirements. Memory Management Unit (MMU) is not used considering the same requirements and its area budget.

In the Sphere of Replication (SoR) level of the dual-core lock-step structure [3], Falcon belongs to the off-core level, which only checks off-core signals to reduce the additional modifications to the original single-core microarchitecture. Therefore, the storage units of the checker core, such as SRAMs in I-cache, D-cache, ITCM, DTCM and the branch prediction unit, are removed and their relevant memory access signals such as address and data signals are compared. While the checker core starts running, all SRAM related data is responded from SRAM arrays of the main core. To eliminate common-cause failures, the inputs of the checker core are delayed by two cycles, and the outputs of the main core are also delayed by two cycles. Memory access related and other state control signals are compared by the Redundancy Control and Checker Unit (RCCU), and if inconsistency occurs, it is reported to the Interrupt Controller and handled through interrupt for error rollback and recovery, so that program context can be restored from the checkpoint stored in main memory by software. This procedure can cost at least hundreds of cycles. Table 1 shows the relevant configurations of the dual-core microarchitecture. And Table 2 is a performance comparison table between Falcon and mainstream lock-step cores such as Power e200z7 and ARM Cortex-R5, which proves that Falcon is comparable to market-leading products in terms of performance. Meanwhile, the synthesis report of the design compiler shows in SMIC 40nm PDK, the single core costs 1812013 um^2 while the dual-core lockstep version costs 2402623 um^2.

Table 1: Dual-Core Lockstep Configurations

Components	Specifications
Target Frequency	350MHz
Branch Target Buffer	1024 entries
Fetch Packet Width	128 bits
Issue Width	2
ROB	24 entries
L1 I-Cache/D-Cache	32/32KB, 8way associative, LRU
I-TCM/D-TCM	16/64KB

Table 2: Performance Comparison

	Falcon	e200z7	ARM R5
ISA	RV32GC	Power ISA Embedded	ARM v7-R, AArch32
Memory Management	PMP, MMU	MMU, MPU (optional)	MMU, MPU (optional)
FPU	Integrated	Integrated	Optional
Issue Width	2	2	Selected Dual Issue
Dhrystone (DMIPS/MHz)	1.82	2.27	1.67
Coremark /MHz	2.90	2.00	3.47

Verification

A UVM verification platform is built based on the spike instruction simulator as the reference model, the value of registers that commit from the top of Reorder Buffer are extracted and compared with value from the spike simulator in a UVM scoreboard. Various instruction types are thoroughly verified using input sequences such as google dv, Coremark, and Dhrystone. Falcon is successfully deployed on a Xilinx ZCU102 FPGA with a Coremark performance of 2.90 Coremark/MHz.

Conclusion & Outlook

We have implemented Falcon, a RISC-V-based dual-core lock-step MCU, and completed its verification work successfully. Our work demonstrates that RISC-V can fully leverage its open-source advantages in the automotive safety MCU market and open up a market comparable to ARM and PowerPC. We plan to complete the tape-out work of Falcon in 40nm Process by the end of this year.

References

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