Falcon: A Dual-Core Lockstep Microprocessor Based on RISC-V ISA

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Dual-Core Lockstep Basic
To meet the requirements of high reliability and safety in the automotive industry, run two identical processor cores in parallel and comparing their outputs

- Reduced software overhead
- Avoided common-mode failures in space and time
- High error coverage

Single-Core Microarchitecture
A 32-bit dual-issue in order RISC-V processor

- Support RV32I/MAFDC
- 6-stage pipeline arch
- In-order dual-issue
- With branch prediction
- With low-power design
- MMU integrated
- PMP integrated
- ICache and DCache
- Support for interrupt, debugging and off-chip memory
- Has been verified by SMIC 40nm

RISC-V in Dual-Core Lockstep
- Open-sourced ISA in Dual-core Lockstep Arch
- Performance equivalent to commercial automotive SoCs
- Software compatible with IAR (an embedded software development tool)

Performance Comparison Table
<table>
<thead>
<tr>
<th></th>
<th>Falcon</th>
<th>E200z7</th>
<th>ARM R5</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISA</td>
<td>RV32GC</td>
<td>Power ISA Embedded</td>
<td>ARM v7-R, AArch32</td>
</tr>
<tr>
<td>Memory Protection</td>
<td>PMP</td>
<td>MPU</td>
<td>MPU (optional)</td>
</tr>
<tr>
<td>FPU Integrated</td>
<td>Integrated</td>
<td>Integrated</td>
<td>Optional</td>
</tr>
<tr>
<td>Issue Width</td>
<td>2</td>
<td>2</td>
<td>Selected Dual Issue</td>
</tr>
<tr>
<td>Dhrystone (DMIPS/MHz)</td>
<td>1.82</td>
<td>2.27</td>
<td>1.67</td>
</tr>
<tr>
<td>Coremark (Coremark/MHz)</td>
<td>2.90</td>
<td>2.00</td>
<td>3.47</td>
</tr>
</tbody>
</table>

Conclusion & Outlook
We have implemented Falcon, a RISC-V-based dual-core lockstep MCU, and completed its verification work successfully. Our work demonstrates that RISC-V can fully leverage its open-source advantages in the automotive safety MCU market and open up a market comparable to ARM and PowerPC.

We plan to complete the tape-out work of Falcon in 40nm Process by the end of this year.