AERO:
Accelerated
Eu**R**opean cl**O**ud
An **open-source** software ecosystem for the **EPI hardware**

Harnessing Hardware Acceleration with RISC-V and the EU Processor

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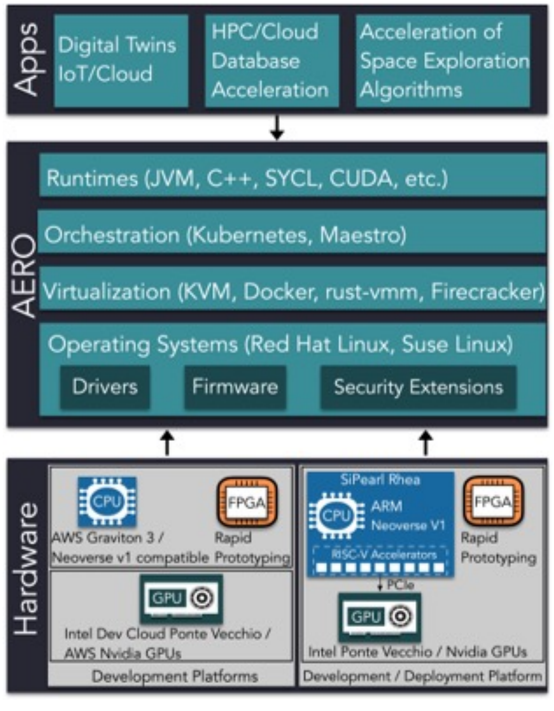
Enriching the software ecosystem for Cloud deployment

ARM/RISC-V based EU hardware designs are being developed

How to efficiently use it from high level programming languages?

AERO Hardware/Software Stack



OS, drivers & virtualization
- Optimized Linux distribution
- Docker, KVM (targeting CPU & RISC-V coprocessors)

Native Programming Languages
- Open-source heterogeneous programming languages & runtimes (SYCL, OpenCL, DPC++/OneAPI)

Managed Programming Languages
- OpenJDK, GraalVM, TornadoVM, Quarkus

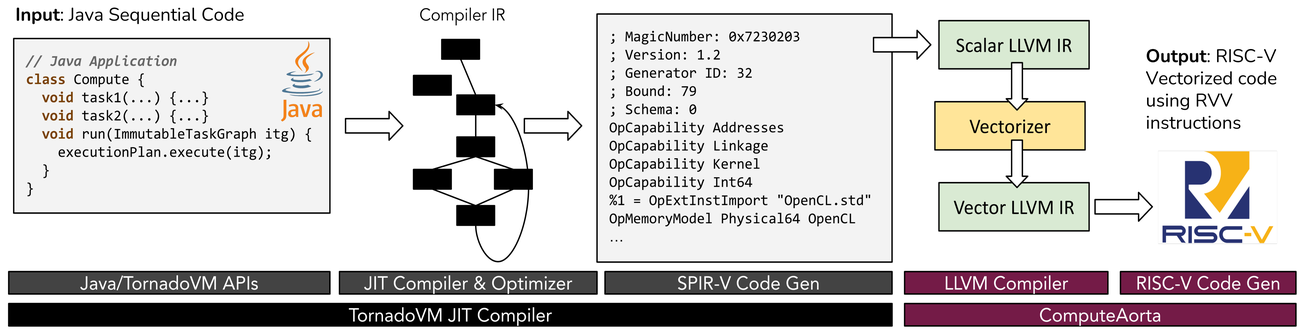
HW acceleration
- Leverage HW components of Rhea for performance & security

Example of leveraging the AERO Stack: Accelerate Java/Cloud workloads on RISC-V

Enabling Language Frontends
- **TornadoVM**: a **Java** parallel programming framework and a **JVM plugin for** transparent **hardware acceleration** on multi-core CPU, GPUs and FPGAs.

Enabling RISC-V Backends
- **ComputeAorta**, from Codeplay, enables implementation of open standards such as OpenCL. It includes **tooling to convert OpenCL C and SPIR-V into target ISA** using existing LLVM backends.

Enabling Vectorization For RISC-V
- **Data Parallel programs** written in Java with TornadoVM can be **accelerated** using **ComputeAorta's** vector units **via RISC-V RVV** ISA instructions generated **from Java scalar code**.




```
$ env SPIKE_SIM_DEBUG=1 CA_RISCV_DUMP_ASM=1 tornado --threadInfo myJavaProgram
Driver: OpenCL
  Total number of OpenCL devices  : 1
  Tornado device=0:0  (DEFAULT)
    OPENCL --  [ComputeAorta] -- RefSi M1
  …
```

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