The TETRISC SoC - A resilient quad-core system based on Pulpissimo

Markus Ulbricht[1]*, Junchao Chen[1], Li Lu[1] and Milos Krstic[1,2]

[1]IHP - Leibniz Institute for High Performance Microelectronics, Frankfurt (Oder), Germany
[2]University of Potsdam, Potsdam, Germany

Abstract

Fault-tolerant systems are typically designed for worst-case scenarios and offer sub-optimal performance during normal operation. Configurable systems that adapt to changing circumstances can improve this situation. This paper presents a design that does just that. The TETRISC SoC is a multiprocessor system based on the Pulpissimo platform that uses various reliability sensors to operate its four cores in different performance and fault tolerance modes as needed. This adaptable solution provides optimal performance and reliability for use cases with high requirements, such as avionics or aerospace.

Introduction and Objective

Due to the steadily increasing demand for real-time data processing, multi- and manycore systems are becoming more and more important, especially in the fields of avionics and aerospace. Their inherent level of redundancy can be exploited to adapt performance and fault tolerance to specific situations. Fault tolerance, in particular, plays a major role in this respect, as for example in space, the radiation rate and thus the number of transient errors can quickly fluctuate by several orders of magnitude ([1]).

The development of such systems requires combining different studies from the fields of adaptive fault tolerance and radiation hardening for avionics and space systems across different system levels. The goal of the present research was to implement such a mixed approach on a single state-of-the-art system with open-source hardware. After thorough investigations on possible platforms, we decided to use the Pulpissimo SoC ([2]) as basis. PULPissimo represents the main System-on-Chip controller for all recent multi-core PULP chips, taking care of autonomous I/O, advanced data pre-processing, external interrupts, and more. The main core, called RI5CY, is an in-order, single-issue core with 4 pipeline stages.

The following section provides deeper insights into the architecture that we created and the different approaches that we used to extend Pulpissimo into a resilient and adaptive quad-core platform.

The TETRISC SoC

The resulting architecture has been named TETRISC (TETra Core System based on RISC-V) SoC and is shown in Figure 1. The gray blocks illustrate the original IPs adopted from the Pulpissimo Platform. The newly added components are shown in blue and orange.

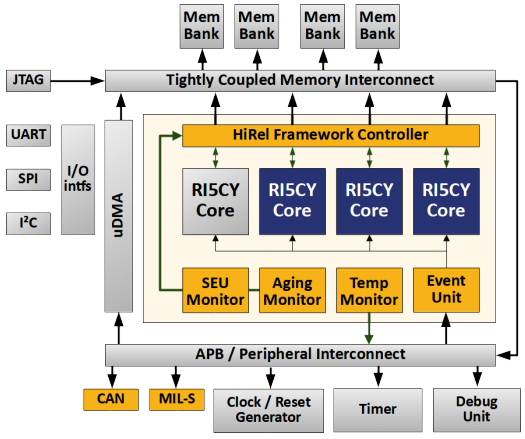

Figure 1: *The system architecture of the TETRISC SoC*

Pulpissimo as multicore

To obtain the necessary degree of redundancy for developing an adaptive and fault-tolerant system, we first extended the Pulpissimo to a quad-core processor structure (see fig. 1). Three additional RI5CY cores, shown in blue, were inserted into the system and connected to the correspondingly expanded interfaces. Above all, the memory interface was reworked and now offers the four cores equal memory access to the entire address space. The separation of the program and data memory of the four cores is done on the software side.

As with the original Pulpissimo platform, interrupts are handled by a (to the cores) external event / interrupt unit. For TETRISC, this was extended accordingly so all four processors can receive interrupts separately.

*Corresponding author: ulbricht@ihp-microelectronics.com

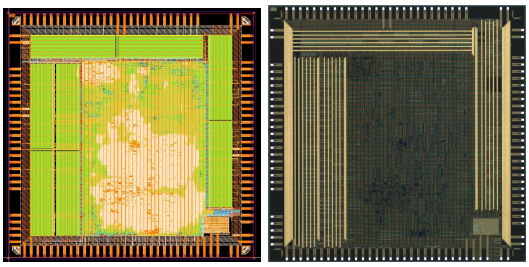

Figure 2: *Layout (left) and die photo (right) of the TETRISC SoC*

Reliability sensors

For the sensor-based proactive reconfiguration of the system, three sensors were selected that, in combination, provide a comprehensive overall picture of acute or future threats: a sensor to determine the temperature, which is a major accelerator of various failure effects, an aging detector for measuring different wear-out related effects on the chip, as well as the single event upset monitor / solar event predictor by Chen et al. ([3]).

Adaptiveness and Fault Tolerance

We implement the adaption of the system in response to the (possibly harmful) factors measured by the sensors as a diverse set of operational modes based on core-level n-modular redundancy (NMR) and clock-gating techniques ([4]). In particular, the TETRISC is capable of assuming three distinct execution modes:

Performance Mode - All cores run independently and execute their own program.

Destress Mode - The cores are clock-gated in a round-robin fashion to limit heat production and, therefore, reduce thermal stress.

Fault Tolerant Mode - Any of the four cores are combined into an NMR lockstep system (two, two-by-two, three- or four-way) with majority voting, to offer additional protection against radiation- or aging-induced faults.

To allow this, we included the so-called HiRel Framework Controller (HFC). It functions as the main control instance and is capable of forwarding the input signals of any core to any other core and, with the help of a programmable NMR majority voter, comparing any combination of output signals. Various control registers in the HFC allow software-based management of the different operating modes based on real-time system status information provided by the sensors.

In addition to the HiRel Framework Controller, the design incorporates custom-designed registers for the cores, which allow rapid switching and synchronization between different modes. This also ensures that the synchronization of tasks between different cores during NMR modes can be achieved in only two clock cycles.

Complementary to the above adjustments, all components beyond the cores were protected against radiation effects by using TMR flip-flops ([5]).

Table 1: *TETRISC SoC details*

Chip area	43,56 mm^2 (6.6*6.6mm)
Nominal clock frequency	30MHz
Power consumption	<1W (estimated)
Memory	4*8192*40 Bit SRAM
Pads	81 signal, 35 other

Summary and outlook

With the TETRISC SoC, a configurable and adaptive platform was created that can dynamically and, based on sensor data, largely autonomously adapt to different performance and fault tolerance requirements. To be able to measure the actual reliability of the system under the harsh conditions of space, the SoC was fabricated in IHPs 130 nm CMOS technology (see Fig. 2 for layout and die picture) and will soon be tested in the beam chamber. Details of the final chip can be seen in table 1. The rather limited clock frequency will be increased in following versions.

Future research will further focus on the design of the custom registers, software support for fast task switching, fault-tolerant design of hardware accelerators, and a broader range of reliability sensors.

References

[1] Robert Glein, Florian Rittner, and Albert Heuberger. "Detection of solar particle events inside FPGAs". In: *2016 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*. 2016, pp. 1–5. DOI: 10.1109/RADECS.2016.8093159.

[2] *PULP platform*. URL: https://pulp-platform.org/ (visited on 10/22/2022).

[3] Junchao Chen et al. "Solar Particle Event and Single Event Upset Prediction from SRAM-Based Monitor and Supervised Machine Learning". In: *IEEE Transactions on Emerging Topics in Computing* 10.2 (2022), pp. 564–580. DOI: 10.1109/TETC.2022.3147376.

[4] Aleksandar Simevski et al. "PISA: Power-robust Multiprocessor Design for Space Applications". In: *2020 IEEE 26th International Symposium on On-Line Testing and Robust System Design (IOLTS)*. ISSN: 1942-9401. July 2020, pp. 1–6. DOI: 10.1109/IOLTS50870.2020.9159716.

[5] Oliver Schrape et al. "Design Concept for Radiation-Hardening of Triple Modular Redundancy TSPC Flip-Flops". In: *2020 23rd Euromicro Conference on Digital System Design (DSD)*. Aug. 2020, pp. 616–621. DOI: 10.1109/DSD51259.2020.00101.