The TETRISC SoC – A Resilient Quad-Core System Based on PULPissimo

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GOALS

- Develop an adaptable and resilient multiprocessor system for reliability-critical applications.
- Implement on-demand reconfigurable redundant system allocations under harsh conditions.
- Develop strategies to balance system reliability, power consumption, and performance in real-time.

MOTIVATIONS

- Growing need for real-time data processing in aviation and aerospace
- Overcoming traditional static fault mitigation methods.
- Requirements for real-time reliability monitoring network.
- Addresses the dynamic reliability needs of systems that provide optimal operation under normal and severe conditions.

PLATFORM

- Using the open-source PULP platform and RI5CY core
- HiRel Framework Controller (HFC) for dynamic tuning of operating modes with core-level NMR and clock gating.
- ResiliCells enable fast switching of operating modes.

OUTLOOK

- Intended to further optimize ResiliCells to reduce hardware overhead and improve fault tolerance.
- Radiation testing and evaluation of the target chip

TETRISC SoC Overview

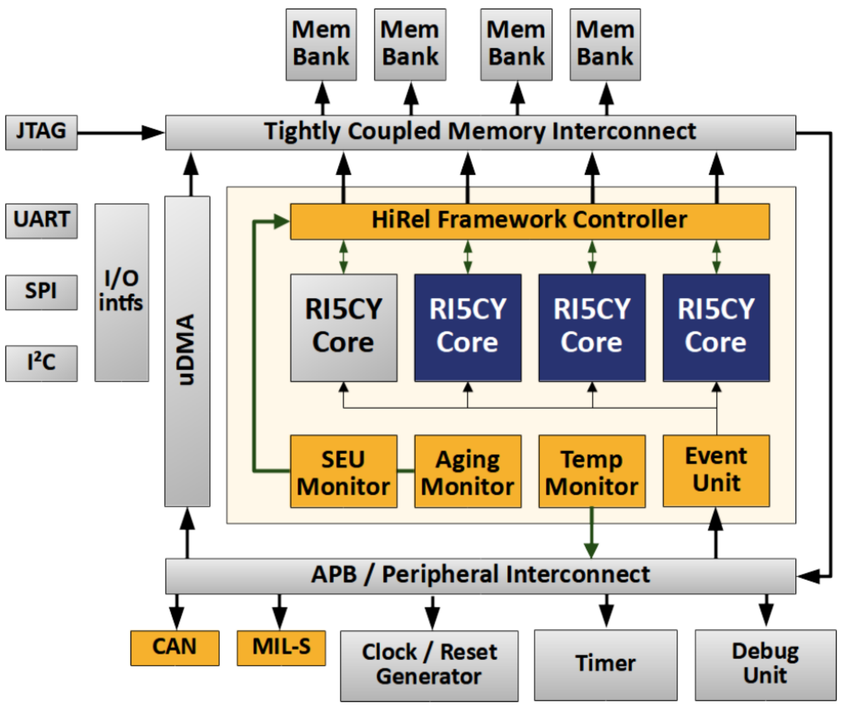

Fig. 1 The system architecture of the TETRISC SoC.

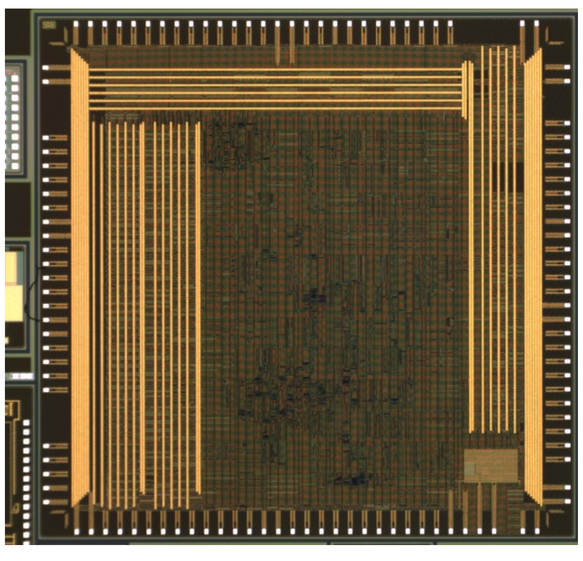

Fig. 2 The die photo of the chip.

- Reconfigurable RISC-V-based quad-core SoC based on the open-source single-core microcontroller architecture PULPissimo.
- Multiple on-chip monitors: SEU (radiation), core aging, and temperature monitors.
- Dynamic tradeoffs between reliability, performance and power consumption.
- Intelligent central framework controller for hybrid critical edge computing applications.
- Fabricated with 130nm IHP technology.
- ASIC and FPGA demonstrators.

Chip area	43,56 mm^2 (6.6*6.6mm)
Nominal clock frequency	30MHz
Power consumption	<1W (estimated)
Memory	4*8192*40 Bit SRAM
Pads	81 signal, 35 other

Reliability Monitors

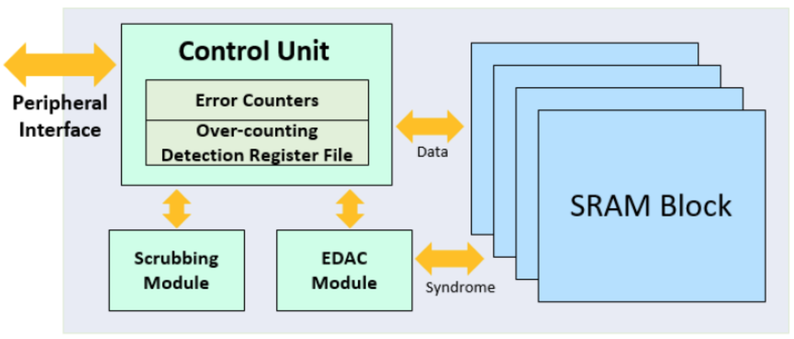

Fig. 3 General architecture of the Single Event Upset (SEU) radiation monitor.

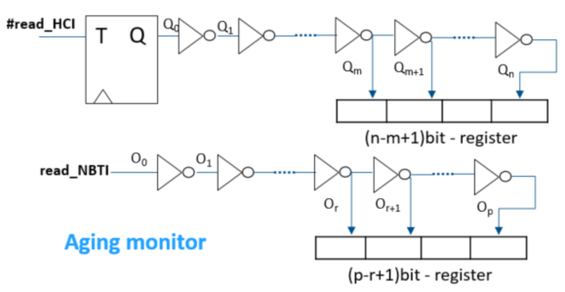

Fig. 4 Gate-oxide aging monitor consists of HCI and NBTI from IHP.

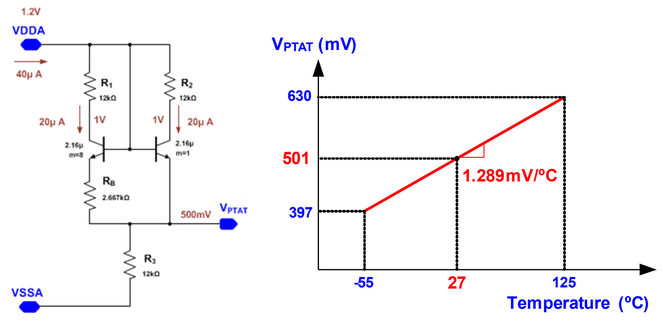

Fig. 5 Analog temperature monitor.

Adaptiveness and Fault Tolerance

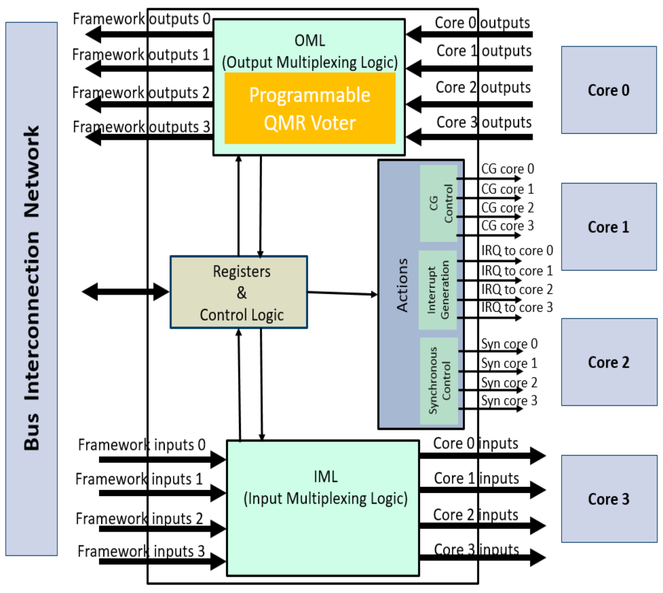

Fig. 6 Block diagram of the HiRel Framework Controller.

- Manages all core inputs and outputs, implementing various operation modes with core-level N-Modular Redundancy (NMR) and clock gating.
- Includes a binary matrix-based programmable NMR majority voter that provides dynamic selection.
- Three operating mode groups: high performance, power saving, and fault tolerance.

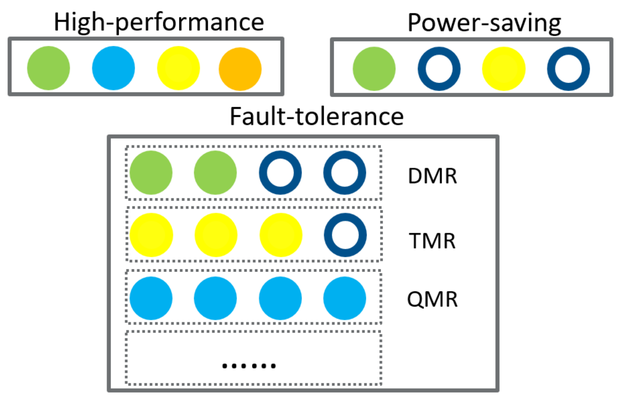

Fig. 7 Example of operating modes in this quad-core multiprocessing system.

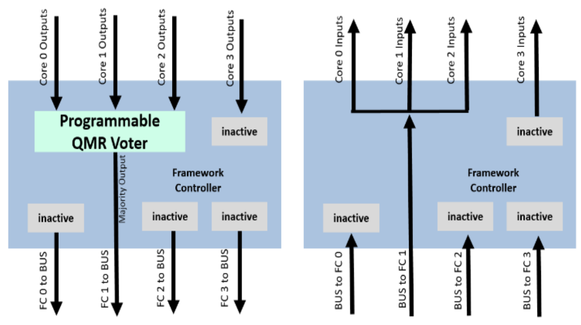

Fig. 8 Example of the HFC configuration. Core 0, 1 and 2 form the core-level TMR, and core 3 is in the clock-gating status.

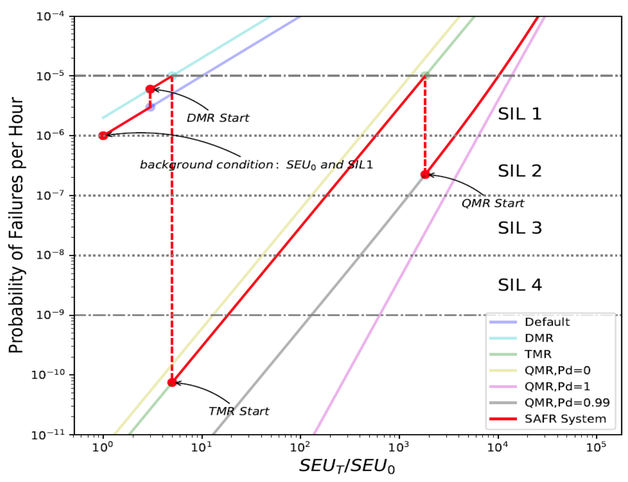

Fig. 9 Example of the optimal mode selection for this chip.

- Various user-defined and self-triggered fault-tolerant modes with the reliable monitor network.
- Task synchronization between different cores can be achieved in two clock cycles.
- Protection of all components outside the core through the use of TMR flip-flops.

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