The Scale4Edge ecosystem covers highly scalable components and extends them for edge applications on three levels:

1. CPU instruction level defined by the RISC-V Instruction Set Architecture (ISA) and Instruction Set Architecture Extensions (ISAX)
2. Software level defined by the C11 standard with compilers and libraries open to complementary standards like MISRA-C
3. Operating system and firmware level through system services, configuration interfaces, and drivers

Scale4Edge tools customize, design, verify, and produce application-specific RISC-V based microprocessors

CoreDSL is a domain-specific language for the definition of base ISAs and ISA extensions (ISAX), usable for verification and HLS

TGC from MINRES is a highly flexible, scalable and extendable RISC-V processor for IoT applications, developed according to the safety standard ISO 26262

"Longnail": High-Level Synthesis for ISA Extensions

The custom HLS flow is based on LLVM, using the CIRCT framework for generating hardware for the ISAX

Software Analysis & Synthesis

Static Software Analysis

- AbsInt provides 3 static analysis tools
  - Astre analyzes C source code for runtime errors
  - StackAnalyzer analyzes binary executables for worst-case stack usage
  - aiT analyzes binary executables for WCET

Software Synthesis

- Compiler generation for ISAX based on CoreDSL, gcc, and Clang/LLVM
- Compiler generation for CoreDSL
- TableGen
- C/C++
- Compiler

TinyML

Complete end-to-end flow transforms ML model into deployable machine code including a kernel library for RISC-V MCUs (muRISC-NN) uses and extends two frameworks:

- TensorFlow Lite for Microcontrollers (TFLM)
- Apache TVM

AI Edge Processing Demonstrators

- ML accelerator for signal processing and RNNs, applies delta encoding and sparsity exploitation
  - Windowing, filtering, frequency transformations
  - Different RNNs (GRU, LSTM, LMU)
  - Demonstrator chip in GF 22FDX technology

SpinNedge

- ML accelerator for signal processing and RNNs, applies delta encoding and sparsity exploitation
  - Windowing, filtering, frequency transformations
  - Different RNNs (GRU, LSTM, LMU)
  - Demonstrator chip in GF 22FDX technology

Applications

UltraTrail

- Ultralow-power AI accelerator for edge devices
  - Real-time inference of temporal convolutional networks (TCNs)
  - Total power consumption in the low microwatt range

Demonstrator Chip

- Neural-network-based audio event detection model
  - PULPissimo-based SoC platform using IP components and software of the Scale4Edge ecosystem
  - GF 22FDX technology

High Reliable Applications (HiRel)

- Different modes: high performance, distortion & fault tolerant modes
- Monitors for SEU, aging, temperature
- Rad-tolerant memory protected with ECC
- Based on PULPissimo platform
- Demonstrator chips in IHP 130 technology

Verification and Simulation, and Debugging

Virtual Prototype Based Simulation

- DBT-RISE: environment to implement ISS interpret or compiled execution, instruction accurate
- VP-VIBES: VP rapo with peripherals & ISS models
- Verification IP: Concolic SW Testing (SymEx/VP), Cross-Level Processor Verification
- ETISS: JIT based VP with varied ISA support customizable by plug-ins for different architectures and applications

Software based Self-Test (SBST)

- BMC based ATPG (FreiTest) using Validity Checker Module (VCM)
- Stuck-at and cell-aware fault models

Fault Coverage and Fault Simulation

FEAR-V: GEMU based framework for RISC-V register fault injection and coverage analysis with fault tracing