Performance Modeling of CVA6 with Cycle-Based Simulation

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**CONTEXT**

- **CVA6\(^1\):** a 32- or 64-bit RISC-V application processor
- In-order, single-issue, 6-stage pipeline
- Has been developed at ETH Zurich as Ariane
- Now maintained by OpenHW Group
- Current performance is 3.09 CoreMark/MHz

How to improve performance further?

1. https://github.com/openhwgroup/cva6

**CYCLE-BASED MODEL**

- **Goal:** Easily evaluate architecture improvements
- **Input:** RVFI trace from CVA6 (committed instructions only)
- **Output:** Cycle-annotated RVFI trace

**Issue**

- data hazards $\rightarrow$ Read-after-Write (data dependence)
- structural hazards $\rightarrow$ multiplication
- control hazards $\rightarrow$ \{IQ length (PC discontinuities), BHT, RAS, BTB\} branch prediction

**Execute**

- load
- store
- mul
- duration $\Rightarrow$ done

**Commit**

- done?

- RVFI trace $\rightarrow$ Instruction Queue $\rightarrow$ Scoreboard $\rightarrow$ Retired $\rightarrow$ Annotated trace

- cycle execution order

**MEASURING MODEL ACCURACY**

- Using 2\(^nd\) iteration of CoreMark
- For each instruction $i$
  - Commit cycle: $t_i$
  - Duration since previous commit: $\Delta t_i = t_i - t_{i-1}$
- Compare with RTL
- Count of correct results: $\#\{i \mid \Delta t_i^{Model} = \Delta t_i^{RTL}\}$
- Number of executed instructions: $\#\{i\}$

**Extrapolating Performance**

- Configurable model: up to $N$ issues & $M$ commits/cycle
- 2-issue, 2-commit: 4.54 CoreMark/MHz
- No additional structural hazards considered yet
- No additional optimisations considered yet

**PERSPECTIVES**

- **Goal:** Go further than 4.54 CoreMark/MHz
  - Exploration of superscalar microarchitectures
  - Performance evaluation using the model
  - Implement the chosen superscalar architecture

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\[\text{Accuracy} = \frac{\#\{i \mid \Delta t_i^{Model} = \Delta t_i^{RTL}\}}{\#\{i\}} = 99.2\%\]