Performance Modeling of CVA6 with Cycle-Based Simulation

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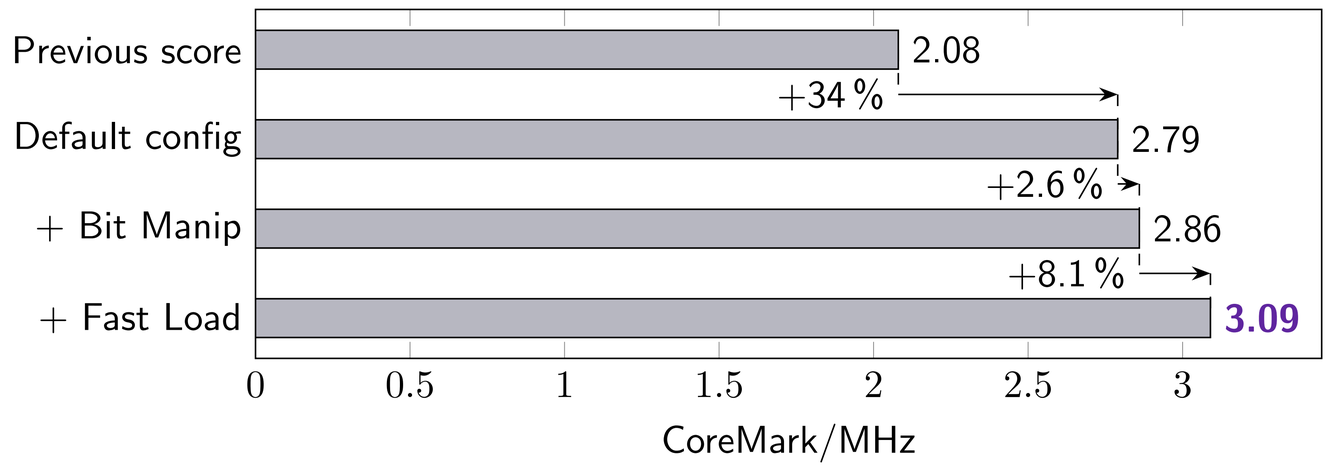
Context

- CVA6[1]: a 32- or 64-bit RISC-V application processor
- In-order, single-issue, 6-stage pipeline
- Has been developed at ETH Zurich as Ariane
- Now maintained by OpenHW Group
- Current performance is **3.09 CoreMark/MHz**

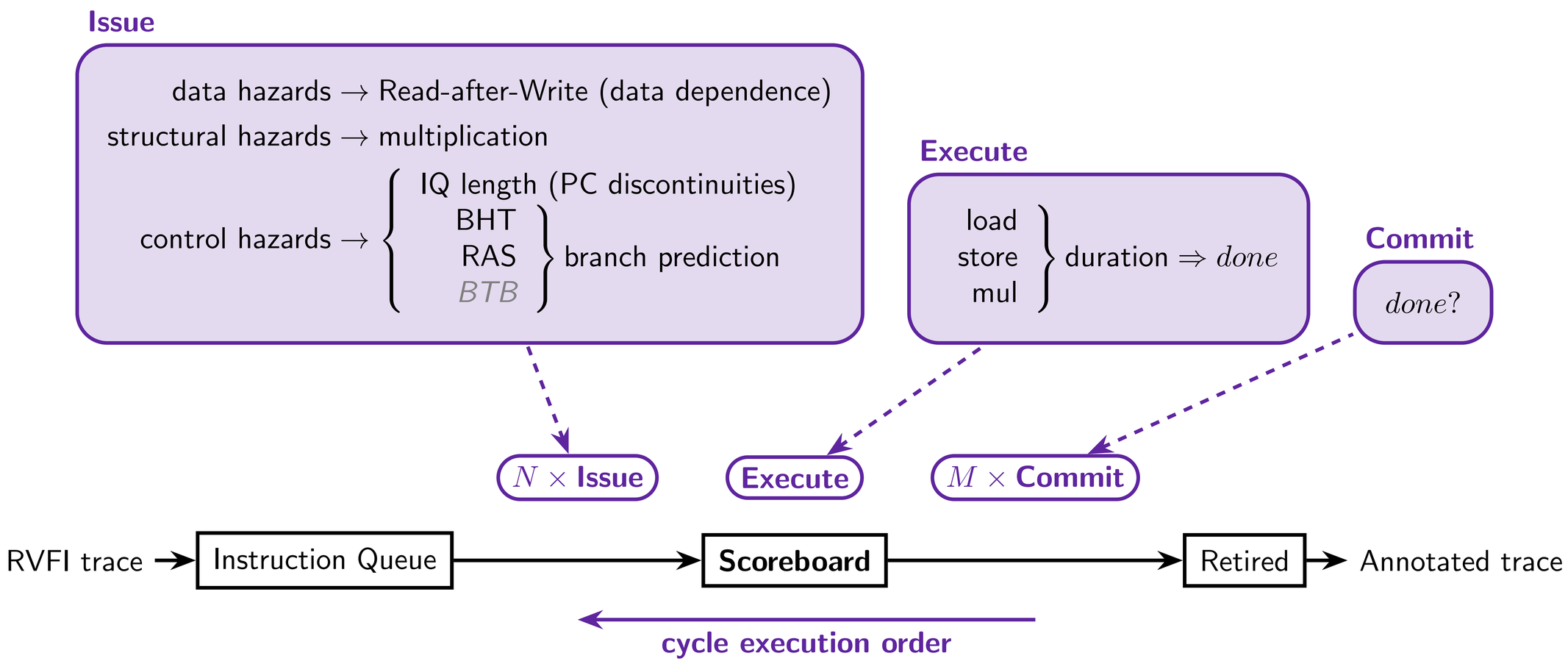
How to improve performance further?

[1]https://github.com/openhwgroup/cva6



Cycle-Based Model

- **Goal** Easily evaluate architecture improvements
- **Input** RVFI trace from CVA6 (committed instructions only)
- **Output** Cycle-annotated RVFI trace
- **Issue** Check for interactions between instructions
- **Execute** Mark as done, delay according to instruction
- **Commit** Check for done mark



Measuring Model Accuracy

- Using 2nd iteration of CoreMark
- For each instruction i
  - Commit cycle: t_i
  - Duration since previous commit: $\Delta t_i = t_i - t_{i-1}$
- Compare with RTL
- Count of correct results: $\#\{i \mid \Delta t_i^{\text{Model}} = \Delta t_i^{\text{RTL}}\}$
- Number of executed instructions: $\#\{i\}$

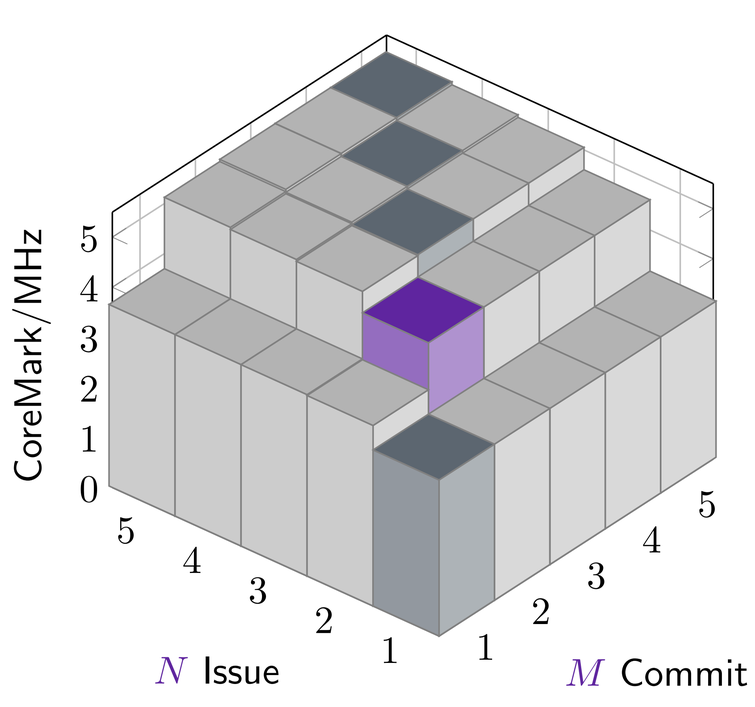
$$\text{Accuracy} = \frac{\#\{i \mid \Delta t_i^{\text{Model}} = \Delta t_i^{\text{RTL}}\}}{\#\{i\}} = \mathbf{99.2\,\%}$$

Perspectives

- **Goal** **Go further than 4.54 CoreMark/MHz**
  - Exploration of superscalar microarchitectures
  - Performance evaluation using the model
  - Implement the chosen superscalar architecture

Extrapolating Performance

- Configurable model: up to N issues & M commits/cycle
- 2-issue, 2-commit: **4.54 CoreMark/MHz**
- No additional structural hazards considered yet
- No additional optimisations considered yet



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