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Open-Source RISC-V Vector Test Suites: A Comparative Analysis

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Abstract

Architecture-level verification of RISC-V Vector (RVV) cores presents a complex challenge due to the diverse behavior of vector instructions under various instruction parameters and core configurations. The vector instruction test suite must be capable of addressing all legitimate combinations of vector instructions under all the different configurations to accomplish comprehensive verification targets. We present a comparative analysis of seven open-source test suites for vector ISA: Imperas, RIOS Labs, RISCV-Torture, RISCV-DV, FORCE-RISCV, Yang's Generator and Tenstorrent. We provide an objective evaluation of the attributes and coverage of these test suites using the RVV Specification v1.0 as a reference. Our study reveals that a combination of these test generators can provide a fairly comprehensive verification strategy for vector cores. On a stand alone basis, FORCE-RISCV covers the complete RVV v1.0 specification upto a VLEN of 4096. Similarly, Imperas is fairly exhaustive but limited to VLEN of 256

1 Introduction

RISC-V is an open-source Instruction Set Architecture (ISA) that offers a wide range of instructions to enable the efficient processing of data. Among these instructions are vector instructions, which are used to process multiple streams of data in parallel. The RISC-V Vector [9] Architecture Compliance Testing (VACT) is crucial in ensuring that a specific vector hardware implementation conforms to the RVV specification and correctly, as well as completely, implements the vector instructions. This typically involves the use of test suites, which are collections of test cases designed to exercise different aspects of the vector ISA. The aim is to develop comprehensive RVV architecture tests that cover not only the full vector instructions but also the various configuration parameters defined in RVV like vector register length (VLEN), register multiplier (LMUL), element width (SEW), etc.

RVV Test Suites

It is important to note that the vector test suite is significantly more extensive than the RISC-V scalar test suite. The vector test suite consists of numerous instructions which can be divided into seven categories defined in RVV Spec as listed in Figure 2 (Column 1). To overcome the challenge RVV-Challenge [1] of verifying a RISC-V based vector core, comprehensive RVV architecture test suites are being developed by the open-source community. Following is the list of the RVV test suites, and in figure 1 presents a comparative analysis of these suites attributes

1. Imperas Vector Test Suite [5]
2. The RIOS Lab Vector Test Generator [3]
3. RISC-V Torture [2]
4. RISC-V DV [4]
5. FORCE-RISCV [7]
6. Yang's Vector Test Generator [8]
7. Tenstorrent Vector Test Suite [6]

Test Suite	Test Suite Attributes					
	Spec Version	Suite Type	Checking Method	Coverage Tool	Supported ISS	Integrated Core
Imperas	1.0	Tests	Signature based	riscvOVPsim	riscvOVPsim	NSITEXE DFP
RIOS Labs	1.0	ATG	Self-Checking	RISCV-ISAC	Sail	-NA-
RISCV-Torture	0.9	RTG	Signature based	-NA-	Spike	Renode
RISCV-DV	0.9	RTG	Signature based	-NA-	Spike	Andes NX27V
FORCE-RISCV	1.0	RTG	Signature based	riscvOVPsim	Handcar	-NA-
Yang's Generator	1.0	ATG	Self-Checking	-NA-	Spike	ARA
Tenstorrent	1.0	Tests	Self-Checking	-NA-	Whisper	Ocelot

Figure 1: Comparative Analysis of different RVV test suites

2 Conclusions || Discussion

In conclusion, we compared seven open-source test suites for RISC-V Vector (RVV) instruction set architecture, aiming to evaluate their attributes and coverage based on the RVV Specification v1.0. The analysis revealed a diverse landscape of test suites, each with unique features.

The Imperas Vector Test Suite emerged as a comprehensive verification tool with a wide range of pre-built test cases. However, its coverage is limited to VLEN 128b and 256b, resulting in reduced coverage for certain vector instruction categories. Also, the RIOS Lab Vector Test Generator, developed in collaboration with the RISC-V Foundation, offers customization options for test generation, making it adaptable to specific testing needs.

Combining these test generators can provide a fairly comprehensive verification strategy for vector cores. However, it is crucial to consider specific project requirements, such as vector register length (VLEN), when selecting an appropriate test suite. This comparative analysis highlights the importance of comprehensive RVV architecture testing and the availability of open-source test suites to facilitate the verification process.

RVV Categories (Total Instructions)	Tests Suites						
	Imperas	RIOS Labs	RISCV-Torture	RISCV-DV	FORCE-RISCV	Yang's Generator	Tenstorrent
Configuration (3)	3	3	2	2	3	3	3
Loads and Stores (310)	45	141	202	258	310	46	25
Integer Arithmetic (139)	137	133	139	136	139	139	60
Fixed-Point Arithmetic (32)	32	32	32	32	32	32	0
Floating-Point (91)	91	66	89	75	91	88	0
Reduction Operations (16)	16	15	16	16	16	16	0
Mask Operations (15)	15	12	15	15	15	13	5
Permutation (21)	21	17	20	18	21	19	5

Figure 2: RVV v1.0 instruction coverage by various tests suites

References

[1] The challenge of risc-v compliance.
[2] Riscv-torture. Dec 2020.
[3] Rios lab atg. Dec 2022.
[4] Riscv-dv. Feb 2021.
[5] Imperas tests. Feb 2023.
[6] Tenstorrent tests. Feb 2023.
[7] Force-riscv. Jan 2023.
[8] Yang's generator. Mar 2023.
[9] Riscv vector spec v1.0. Sep 2021.