Taking the Risk out of Optimizing Your Own RISC-V Architecture Design

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### ASIP Designer™

- Industry-leading tool to design your own Application-Specific Instruction-set Processor (ASIP)
- Language-based description of ISA and microarchitecture: nML
- Single processor model ensures that SDK and RTL are in sync
- Architectural exploration with Compiler-in-the-Loop™ & Synthesis-in-the-Loop™
- Licensed as a tool (not IP): product
- Reuse HW peripherals
- Speedup: DIV

### RISC-V Extensibility

- ISA customization and extensibility are drivers for the growing adoption of RISC-V
- This results in ASIPs with a RISC-V baseline
- Preserve RISC-V compatibility
  - Execute SW code and libraries
  - Reuse HW peripherals
- Challenges
  - Which extensions are best for the target application domain?
  - How to obtain a high-quality SW Development Kit (SDK), including an optimizing compiler?
  - How to obtain a reliable RTL implementation with excellent PPA?
  - How to verify the design?

### Trv (RISC-V) Models

#### Integer models: Trv<mpp<n<r>

- ISA: RV64IM, RV32IM
- Integer and multiply instructions
- Micro architecture
  - Protected pipeline, 3 or 5 stages
  - Hardware multiplier
  - Iterative divider
- Optional extensions: Trv<mmpp<n>r
  - Two-way static ILP
  - Zero overhead hardware loops
  - Load/store with post-modify addressing

#### Floating-point models: Trv32p<n>f

- ISA: RV32IMFixin
- Integer and multiply instructions
- Single precision floating-point instructions
- Micro architecture
  - Protected pipeline, 3 or 5 stages
  - FPU models based on HardFloat (Hauser)
  - Iterative divider and square-root units
- Optional extensions: Trv<mmpp<n>f
  - Two-way static ILP
  - Zero overhead hardware loops
  - Load/store with post-modify addressing

### Designing RISC-V Extensions

- nML models of Trv family are shipped with ASIP Designer tools
- Designers can extend these nML models as desired
- Leverage Compiler-in-the-Loop & Synthesis-in-the-Loop methodologies

#### Option 1: Simple Datapath eExtensions (SDX)

- Acceleration through specialization of scalar RISC-V core
- Trv32p3xs3 is an nML model of RISC-V with predefined extension stubs in the custom-2 opcode space
- User adds behavior of the stubs in bit-accurate C code

#### Option 2: Large-scale Trv extensions

- Acceleration through instruction-level parallelism, SIMD, and/or specialization
- By direct editing of any Trv model
- Typically results in VLIW architecture with a RISC-V scalar issue slot

### Take-Aways

- Designing your own RISC-V architecture with application-specific extensions yields product differentiation and superior PPA, while maintaining flexibility and eco-system compatibility
- ASIP Designer is the industry-leading processor design tool, taking the risk out of your RISC-V design optimization

### More info

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