



X-HEEP: open-source RISC-V uC for EVERYONE

CONFIGURABLE

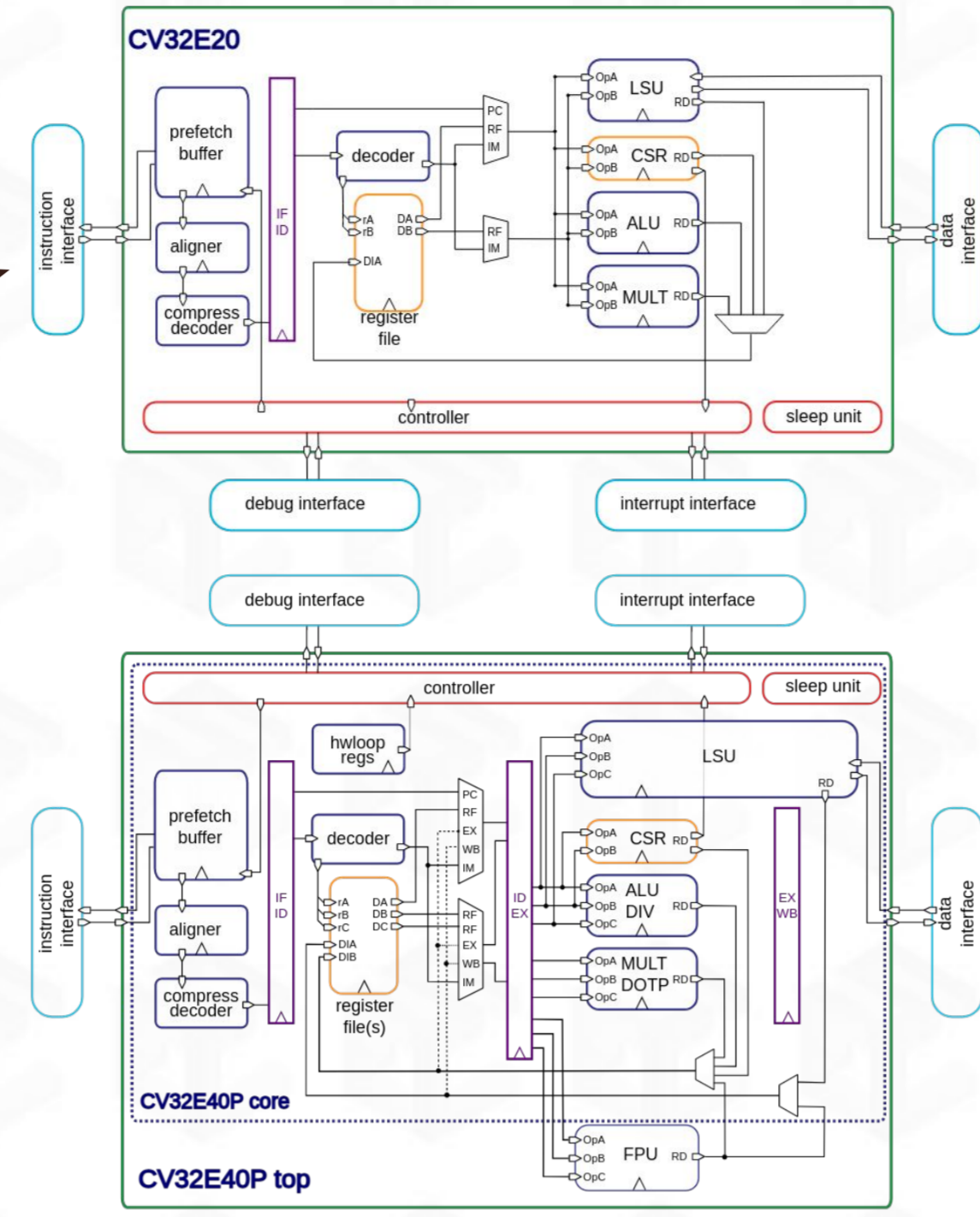


RELIES ON SUCCESSFUL IPS

RELIES ON SUCCESSFUL PACKAGE MANAGER

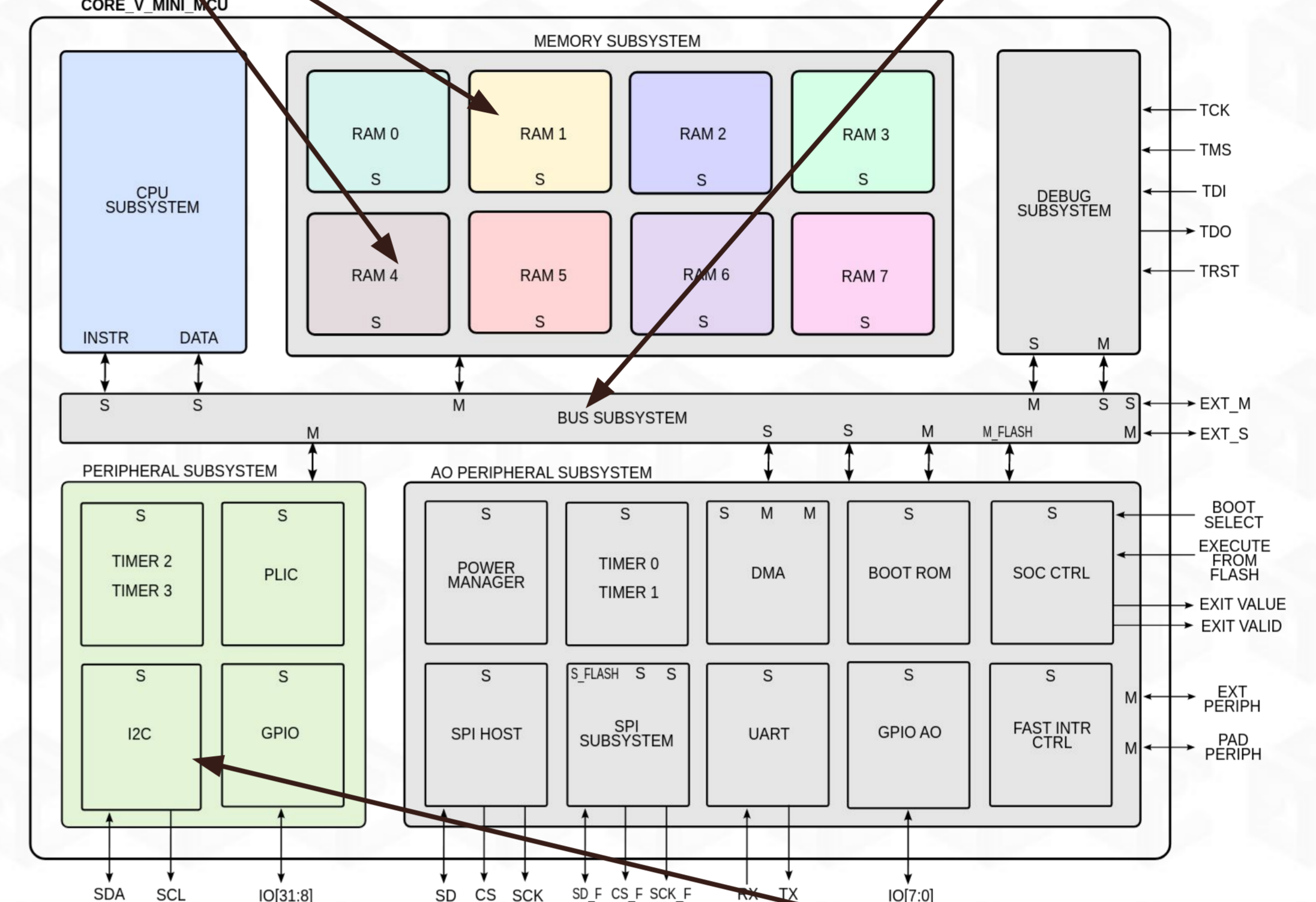


FUSESOC



AMOUNT OF MEMORY

BUS ARCHITECTURE



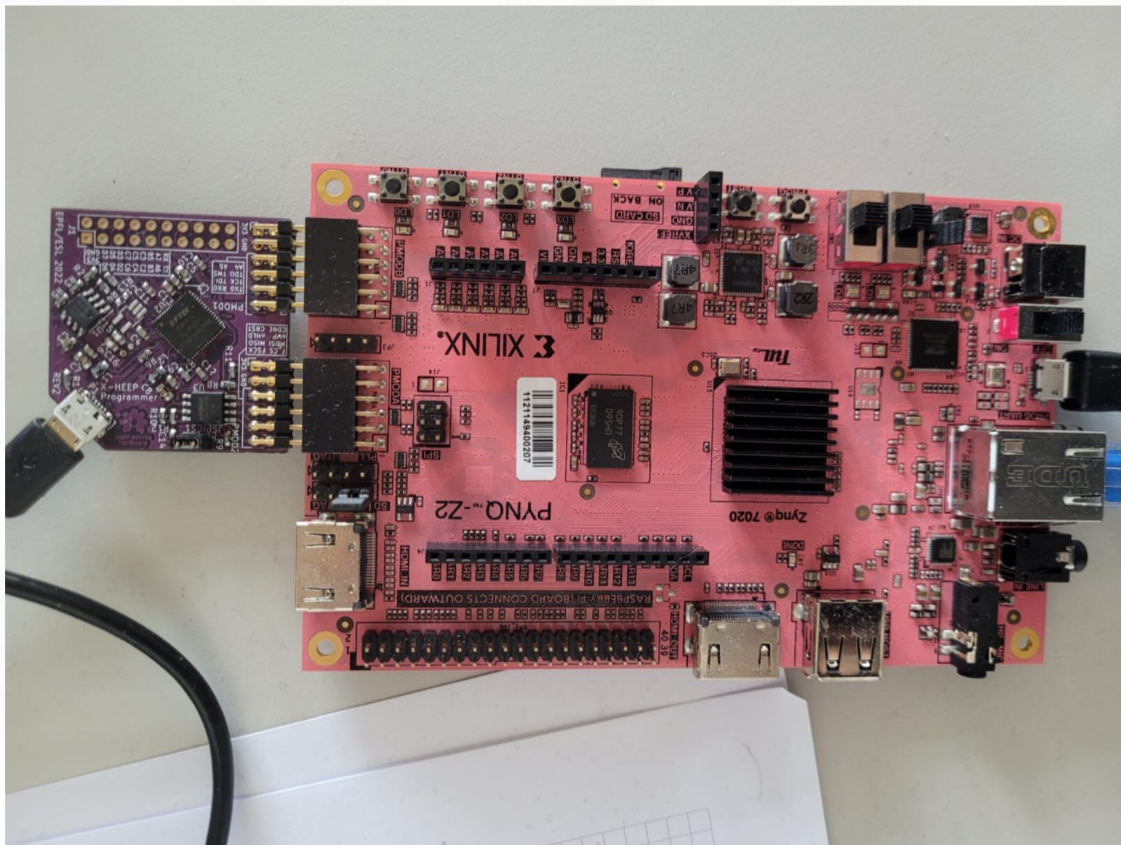
INCLUDE PERIPHERALS

EXTENDABLE

EASY PLUG&PLAY YOUR ACCELERATOR

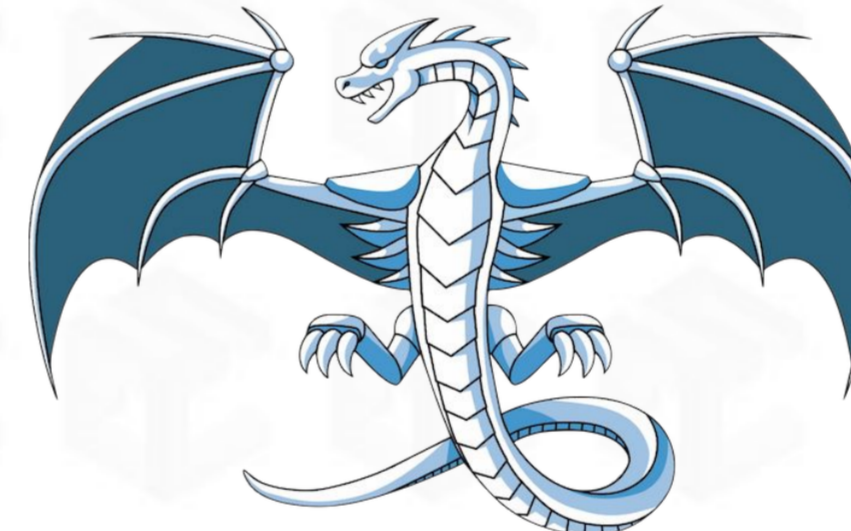
SUPPORT MULTIPLE TARGES

ASIC, FPGA



SUPPORT FOR

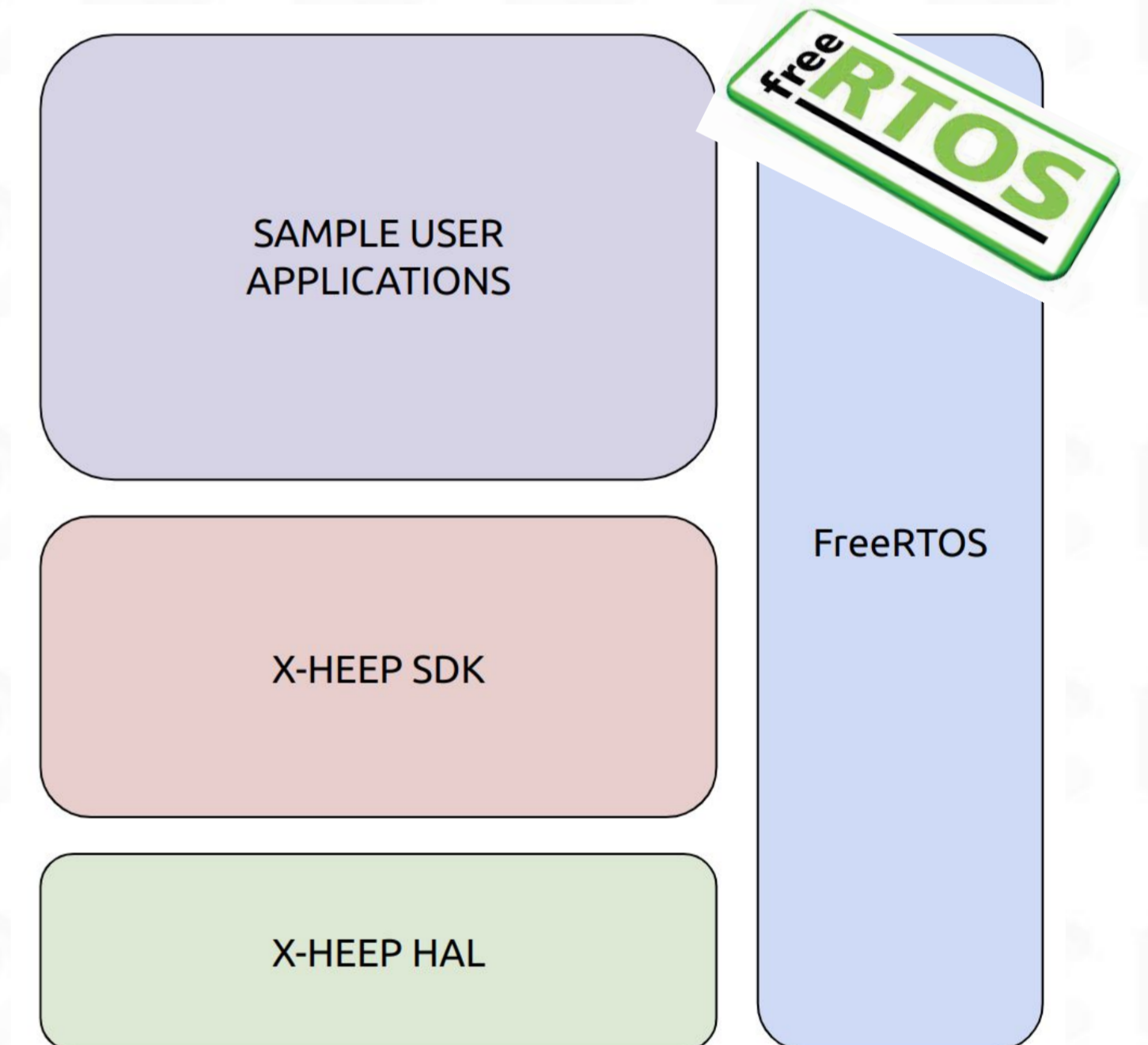
MULTIPLE COMPILERS



SUPPORT FOR MULTIPLE EDA TOOLS



COMPLETE FW STACK

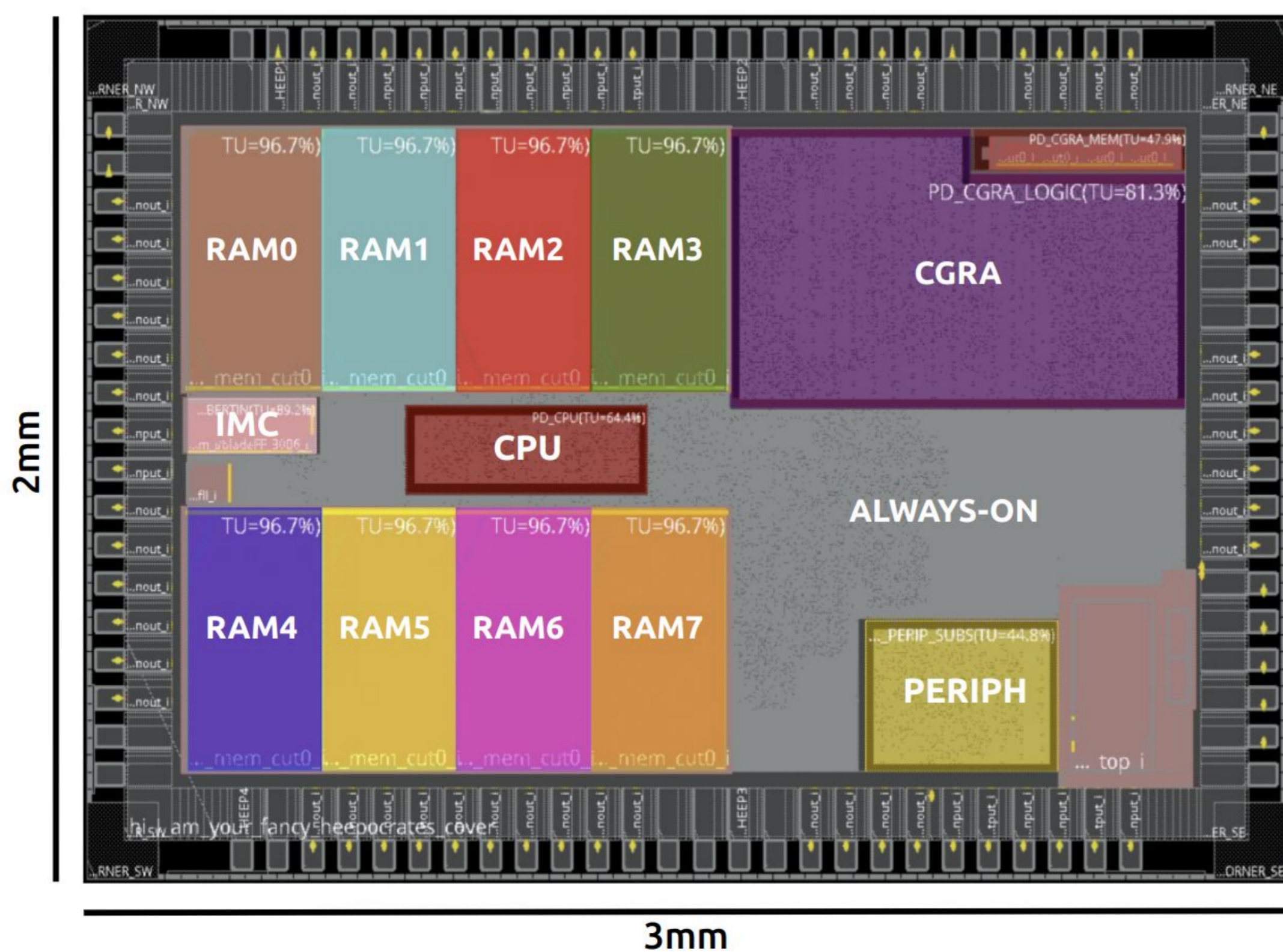


EASY TO USE

STUDENTS, EDUCATION, IP DEVELOPERS

1st TSMC65nm LP IMPLEMENTATION

cve2 CPU, 256kB SRAM, 10 power domains eXtended with CGRA and IMC blocks



TSMC65 LP LVT	SPEED: 32kHz - 250MHz
POWER @1.2V,100MHz (mW)	AREA (kGE)

● CPU - cv32e2/lbex ● 256KB SRAM
● DEBUG ● BUS ● PERIPHERALS

