

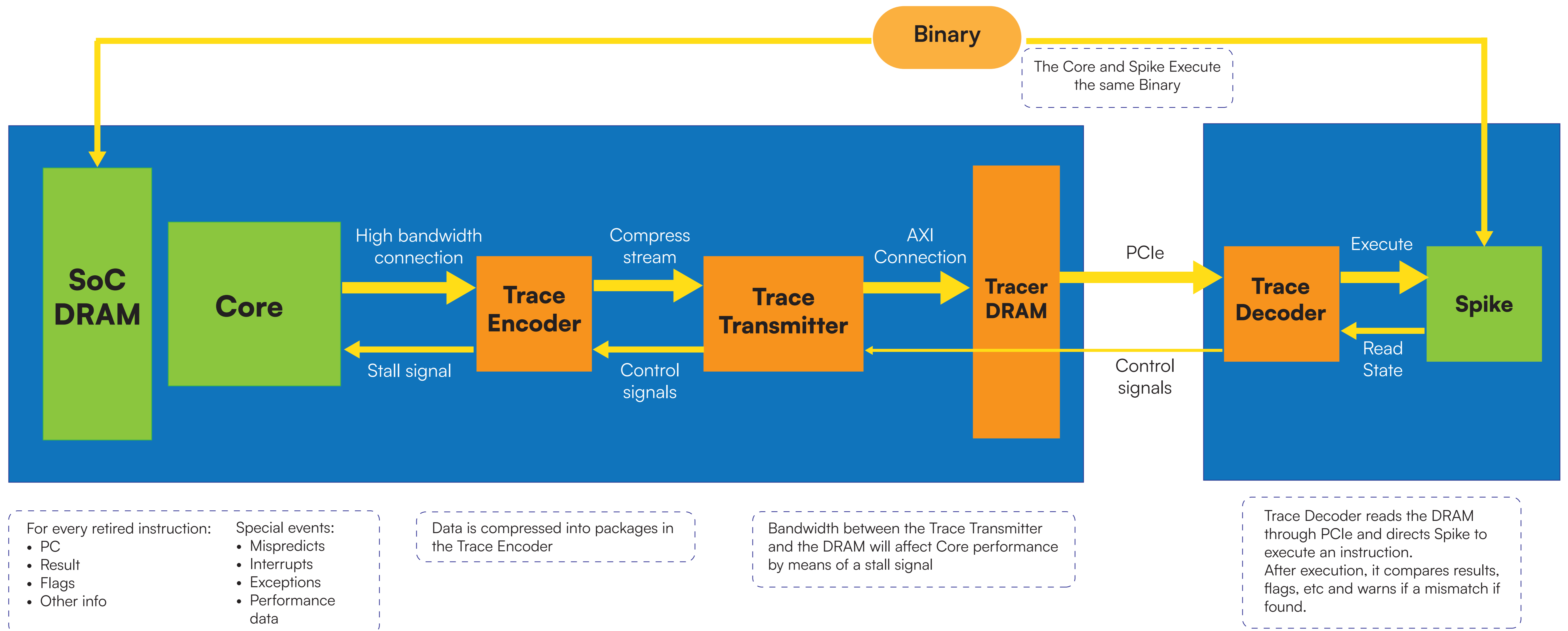
RISC-V Core FPGA tracing for verification

Alberto Moreno, Jordi Cortina, Àlex Torregrosa and Roger Espasa

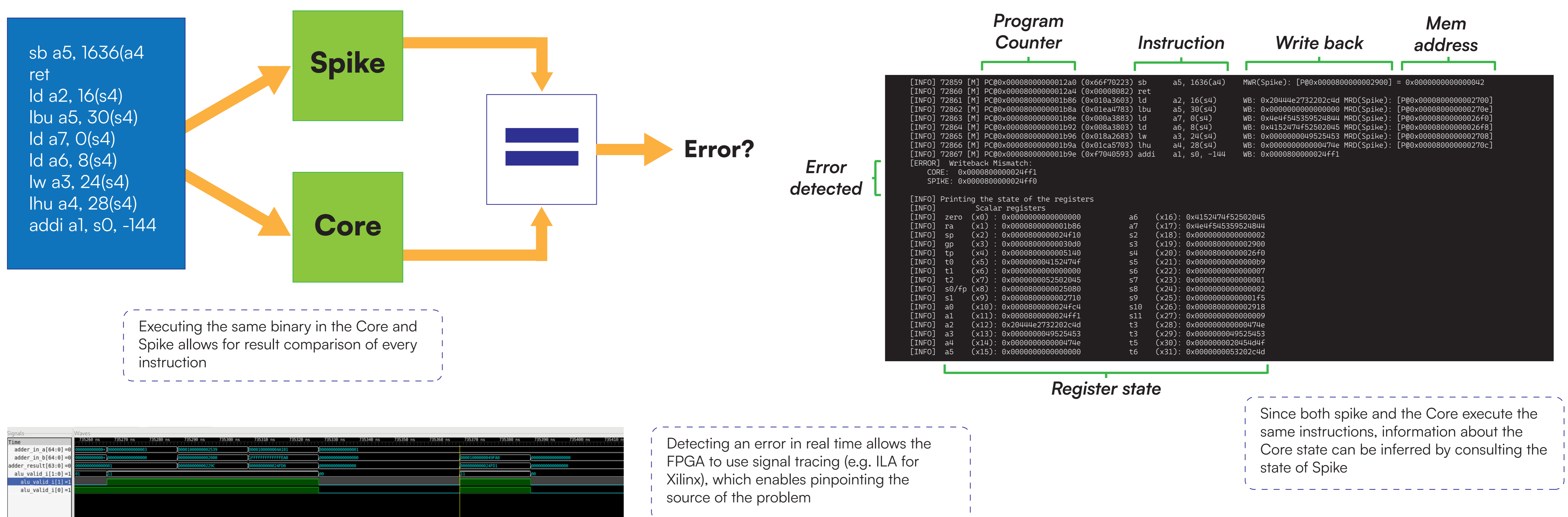
Introduction

Functional verification is a challenging aspect of RISC-V core design. This is typically accomplished by a combination of unit-level testing in simulation along with FPGA-based emulation in very large FPGA platforms such as Veloce or Zebu. Here we present an approach that allows functional verification by co-emulating a RISC-V design along with the open source simulator Spike. Our solution uses a single FPGA to contain the Core and a tracer platform to verify the execution against a golden model (Spike).

Tracer overview



Golden Model Comparison



Performance Exploration

Along with functional verification, it is possible to include performance metrics of the RISC-V Core. Analysis of the binary object enables matching function names to those performance metrics. This allows a very high level of detail, which becomes invaluable for optimization and rapid iteration of designs

