Validating Full-System RISC-V Simulator: A Systematic Approach

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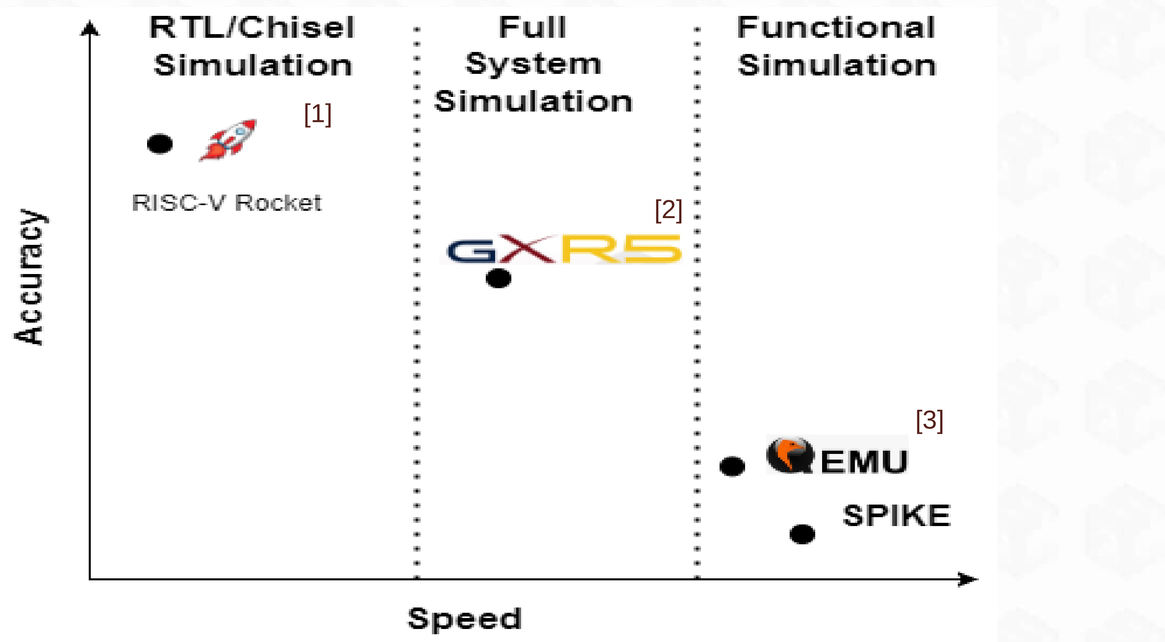
Motivation

- Execute user's workload atop filesystem, kernel.
- Simulate impact of architectural innovations quickly.



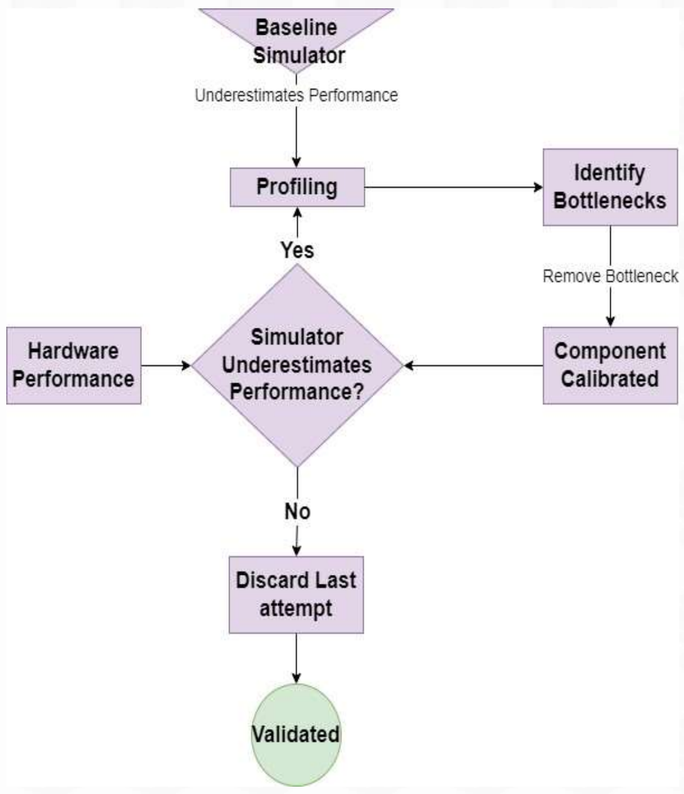
Contributions

Enriches Simulator Validation Methodologies

Full System RISC-V simulator validated against actual hardware (Sifive HighFive Unleashed u54 Core)[4]

Open Sourcing:
- gXR5
- Kernel
- Bootloader
- Filesystem

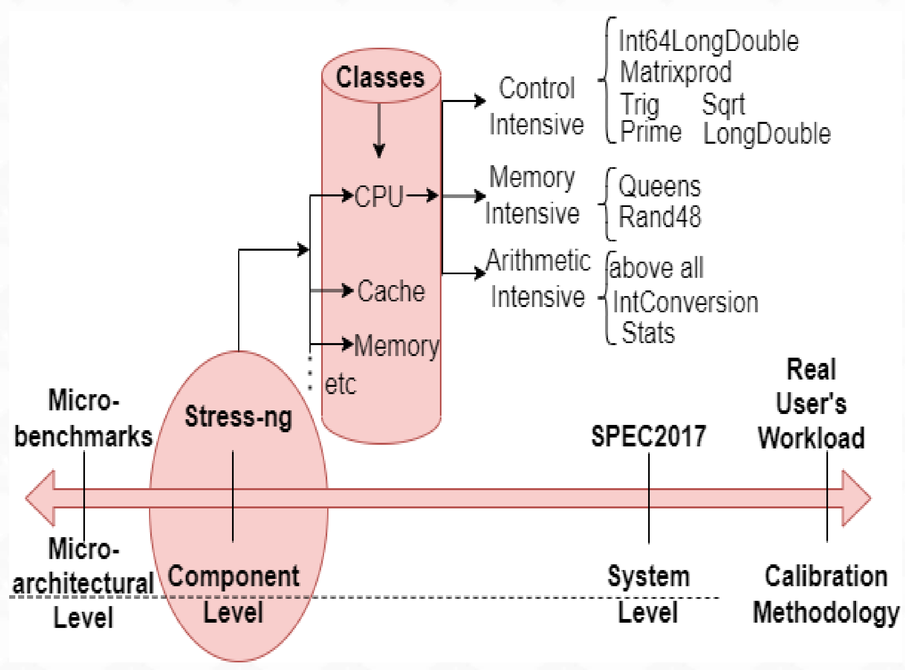
Methodology

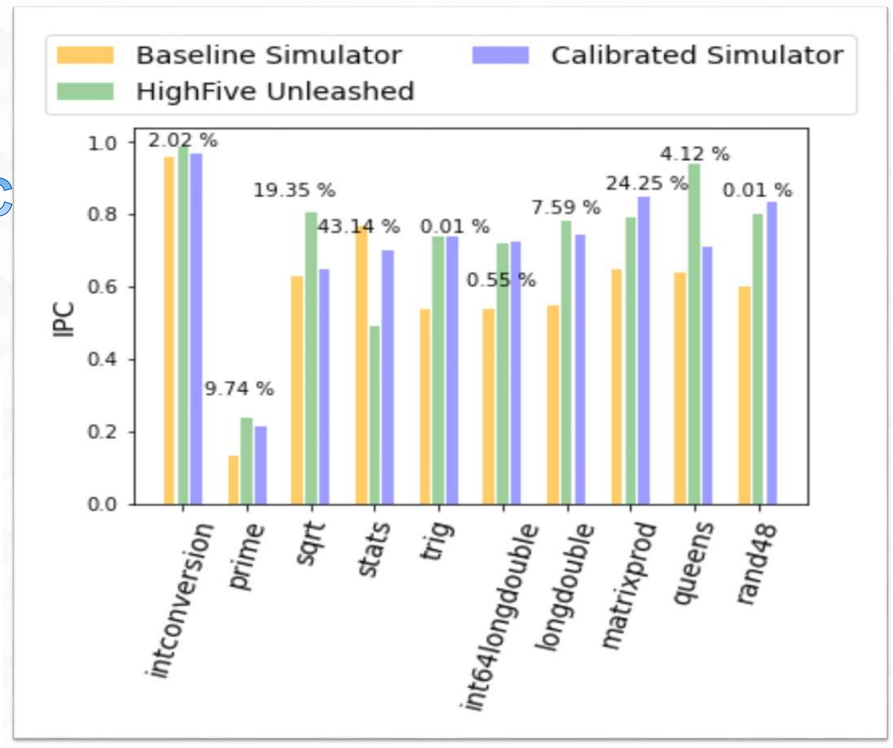


Stress-ng:
Originally, perform stress tests (of components) by causing thermal overruns

Calibrate for IPC

Stress CPU with "stressors"





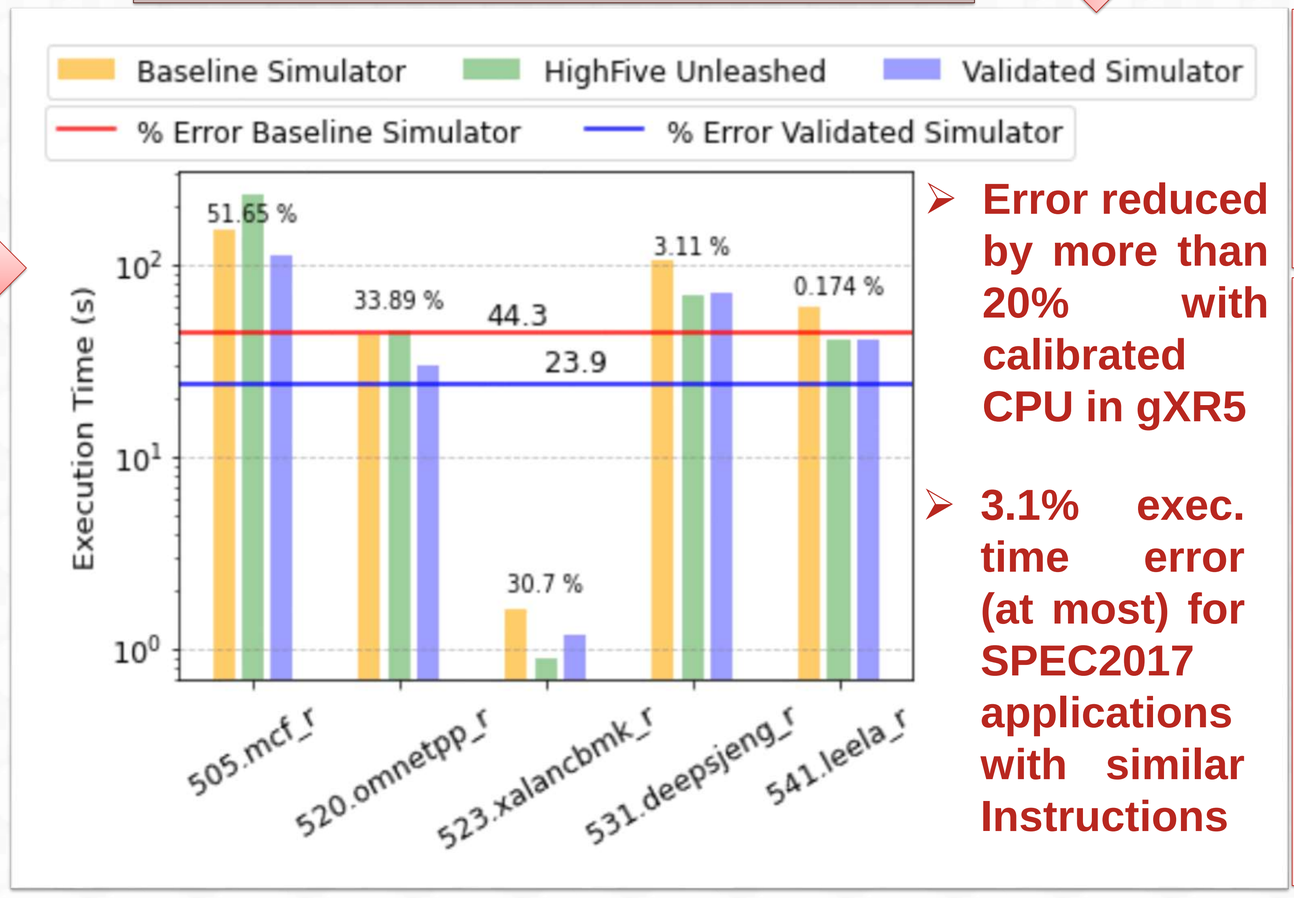
Simulator vs. Hardware performance for stress-ng benchmarks

Validated simulator

Results

Component: Attribute	Baseline Value	Calibrated Value
Read Memory Functional Unit : Op Latency	4 (cycles)	2 (cycles)
Integer Division Functional Unit : Op Latency	33 (cycles)	19 (cycles)
Branch Predictor : Type	Tournament	Multiperspective Perceptron
Fetch2-Fetch1 : Backward Delay	1 (cycle)	0 (cycle)
Execute Unit : Branch Delay	1 (cycle)	3 (cycles)
L1 Cache : Associativity	2	8
L1 -Data Cache : Clusivity	Mostly exclusive	Mostly inclusive

Simulator vs. Hardware performance for SPEC2017 applications



- **Error reduced by more than 20% with calibrated CPU in gXR5**
- **3.1% exec. time error (at most) for SPEC2017 applications with similar Instructions**

Acknowledgments

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