Automated Cross-Level Verification Flow of a Highly Configurable RISC-V Core Family with Custom Instructions

Stanislaw Kaushanski, MINRES Technologies GmbH, Duisburg, Germany (stas@minres.com)
Eyck Jentzsch, MINRES Technologies GmbH, Munich, Germany (eyck@minres.com)

0. The Good Core Family

The TGC core family consists of a set of standard configurations with varying pipeline stages, registers and instruction sets. Each core can be configured and extended with additional features such as different bus interfaces, interrupt controllers, memory protection, caches and custom instructions. This high level of configurability in conjunction with functional safety requirements implies a highly automated, modular, and reusable verification environment.

1. Single Source of Truth

CoreDSL is a domain-specific language that provides a unified representation of the RISC-V ISA and its extensions. The verification environment uses the CoreDSL specification as single source of truth to define random stimuli generation, coverage collection, and coverage goals. The ISS reference model as well as the RTL for custom instructions are also generated from the same source.

2. Automated Code Generation

The verification flow begins with the description of the core in CoreDSL as the single-source-of-truth. The instruction accurate and cycle approximate ISS implementations are generated from this description, along with the configuration for the instruction generator and functional coverage monitor. DBT-RISE infrastructure forms the basis for the generated ISS reference model. Longnail and SCAIE-V tools integrate the custom instructions into the TGC RTL.

3. SystemC-UVM Testbench

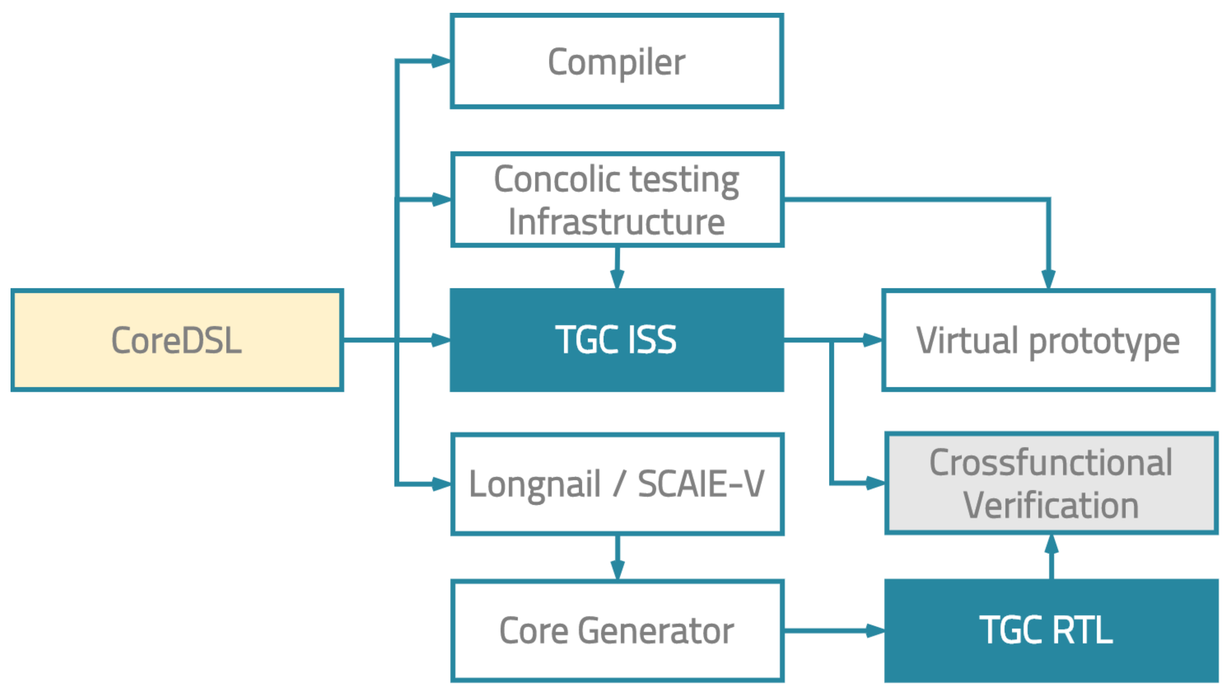
The UVM-SystemC methodology combines the powerful features of UVM, a state-of-the-art hardware verification methodology with SystemC, which simplifies the integration of the ISS.

The testbench has an iBus and a dBus agent, consisting of a sequencer and a driver. During simulation, the DUT initiates instruction fetches, which are received by the iBus driver through a virtual interface (vif). The vif allows them to communicate without being bound to a specific implementation, therefore the DUT can be exchanged without changing the interface itself.

The TGC trace interface maps the internal state of the core. The UVM monitor reads the state and forwards it to the scoreboard, where it will be analysed and compare against the reference.

4. Functional Coverage

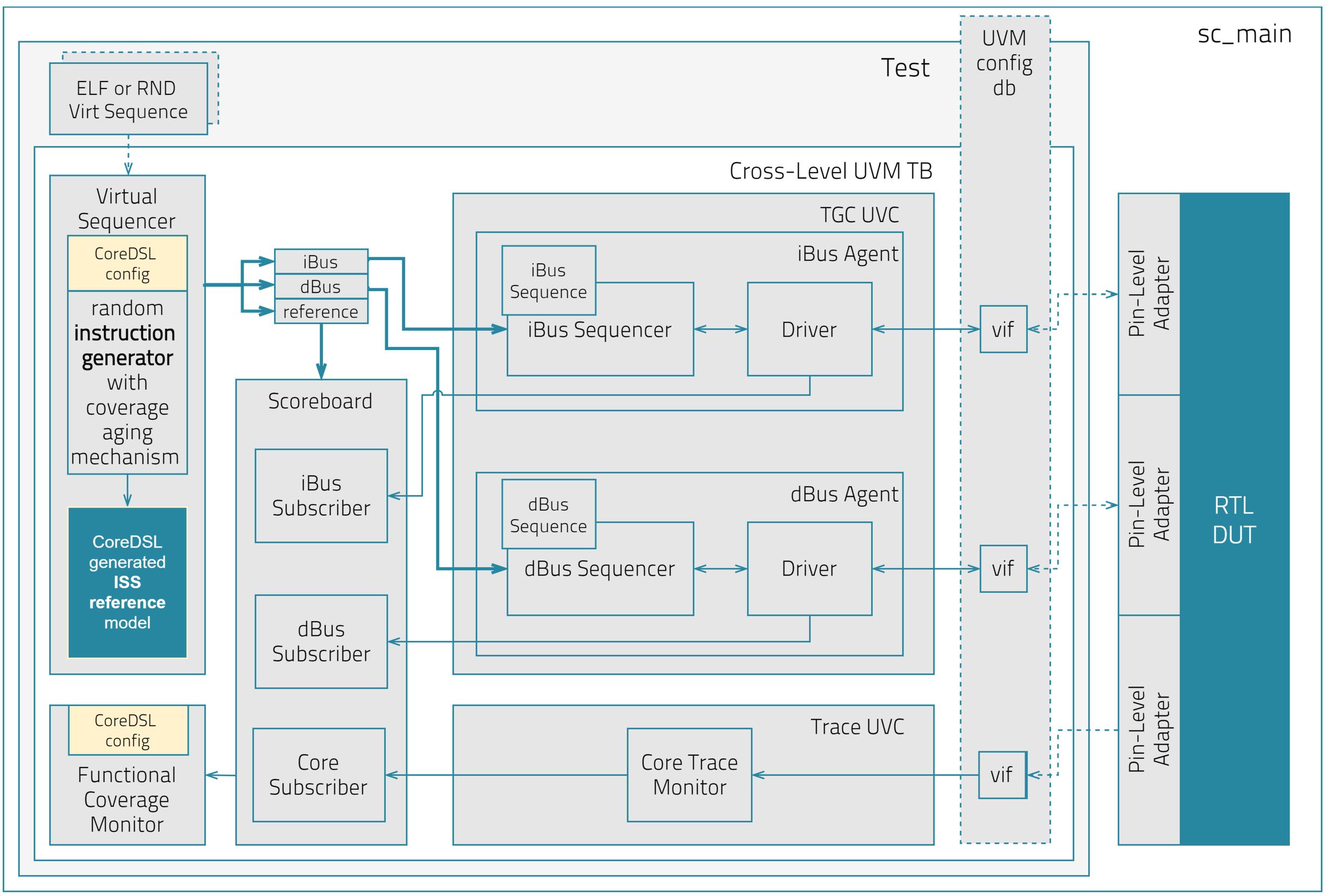
Each instruction that is successfully verified in the scoreboard is sent to the coverage monitor. The FC4SC based coverage monitor is responsible for collecting and reporting functional coverage data. The coverage monitor defines cover groups for each instruction type, which includes coverpoints for tracking all instruction parameters and parameter combinations, as well as hazards between instructions. These cover groups are instantiated for each instruction in the CoreDSL description.



Conclusion

Overall, the UVM-SystemC cross-level verification environment presented in this paper offers a highly effective solution for detecting a range of design issues, including control and data hazards. This approach is not limited to the TGC core family and can be applied to other highly configurable RISC-V core families.

The modular design of the testbench ensures that new core configurations and custom instructions can be added seamlessly, without disrupting the existing verification environment. The use of UVM-SystemC provides a scalable, modular, and reusable solution that can be executed on different simulators, including Verilator, Xcellium, or even on an FPGA e.g. using Raven.



TGC TGC-VP TGC-ISS CoreDSL SCC

CONTACT US

MINRES Technologies GmbH
Keltenhof 2, 85579 Neubiberg
Telefon: 089/67807688
Telefax: 089/67807689
E-Mail: info@minres.com