Iguana: An End-to-End Open-Source Linux-capable RISC-V SoC in 130nm CMOS

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Abstract

Open-source architecture design and register-transfer level (RTL) descriptions, particularly around RISC-V, have made huge strides in the past decade. While open-source physical design and implementation are still lagging behind by comparison, they have recently been catching up: open EDA tools are nearing feature completeness, and some proprietary PDKs are being opened. We present Iguana*, the first end-to-end open-source Linux-capable, 64-bit RV64GC, RISC-V System-on-Chip (SoC). Scheduled to tape out in IHP's 130nm technology, which is currently being open-sourced, Iguana sets important milestones for both open-source silicon and European silicon sovereignty. It implements our* Cheshire *architecture, which uses IP-based high-level synthesis (iHLS) to generate SoCs from carefully designed, silicon-proven open-source IPs. It includes a variety of standard peripherals, a DRAM controller, VGA display output, and a parallel die-to-die link. Cheshire, all its IPs and physical layers (PHYs) are released under a liberal Apache-based license. We implement Iguana with a fully open RTL-to-GDS toolchain, using established tools where possible and filling gaps with our open tools. Iguana is not a one-shot, but the first in a series of SoCs we will progressively extend and improve on. Furthermore, we have pre-validated our architecture through an FPGA mapping and a tested silicon prototype in TSMC's proprietary 65nm node.*

Introduction

In recent years, open-source synthesis and physical implementation tools have significantly improved in quality [1], and some proprietary process design kits (PDKs) have been or are currently being open-sourced [2]. At the same time, the existing open-source architecture ecosystem around RISC-V has matured and is ready to be used in industry-grade silicon. Therefore, the time is ripe to work toward an *end-to-end open-source* Linux-capable RISC-V SoC.

Google and Efabless provide open tape-out runs in Skywater's 130 nm node with their *Caravel* chip [3]. While this approach lowers the bar of entry for IC designers and provides a standard *smart* padframe, it comes with severe design restrictions that render larger SoCs with custom interfaces impossible. Submitted circuits cannot be larger than 10 mm^2 or 1.5 MGE and are to bound mandatory on-chip logic and a fixed padframe. This not only precludes custom IO in general, but also a DRAM interface typically necessary to run an operating system like Linux. Submitted designs are thus typically based around tiny 32-bit microcontrollers connected to custom accelerators.

Fully custom application-specific integrated circuits (ASICs) like Raven [4] have been manufactured, but lack the scale and features required to boot Linux autonomously. We present *Iguana*, a fully custom, end-to-end open-source Linux-capable, 64-bit RISC-V (RV64GC) SoC implemented in IHP's 130nm technology. In particular, we present the following contributions:

- We implement Iguana using a fully open-source tool pipeline from an industry-grade SystemVerilog register-transfer level (RTL) description to a GDS-II layout *without* source alterations to avoid tool limitations. Iguana will tape out in July using the European IHP's *SG13G2* technology [2].
- We build our SoC using the Cheshire [5] platform, which leverages IP-based high-level synthesis (iHLS) to generate arbitrary top-level architectures from hand-crafted silicon-proven open-source intellectual properties (IPs).
- We include two fully digital off-chip interfaces: HyperBus to provide our SoC with DRAM and a parallel die-to-die link to connect to other chips. Both interfaces, including their PHYs, are open-sourced using an Apache-based license.
- We provide various peripheral IO on Iguana, including UART, SPI, I2C, GPIOs, a VGA display output, and JTAG for live debugging.
- We verify Iguana and our Linux boot flow through an FPGA implementation and a tested silicon prototype in TSMC's proprietary 65nm node.

Iguana is the first ASIC in a series of three IHP 130nm tape-outs planned for 2023.

Architecture

Iguana is built around the *Cheshire* platform, a modular framework to create custom Linux-capable SoCs based around CVA6 [6], a 64-bit RV64GC core. Cheshire uses an iHLS approach, assembling systems from a pool of carefully designed silicon-proven IPs

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