Extending OpenPiton framework towards the HPC domain: first steps

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Motivation

- HPC applications are demanding more specialized accelerators to tackle their increasing complexity and requirements
- Europe is promoting the use of the open source RISC-V ISA
- OpenPiton framework is not yet suited for the HPC domain: NoC bus width, fixed caches' block sizes, single issue CPU (OpenSPARC)...

DVINO as a Tile in OpenPiton

OpenPiton[1]: Open source manycore research framework that comprises different tools and modules to build, test and implement RTL designs

DVINO[2]: Drac Vector IN-Order system composed by a RISC-V Scalar Core with a coupled accelerator. Developed at Barcelona Supercomputing Center (BSC)

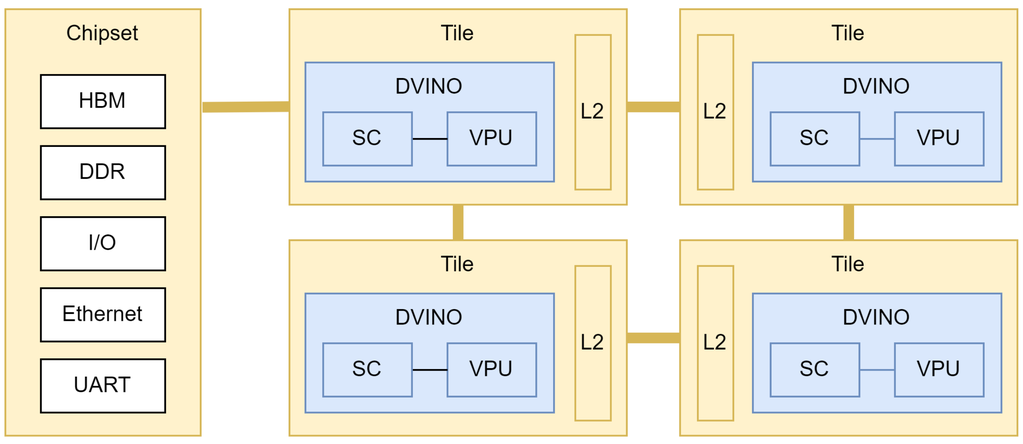


Fig 1. Multicore system based in OpenPiton (yellow-colored) with DVINO as a CPU (blue-colored)

In order to make OpenPiton suitable for the HPC domain, we include several modifications, listed below:

DVINO integration in OpenPiton:

- Provide straightforward compatibility with all in-house RISC-V cores:
  - In-order (currently operative)
  - Deeper pipeline in-order and out-of-order (under development)
- Adaptation to Ariane L1 cache subsystem
- New Performance Monitoring Unit to obtain metrics through CSRs

Scalar core's new features:

- Floating point operations (FD extension v2.2)
- Compress instruction extension (C extension v2.0)
- 6 pipeline stages

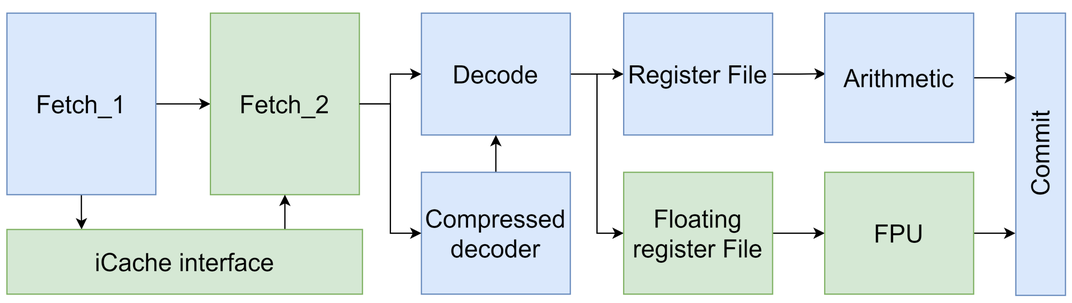


Fig 2. Scalar core pipeline, modifications highlighted in green

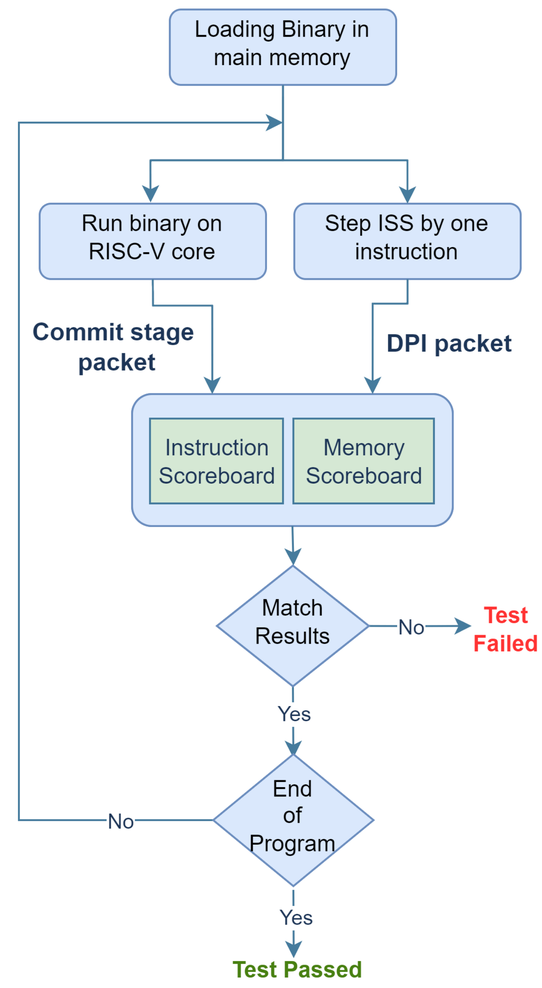
Vector Processing Unit improvements:

- Fusing vector lanes in pairs
- Configurable amount of active lanes (2, 4, 8 or 16 lanes)

Verification

Baseline[1] provides self-checking simulation environments able to compile and run RISC-V tests. On top of that, several improvements have been added:

- Implementation of ISA Scoreboard (cosimulation)
- Implementation of Memory Scoreboard (to be extended for multi-core)
- Addition of an RISC-V ISA Coverage model
  - Unprivileged ISA
  - Privileged ISA
- Continuous Integration (CI) on Gitlab



FPGA contributions

- **Extending FPGAs support** for the Xilinx FPGAs: Alveo U280 and U55C
- **Supporting a custom FPGA Shell[3]:** the framework is now compatible with a flexible, adaptable, configurable and open source FPGA Shell, which provides a seamless communication between the host and accelerators implemented in the FPGA

Conclusions and Future work

We exploit the open source OpenPiton framework to add new features and integrate our in-house CPU series aiming to make steps towards the HPC domain. These steps include modifying the following areas:

- Computational elements, the Tiles
- Verification environment
- FPGA implementation

The main upcoming work will be focused on:

- Including parametric L1 data cache blocks
- Increasing NoC size
- Adding custom L1 data and instruction cache subsystem
- Replacing in-order core by out-of-order core

References

[1] Jonathan Balkind et al. OpenPiton: An Open Source Manycore Research Framework. url: http://doi.acm.org/10.1145/2872362.2872414

[2] Guillem Cabo et al. DVINO: A RISC-V Vector Processor Implemented in 65nm Technology. doi: 10.1109/DCIS55711.2022.9970128 https://drac.bsc.es/en/media/news/tech-dvino-second-generation-lagarto-processor-series-submitted-fabrication-europractice

[3] MEEP FPGA Shell open source repository. https://github.com/MEEPproject/fpga_shell

The MEEP Project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No 946002. The JU receives support from the European Union's Horizon 2020 research and innovation program and Spain, Croatia and Turkey