GreenRio: A Linux-Compatible RISC-V Processor Designed for Open-Source EDA Implementations

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Introduction

Since 20 years ago, Intel has already successfully developed the 3 GHz, 130 nm IA32 processor[1]. However, as the design complexity of IC continues to increase, so does the demand and reliance on electronic design automation (EDA) flow. Besides, the adoption of public toolchains and open Process Design Kit (PDK) has significant implications for the future of semiconductor innovation. Just as the use of open source compilers such as *GCC/LLVM* has revolutionized the software development industry. The optimization capabilities in OpenEDA have the potential to transform the hardware landscape. By leveraging the advantages of open source projects, EDA licenses no longer serve as a bottleneck to design space exploration (DSE), allowing for greater flexibility and collaboration among designers.

Despite the availability of many existing open RISC-V implementations, few are designed with the open-source fabrication flow in mind. As shown in 1, several designs submitted to OpenEDA lack structural components that characterize modern processors. Furthermore, the existing implementations of memory compilers such as *OpenRAM*[2], have mediocre performance and low area utilization. Alongside, current *OpenMPW* designs are too simple and lack the complexity and design features to stress the openEDA flow.

To push forward RISC-V implementation with superior performance, power and area (PPA). Our self-developed processors GreenRio has emerged as the most complex and feature-rich RISC-V architecture among the 600+ designs submitted to *OpenMPW*. We hope GreenRio can serve as an pioneer in demonstrating and perfecting the open design methodology. Its goals can be summarised as follows:

- Build a RISC-V processor from scratch that is fully compatible with the OpenEDA flow
- Drive the growth of both chips and EDA tools through a real and reasonable design
- Facilitate chiplets and multi-physics through innovation in both fabrication flow and models
- Conduct researches in Open-Chip field through a meaningful and non-toy-like design instance

Through this process, we try to optimize the OpenEDA along with the RISC-V CPU together, putting explorations in the flow at various stages.

The rest of the paper is organized as follows. Section2 discusses the history of GreenRio's development. Section3 analyses the gap between open and proprietary EDA tools. Section4 descripes GreenRio co-design experience with open toolchains and future work. Section5 concludes this paper.

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GreenRio Development History

The features of the GreenRio were chosen such that the micro-architecture could serve as a reference in both the EDA and RISC-V domains. Therefore, we equipped GreenRio with morden processor characteristics to enhance its optimizability and extensibility. Figure 1 depicts GreenRio's milestone. GreenRio1.0 is a 7-stage, dual-issue, out-of-order (OoO) processor. We demonstrated it in the efabless *OpenMPW-7* program[1] using the *Skywater 130nm* process. We present the first version of GreenRio at the Workshop on Open-Source EDA Technology (WOSET)[3] as well as RISC-V Days Tokyo 2022 Autumn[2]. In order to make OpenEDA more adaptable to increasingly complex chips and identify pain points in current design flow, Greenrio 2.0 adds more hardware supports allowing for running applications. It supports the RV64ICMA unprivileged ISA, as well as the privileged ISAs Zicsr, Zifencei, and Sfence.vma. Furthermore, it also allows for Supervisor (S), Machine (M), and User (U) modes.

GreenRio2.0 has won the ISSCC Code-a-Chip competition[3] and is becoming a benchmark in the OpenEDA domain. Its achievements also have the potential to inspire the RISC-V community and drive growth for open-source semiconductor fabrication.

Future work includes enhancing the performance and scalability of GreenRio while further optimizing EDA tools. To achieve this, we plan to add support for the vector extension, enabling GreenRio to become a multi-core architecture. Additionally, we are developing a high-performance SRAM compiler to improve the memory system of open PDK. These efforts are driven by our goal to position GreenRio as a cutting-edge solution for OpenEDA and RISC-V, and to explore new possibilities for future research.

Experience in OpenEDA

One of the challenges that the EDA community faces is the gap between open and proprietary EDA tools in terms of quality of results (QoR) and runtime. To evaluate this

[1] https://github.com/b224hisl/rioschip
[2] https://riscv.or.jp/en/risc-v-days-tokyo-2022-autumn-en
[3] https://github.com/0616ygh/GreenRio2

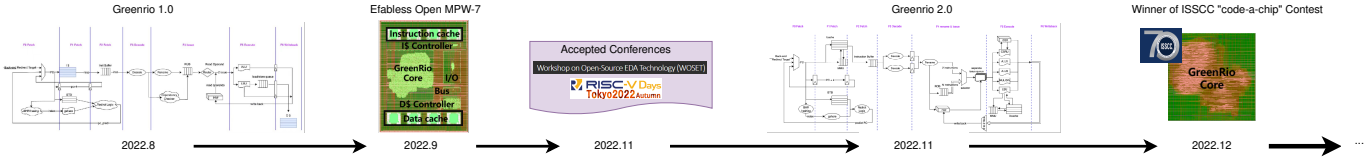

Figure 1: *Timeline of Greenrio*

Table 1:

RISC-V Processors in Open Design Methodology

Picorv32a	EH1	IBEX	Count	biriscv	GreenRio
ISA	RV32	RV32	RV32	RV32	RV64
Pipeline	6	2or3	2or3	6or7	7
Issue Width	single	single	single	dual	dual
Out-of-Order	✗	✗	✗	✗	✓
Gate Count(K)	17	10	20	67	250

Table 2: *OpenEDA vs Proprietary EDA Tools*

	OpenLane	Proprietary EDA Tools	Gap
Synthesis Run Time	6m12s	4m04s	1.5X
Gate Count	53K	33K	1.6X
Placement & Routing Time	1h58m	43m	2.7X
Die Area	2.02mm^2	1.24mm^2	1.6X
Leakage Power	209nW	152nW	1.4X
Placement Density	32%	45%	1.4X
Best Clock Frequency	80MHz	110MHz	1.4X

Timing Corner: sky130_fd_sc_hd_tt_025C_1v80
Timing Closure: No hold and setup violation

gap, we utilized the proprietary tools and *OpenLane*[4][4] in the sign-off flow of GreenRio. Table 2 displays the results. The area optimization performance using *OpenLane* was 60% of that achieved using proprietary tools when clock frequencies were identical. Due to the differences in optimization strategies, *Yosys* and proprietary tools produced netlists with varying gate counts.

Therefore we demonstrated that OpenEDA tools could achieve acceptable QoR while having advantages in terms of transparency, modifiability, and accessibility. These advantages are particularly beneficial for DSE. We also have identified areas of improvement for OpenEDA, including *System Verilog* support, high-density placement and routing (PNR), logic equivalence check (LEC) attributes, antenna violation remediation, and PPA optimization. Moreover, the implementation of early checks to alert users of inappropriate parameter usage is also crucial in preventing premature termination or endless execution during the process.

Machine-driven DSE

The design complexity of GreenRio has revealed the convergence difficulty in the Open-Chip flow. Although the application of machine-driven techniques in EDA can trace its history back to the 1990s[5], the recent breakthrough of machine learning (ML) and the increasing complexity of electronic systems have aroused more interest in incorporating ML to solve EDA tasks.

In order to generate high-quality solutions for chips' physical implementation, we integrated *FlowTune*[6], a ML-based decision making framework for synthesis optimization, to this flow. Nevertheless, to speed up the chip development cycle and facilitate DSE in OpenEDA, we gathered a comprehensive list of user problems that arise during program execution and built a *Solution-inspiring Error Log System* by embedding potential solutions in the error logs. We won the *Excellent Effort Award* in the *OpenROAD-7nm-contest*[5] for these two contributions[6]. In future, we plan to construct the first open-source data-set for RISC-V VLSI CAD, thereby creating more efficient and customized chip designs.

Conclusion

The RISC-V and open-source EDA ecosystem reduces the barrier to entry for silicon designs[7]. Our experiences in the *efabless MPW-7* shuttle and Code-a-Chip competition have verified the feasibility of our full-stack design approach for modern processors. Through GreenRio, we also optimize development in the EDA field and foster more streamlined development methodologies.

Leveraging the power of open-source will enable the global community to collectively push the frontiers of hardware innovation. We hope GreenRio act as a catalyst towards the industrialization of open-source semiconductor fabrication in the RISC-V community.

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