Kameleon, a RISC-V Based 2-core Multi-accelerator Academic SoC

https://drac.bsc.es/en

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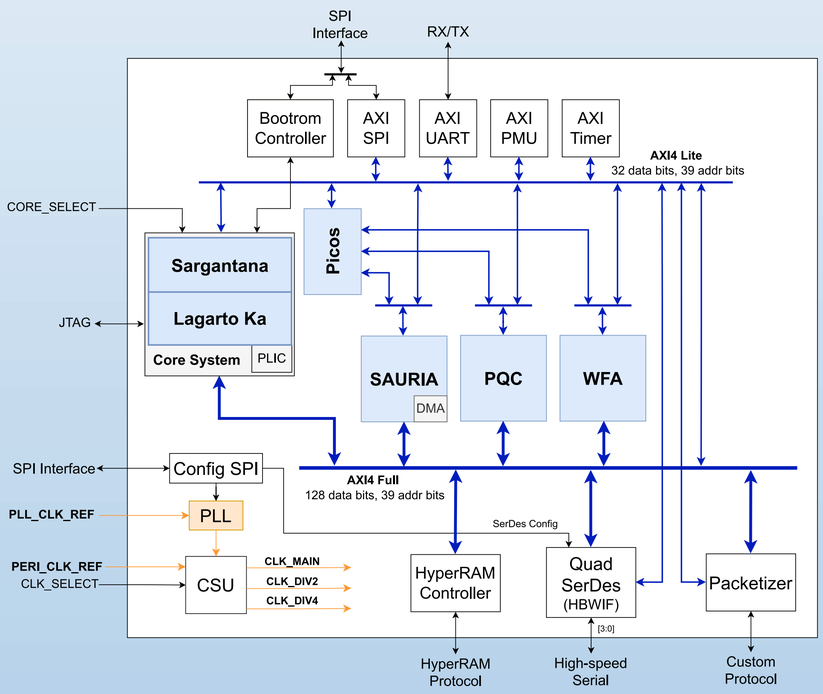
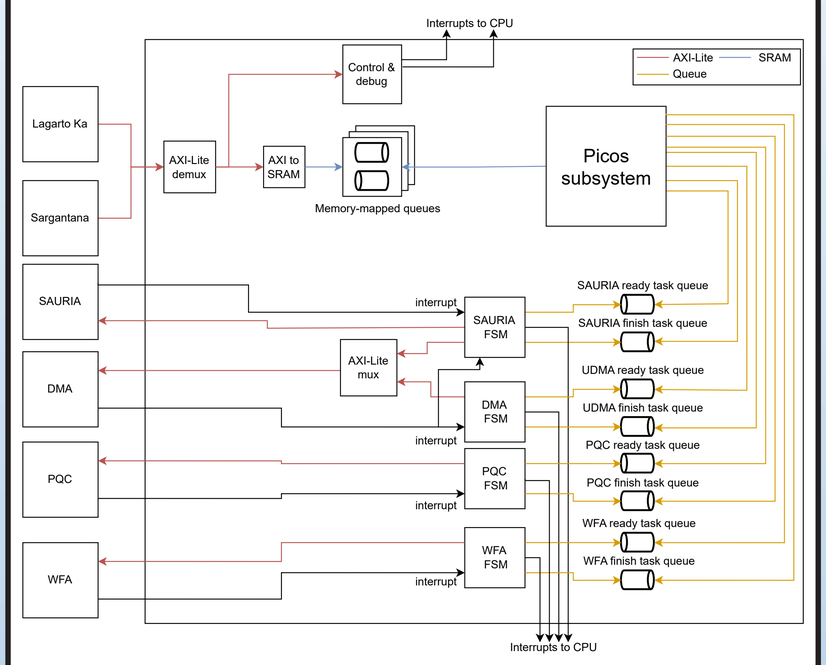
Overview

Kameleon, the final chip of the DRAC project, is an SoC based on the RISC-V ISA. It integrates two cores, one of them with an out of order back-end, and four accelerators.



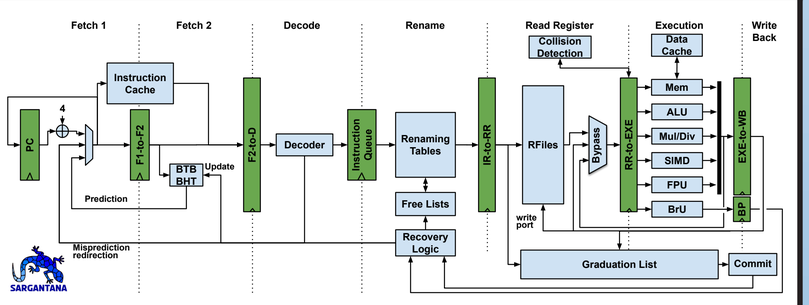
- Sargantana: In order general purpose processing core.
- Lagarto Ka: Out of order general purpose processing core.
- PQC: Hardware cryptography accelerator for the Classic McElice Key-Encapsulation Mechanism.
- SAURIA: Systolic Array tensor Unit for aRtificial Intelligence, designed towards autonomous driving.
- Picos: Hardware accelerated task scheduler.
- WFA: Hardware accelerator for the Wavefront alignment algorithm, for genomics study.
- PLL: Generating up to 2 GHz internal frequency.
- 4 line Serializer/Deserializer, up to 8 Gbps transfer rate.

Picos



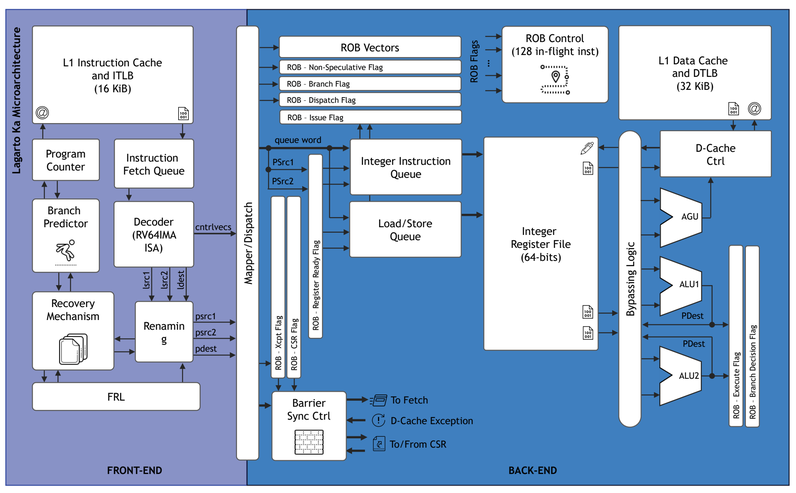
- Heterogeneous task scheduler for CPU and accelerator tasks, CPU tasks can be any piece of code, accelerator tasks must be the implemented application.
- Support for up to 8 concurrent threads creating tasks.
- Capable of holding 256 in-flight tasks with dependencies.
- Capable of holding 640 unique and 1024 non-unique dependencies for all in-flight tasks.
- Independent finite state machines to manage task execution on each accelerator.
- Individual interrupt for each CPU.

Sargantana



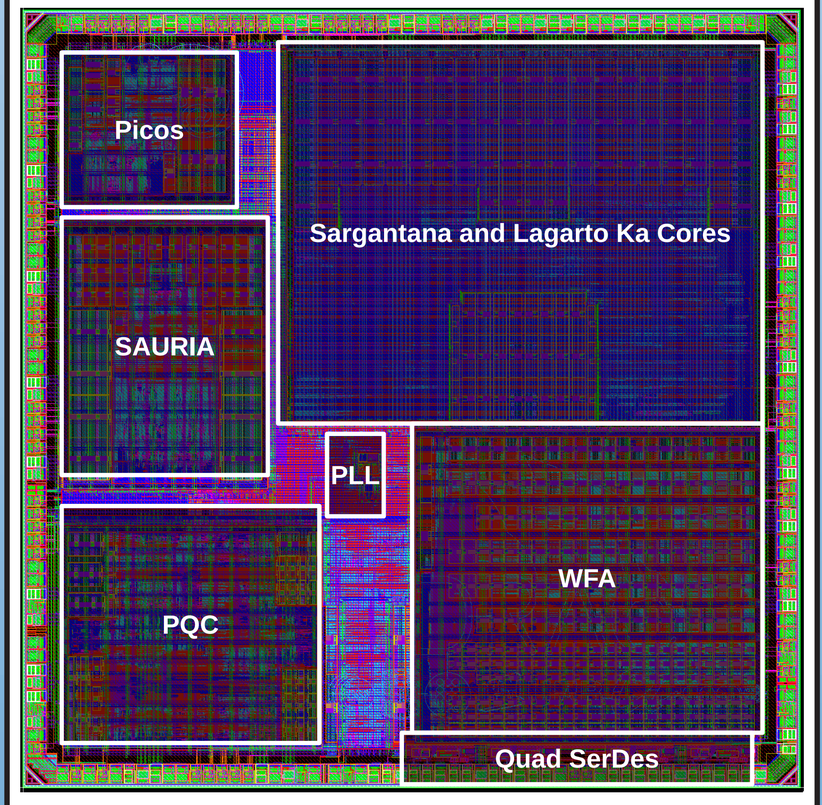
- 64-bit In-order processing core implementing RV64G ISA.
- Capable of reaching frequencies of 1 GHz.
- Capable of reaching 0.716 IPC in the RISC-V benchmark and 0.766 IPC in the EEMBC benchmark.
- Greater or equal performance than other state-of-the-art academic chips. Compared againts ariane (ETH), CVA6 (OpenHW group), Rocket (UC Berkeley) and Riscy (MIT).

Lagarto Ka



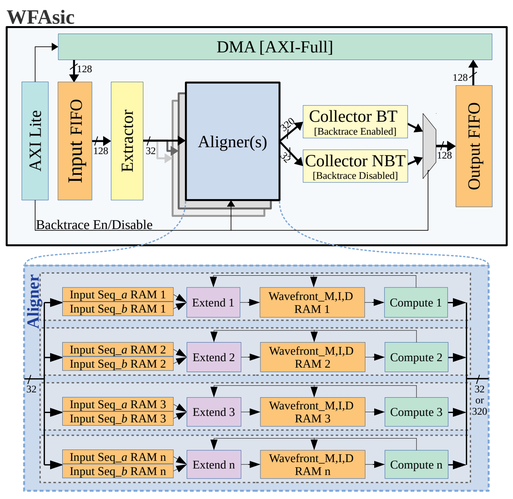
- 2-way 64-bit Super-scalar Out of Order General purpose processing core.
- Supports the I, M and A extensions of the RISC-V ISA.
- Formed by two main blocs, a sequential front-end and an out of order back-end.
- Design focused on reducing energy consumption.
- Capable of reaching 0.897 IPC in the RISC-V benchmark and 0.988 IPC in the EEMBC benchmark.

Physical Design



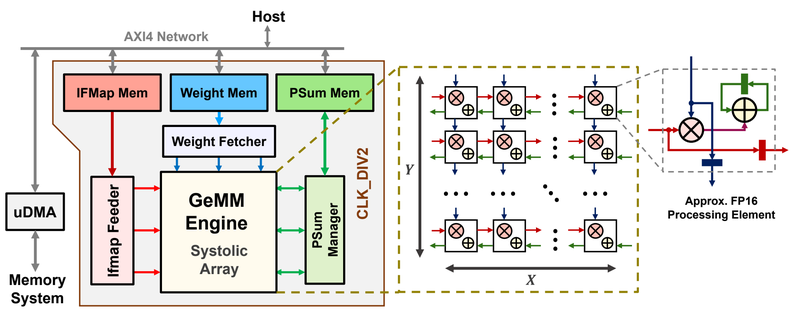
- Globalfoundries' 22nm FDSOI technology.
- 3×3 mm² die with 203 IO pins.
- Kyocera's CERQUAD FP 208 package.
- Area bounded design.
- 11 metal layer design.
- Design made using Cadence tools. Verification done with Cadence and Mentor tools.
- Separated power delivery for the analog IPs to decrease voltage ripple in the digital areas of the chip.
- 0.8 V internal supply voltage, 1.8 V IO supply voltage.

WFA



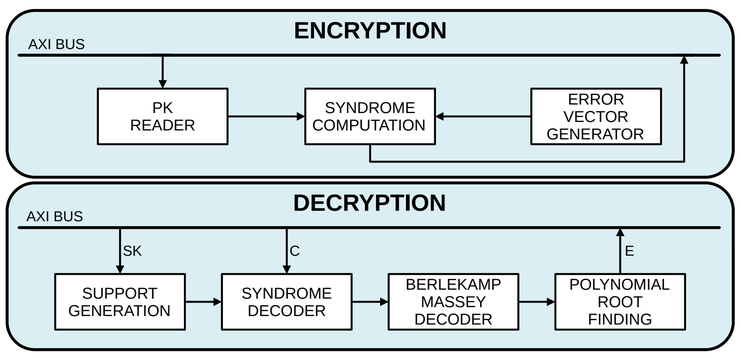
- First ASIC accelerator of the wavefront alignment (WFA) algorithm for pairwise alignment of DNA sequences.
- Supports the alignment of DNA sequences with lengths of up to 10K bases.
- Can detect up to 1K differences between each pair of sequences.
- Contains a configurable backtrace data generator.
- Contains a DMA engine with direct access to the main memory.
- Provides 1076x performance over implementing the algorithm on the Sargantana CPU.
- Capable of reaching 1 GHz work frequencies.

SAURIA



- Energy-efficient neural accelerator for DNN workloads.
- Approximate arithmetic reduces power consumption by 30% with no significant accuracy loss.
- Array size of 8×16 (128 PEs) and FP16 arithmetic precision.
- Capable of reaching 500 MHz work frequencies.
- Peak throughput of 128 GFLOP/s and peak energy-efficiency of 1.41 TFLOP/(s·W).
- Integrated on-the-fly im2col.

PQC



- Post-Quantum Cryptography accelerator for the Classic McElice Key-Encapsulation Mechanism.
- Based on an HLS-Design Approach.
- Encryption/Decryption functionality of security level 1.
- Capable of reaching 1 GHz work frequencies.
- Uses a 255 KB Public Key, a 6.3 KB Secret Key and a 128 B Ciphertext.

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