Open Source RISC-V Advanced Interrupt Architecture (AIA) IP

Francisco Costa
Manuel Rodríguez
Bruno Sá
Sandro Pinto
Centro ALGORITMI/LASI, Universidade do Minho

Abstract

This work describes the design and implementation of an open-source Advanced Interrupt Architecture (AIA) IP compliant with the RISC-V AIA specification (v1.0-RC2). We have designed and implemented the core extensions, the Advanced Platform Level Interrupt Controller (APLIC), and the Incoming Message-Signalled Interrupt Controller (IMSIC) IPs. These IPs being integrated into a RISC-V CVA6-based (64-bit) SoC. We conduct a preliminary evaluation of the system and present a hardware report. Our work showcases the feasibility of implementing RISC-V AIA and establishes a base for future research and development. We will open-source our IP to foster collaboration among the RISC-V community.

RISC-V AIA in a nutshell

AIA Control and Status Registers
- Provide a means to interact with the IMSIC IP;
- Provide a mechanism to change the major interrupt's priority;

Incoming Message-Signalled Interrupt Controller
- Consists of a set of interrupt files;
- Supports Message Signalled Interrupts (MSIs);
- Provides for virtualization support;

Advanced Platform Level Interrupt Controller
- Consists of a set of interrupt domains;
- Can be in one of two operation modes:
  - Direct mode: Acts as a replacement for the RISC-V PLIC;
  - MSI mode: Acts as a translator of wired interrupts to MSIs.

Evaluation

Functional Validation
- Run a set of unit tests to validate basic AIA operations;
- Run a bare-metal application with the developed AIA drivers;
- Execute Linux to complete the hardware validation;
- Conduct the same tests while introducing the Bao hypervisor between the hardware and the application

Hardware Resources

<table>
<thead>
<tr>
<th>SoC Configuration</th>
<th>Resource</th>
<th>HW Cost (Genesys2)</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLIC (1)</td>
<td>LUT</td>
<td>74541 / 203800</td>
<td>36.58</td>
</tr>
<tr>
<td></td>
<td>FF</td>
<td>51446 / 407600</td>
<td>12.62</td>
</tr>
<tr>
<td>APLIC (2)</td>
<td>LUT</td>
<td>81480 / 203800</td>
<td>39.98</td>
</tr>
<tr>
<td></td>
<td>FF</td>
<td>54334 / 407600</td>
<td>13.33</td>
</tr>
<tr>
<td>AIA IMSIC w/ 1 VS file + APLIC (3)</td>
<td>LUT</td>
<td>84610 / 203800</td>
<td>41.52</td>
</tr>
<tr>
<td></td>
<td>FF</td>
<td>55735 / 407600</td>
<td>13.67</td>
</tr>
</tbody>
</table>

Post-synthesis hardware utilization results for single core CVA6 SoC targeting a Genesys 2 FPGA

Interrupt Latency

- Trigger an interrupt at 1 KHz;
- Running the custom benchmark on top of Bao:
  - SoC configuration (1) introduces a latency of ~13 ms;
  - SoC configuration (2) introduces a latency of ~7 ms;
  - SoC configuration (3) has a latency near the native value.