Accelerating RISC-V Developments Through Network-on-Chip (NoC) Automation

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Drivers for Network-on-Chip Physical Awareness

Computing sophistication and complexity continue to skyrocket:
- Exponential transistor count growth over the last decades
- Number of logical cores and I/Os quadrupling or exponential growth in increased connectivity
- Overall NoC complexity
- More sub-systems meaning more time user spent manually

Physical effects are pronounced at 16nm and below:
- SoC contains multiple Networks-on-Chip (NoC), accounting for 10-12% of silicon
- Drivers for Network-on-Chip Physical Awareness
  - Economics of using silicon-proven NoC IP versus in-house development
  - Shrinking project schedules despite increasing project complexity
  - Further impact expected at the more advanced nodes: 7nm, 5nm, 3nm, etc.
  - Power, Performance, and Area (PPA) factors impacting NoC and SoC iterations
  - SoCs contain multiple Networks-on-Chip (NoCs), accounting for 10-12% of silicon

Manual Flow With Some Layout Awareness & Guidance

Manual update of constraints for P&R
- Engineering efficiency
- Over manual iterations
- Up to 5X faster physical closure
- Reduces NoC IP power due to less pipeline logic and fewer LVT cells
- Shrinks interconnect area by 15% or more (vs pipeline over-provisioning)
- Early physical awareness for faster convergence without re-designs

Physically Aware NoC IP with Pipeline Optimization

Arteris FlexNoC 5 Physically Aware Network-on-Chip IP

Up to 5X faster physical closure over manual iterations
- Enables physical awareness for silicon-convergence ethereal designs
- Allows physical awareness to be leveraged in many more design scenarios
- Reduced NoC IP power due to less pipeline logic and fewer LVT cells
- Topology visualization directly on floorplan with user-selectable filter options
- Reduces hours of work to minutes, removing iteration loops
- Source: "Microprocessor Trend Data – 50 Years", Karl Rupp, Feb 2022

Can’t Cross Advanced Node SoCs in One Clock Cycle

Physical distance impacts the number of pipeline stages
- Transport delay = \( F \) (Foundry, routing stack, type of driving cell, process voltage, temperature, ...)

We are happy to share that we are partnering with Arteris to use NoCore and FlexNoC in our next-generation product. The combination of performance and features made it a great choice for both our AI chips and our high-performance RISC-V CPUs. The Arteris team and IP solved our on-chip network problems so we can focus on building our next-generation AI and RISC-V CPU products.”