Accelerating RISC-V Developments Through Network-on-Chip (NoC) Automation

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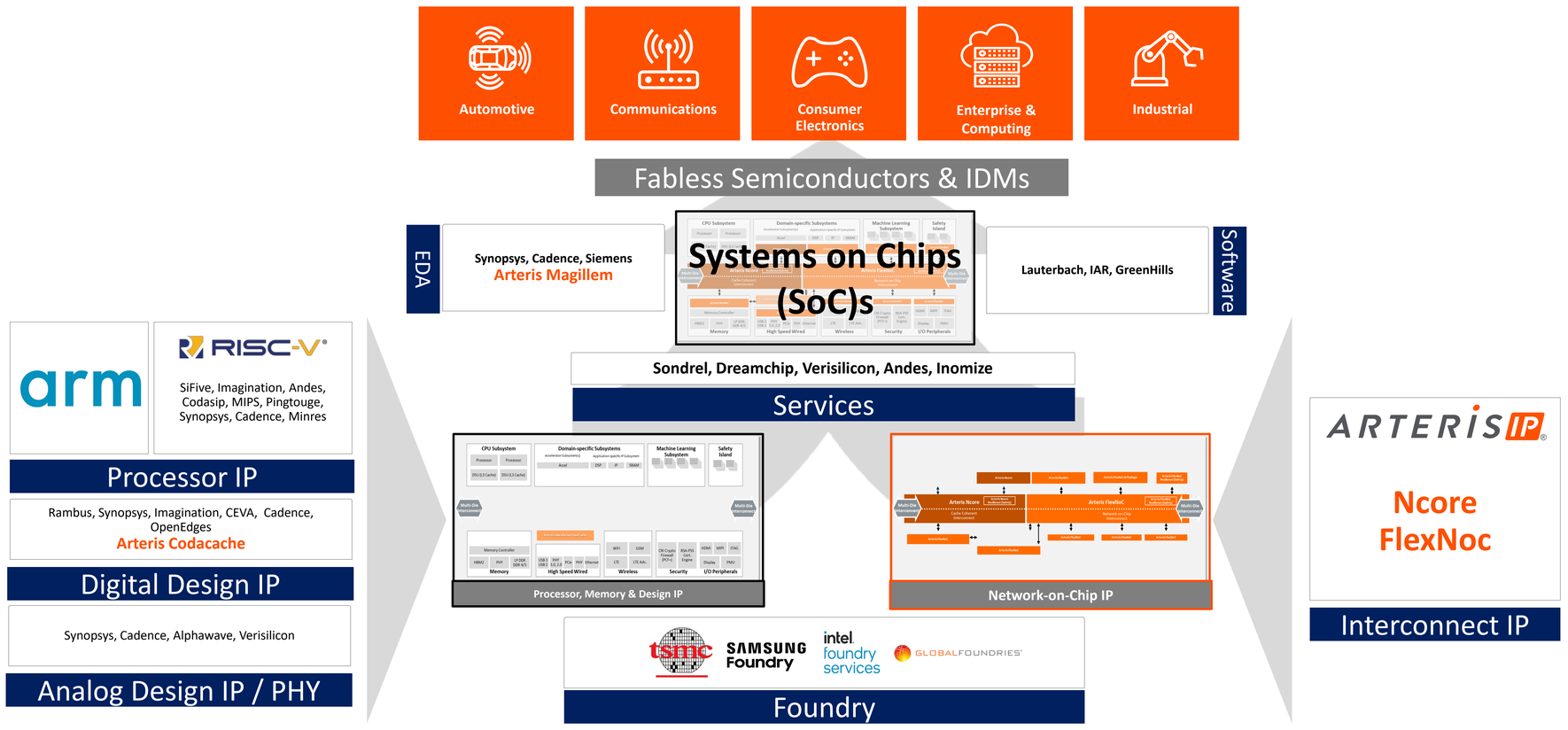


Drivers for Network-on-Chip Physical Awareness

Computing sophistication and complexity continue to skyrocket

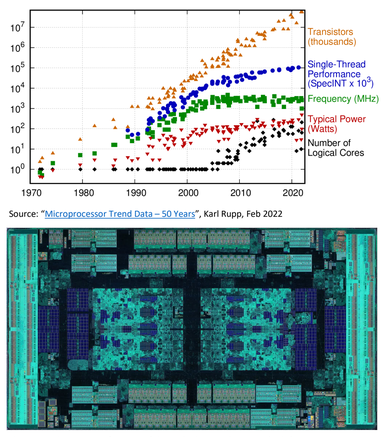
- Exponential transistor count growth curve → increased data traffic
- Number of logical cores → quadratic/exponential growth in interconnect connectivity
- Overall SoC complexity → more sub-systems requiring their own connectivity

Physical effects are pronounced at 16nm and below

- SoCs contain multiple Networks-on-Chip (NoCs), accounting for 10-12% of silicon
- Power, Performance, and Area (PPA) factors impacting NoC and SoC iterations
- Further impact expected at the more advanced nodes: 7nm, 5nm, 3nm, etc.

Market pressures put a squeeze on project realities

- Shrinking project schedules despite increasing project complexity
- Economics of using silicon-proven NoC IP versus in-house development
- Shortage of trained system IP engineers → driving the shift to flexible IP automation

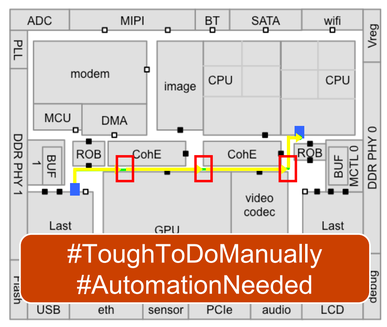


Source: "Microprocessor Trend Data – 50 Years", Karl Rupp, Feb 2022

Source: Techspot, A Brief History of the Multi-Core Desktop CPU (2021)

Can't Cross Advanced Node SoCs in One Clock Cycle

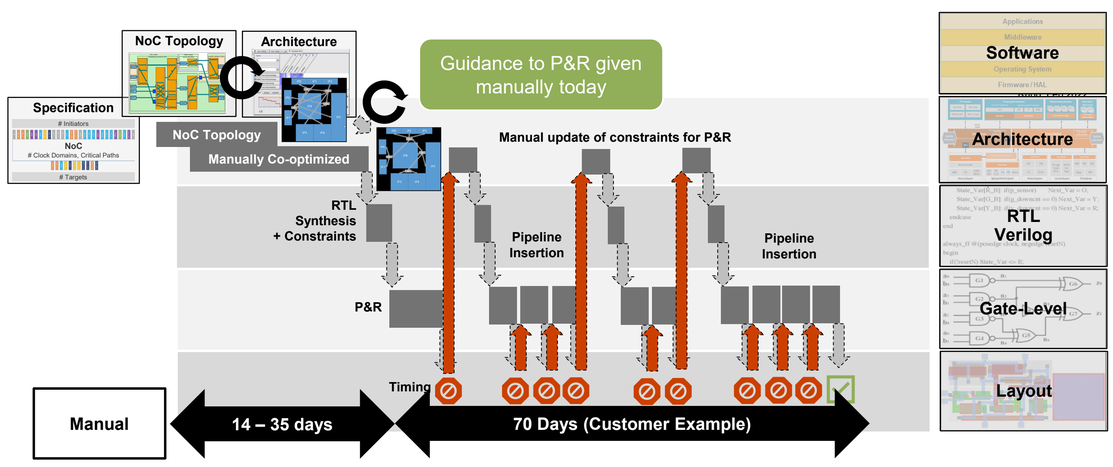
Physical distance impacts the number of pipeline stages



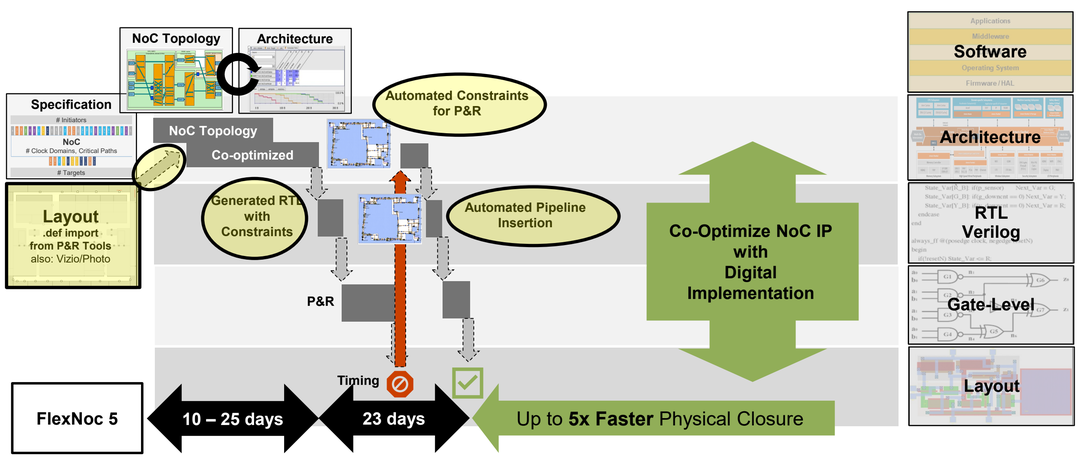
- Endpoint (NIU)
- Single NoC cycle path
- Pipeline

Transport delay = F (foundry, routing stack, type of driving cell, process voltage, temperature, …)

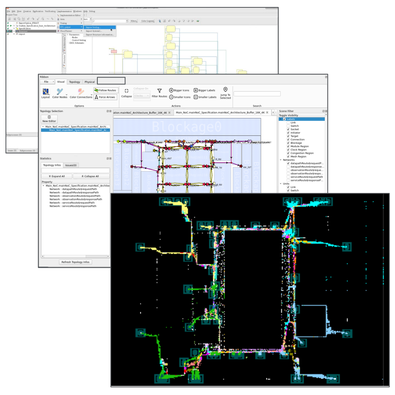
Manual Flow With Some Layout Awareness & Guidance



Physically Aware NoC IP with Pipeline Optimization



Arteris FlexNoC 5 Physically Aware Network-on-Chip IP



Note: Multiple patents granted; additional patents pending

Up to 5X faster physical closure over manual iterations

- Early physical awareness for faster convergence without re-designs
- Allows place and route tools a better starting point
- Shrinks interconnect area by 15% or more (vs pipeline over-provisioning)
- Reduces NoC IP power due to less pipeline logic and fewer LVT cells

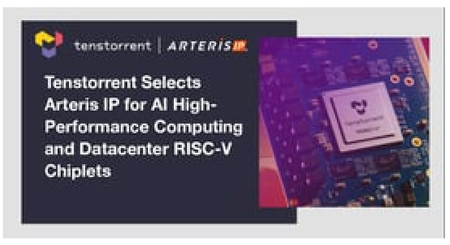
Engineering efficiency

- Reducing hours of work to minutes, removing iteration loops
- Automated NoC element preparation for the timing closure process
- Seamless integration of GUI windows for new physically aware flow
- Topology visualized directly on floorplan with user-selectable filter options

Other enhancements

- Automates import/export of NoC configurations with Arteris Magillem
- Debug and Trace with ATB 128b and timestamps support
- AMBA 5 support of DVM 8.1 (Device Virtual Messaging)
- Re-order Buffer Optimization benefitting Cache and DRAM connectivity

Enables SoC developers to build NoCs with faster physical closure!



> *We are happy to share that we are partnering with Arteris to use Ncore and FlexNoC IP in our next-generation product, The combination of performance and features made it a great choice for both our AI chips and our high-performance RISC-V CPUs. The Arteris team and IP solved our on-chip network problems so we can focus on building our next-generation AI and RISC-V CPU products."*

tenstorrent

Jim Keller, CEO of Tenstorrent.

ARTERIS IP