Floating Point HUB Adder for RISC-V Sargantana Processor

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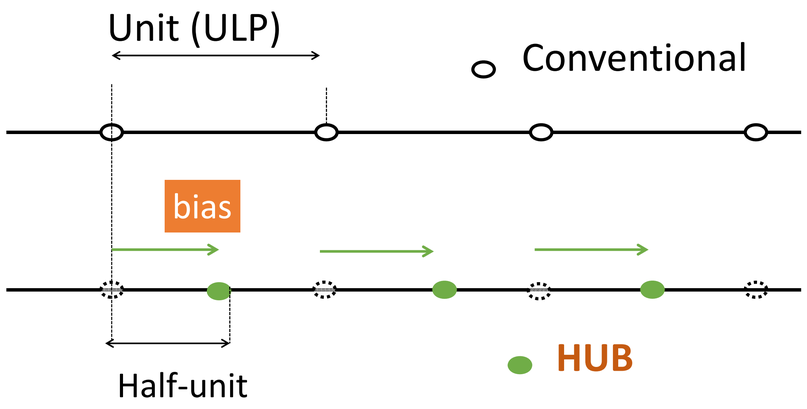
HUB FP format (*Half Unit Biased format*)



$$M_x = (M_{x_0}, M_{x_{-1}}, M_{x_{-2}}, \cdots, M_{x_{-f}})$$

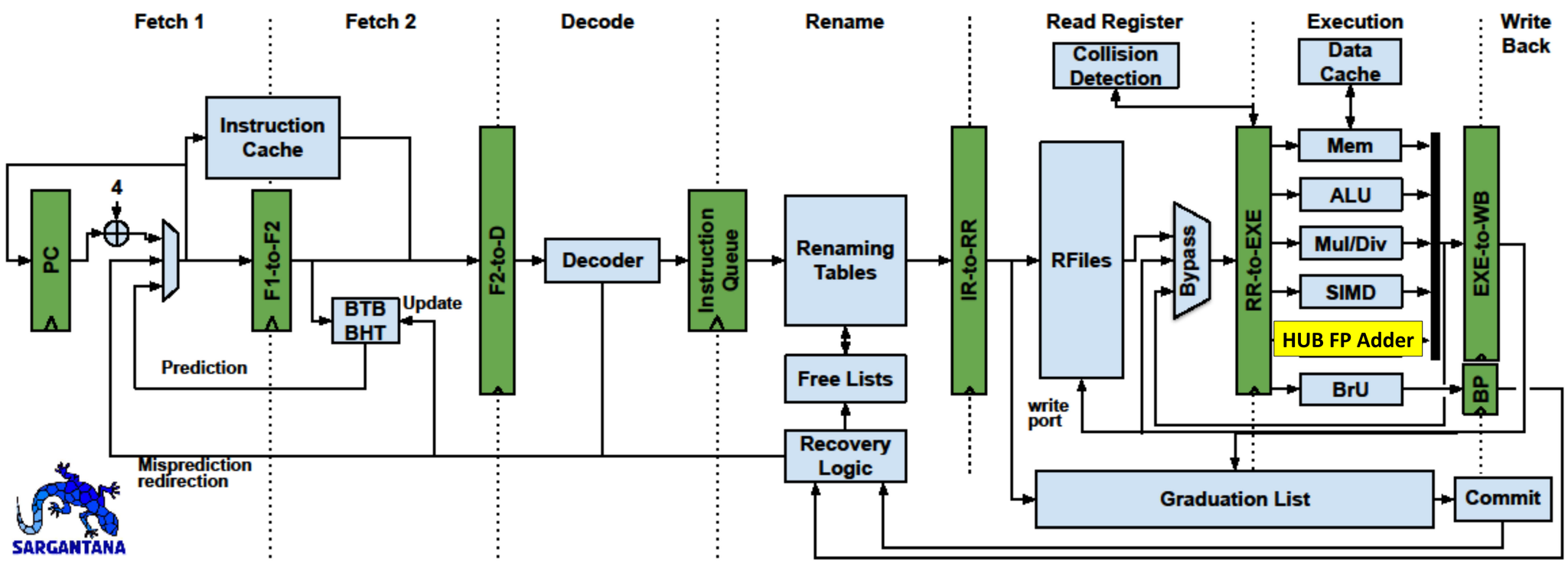
$$M_x = 1 + \left[\sum_{i=1}^{f} M_{x_i} \cdot 2^{-i}\right] + 2^{-f-1}$$

ILSB

$$M_x = 1.M_{x_{-1}} M_{x_{-2}} \cdots M_{x_{-f}} 1$$

bias

SARGANTANA processor

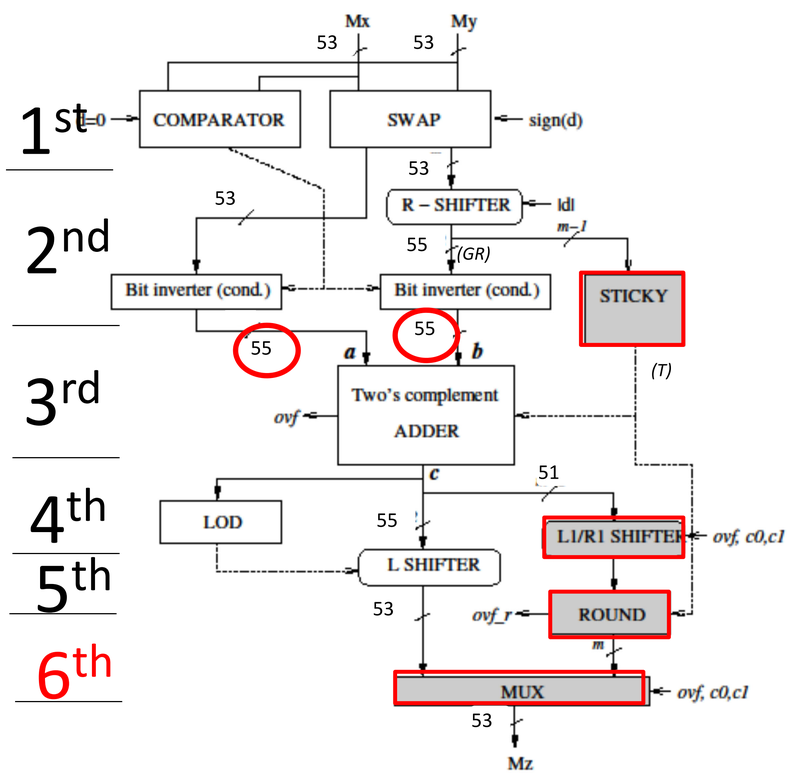


***Advantages of HUB format**:*

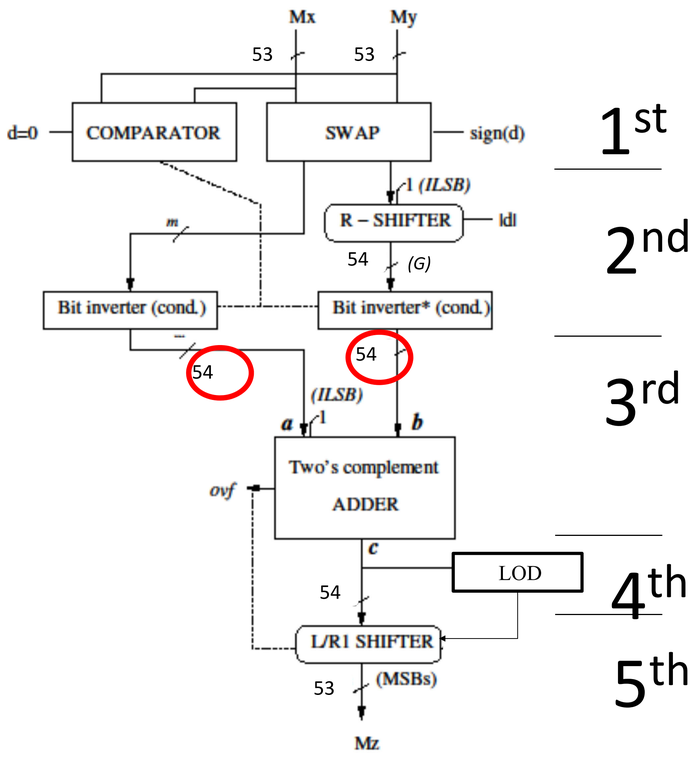
- *Two's complement → bit-wise inversión*
- *Round to nearest → by truncation*
- *Same precision and accuracy as its conventional counterpart*
- *One less bit in Data path for round to nearest adders*
  - *1.xxxxx…xxxGRT (conventional)*
  - *1.xxxxx…xxxG1 (HUB)*
- *Sargantana:*
  - *No sticky calculation (T), No rounding bit (R)*
  - *No rounding stage → Save one pipeline stage*

Main features of Sargantana processor:

- *64-bit in order Linux-capable RISC-V CPU*
- *Implements the RV 64 ISA*
- *Uses SIMD unit*
- *RVV 0.7.1 vector extensión*
- *Custom application specific instructions*
- *7-stage CPU pipeline with register renaming, out-of-order write-back and a non-blocking memory accesses.*
- *16KB InstL1 32KB DataL1cache, 512KB L2*



Round to Nearest FP Standard adder
64-bit precisión (53 bit mantissa)



FP HUB adder
64-bit precisión (54 bit mantissa)
Round to nearest by truncation

CONCLUSIONS:

✓ The FPU adder of the RISC-V Sargantana processor has been replaced by a new adder with HUB numbers.

✓Number of pipeline stages decrements (6 to 5 stages).

✓25% of area reduction (3110µm^2 vs 2332µm^2).

✓Absence of denormals, rounding stage and sticky calculations.

NEAR FUTURE:

✓It is a first step to extend the HUB format to all RISC-V arithmetics operations.