RISC-V based Programming Model of a Computational SRAM Vector Processing Unit

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Von Neumann Bottleneck

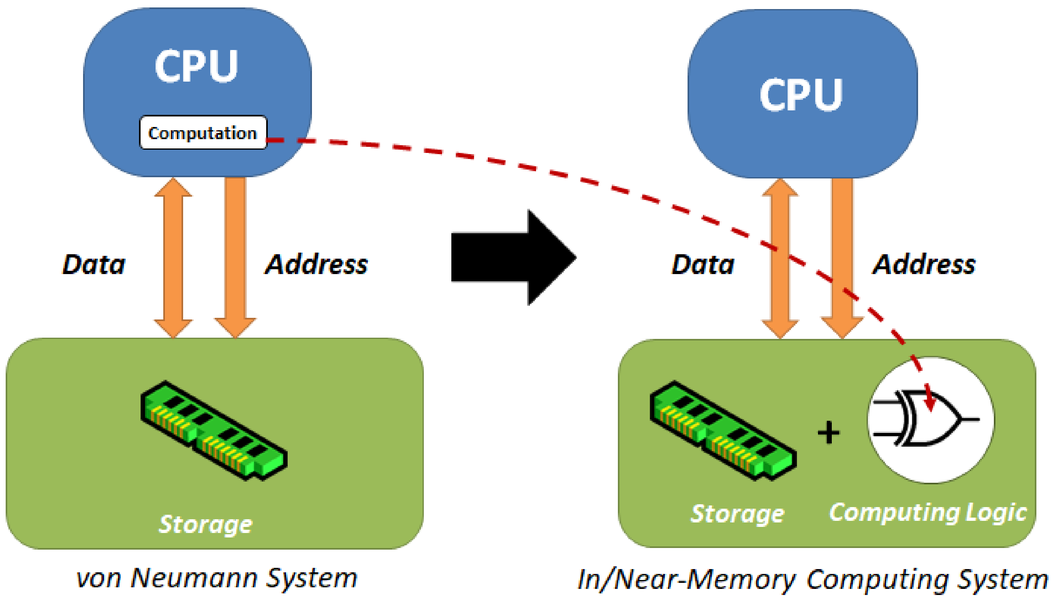


Fig 1. In/Near Memory Computing Architecture

- Integrating computation inside or near memories
- Reduce data transfer between processor and memory
- Increase the system performance and reduce energy consumption

Computational SRAM (C-SRAM)

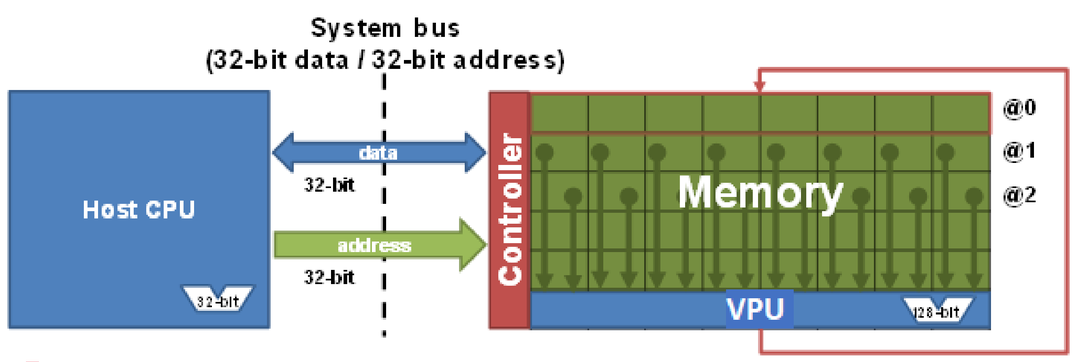


Fig 3. C-SRAM Architecture

- **Compute where data is located**
  - ➢ Vector computing
  - ➢ Low-latency memory
- **Rethink micro-architecture and compilation**
  - ➢ Specific instructions
  - ➢ Compile-time dynamic allocation
- **Two design methodologies**
  - ➢ Full custom solution
    - Change the memory bitcell
    - Specific in- and near-memory functions
  - ➢ Automated solution
    - Based on SRAM cut generated from SRAM compilers
    - Near memory functions only
    - Better Time-to-market

Category	Width (bits)	Mnemonic	Description
Memory	CSRAM Line	copy	Copy a line inti another
	8,16,32	copyeq, copygeq, copygt, copyleq, copylt, copyneq	Conditional Copy
	8,16,32	bcast	Broadcast 8,16 or 32-bit value to whole line
	32,64	hswap	Horizontal 32 or 64-bit word swap
Logical	8,16,32	slli, srli	Shift Left or Right Logical Immediate
	CSRAM Line	and, nand	Logical AND
	CSRAM Line	or, nor	Logical OR
	CSRAM Line	xor, xnor	Logical XOR
Arithmetic	8,16,32	add	Arithmetic Addition
	8,16,32	sub	Arithmetic Subtraction
	8,16,32	cmp	Comparison
	8	mullo, mulhi	Arithmetic 8-bit integer multiply
	8	maclo	Arithmetic 8-bit integer multiply-accumulate

Table 1. C-SRAM Instruction Set Architecture

C-SRAM Programming Model

A C-SRAM instruction is composed of 3 elements that must be encoded on the bus transaction:

- The opcode defines the C-SRAM operation
- The source addresses define the memory vector-lines that store the operands
- The destination address defines the memory vector-line that stores the result

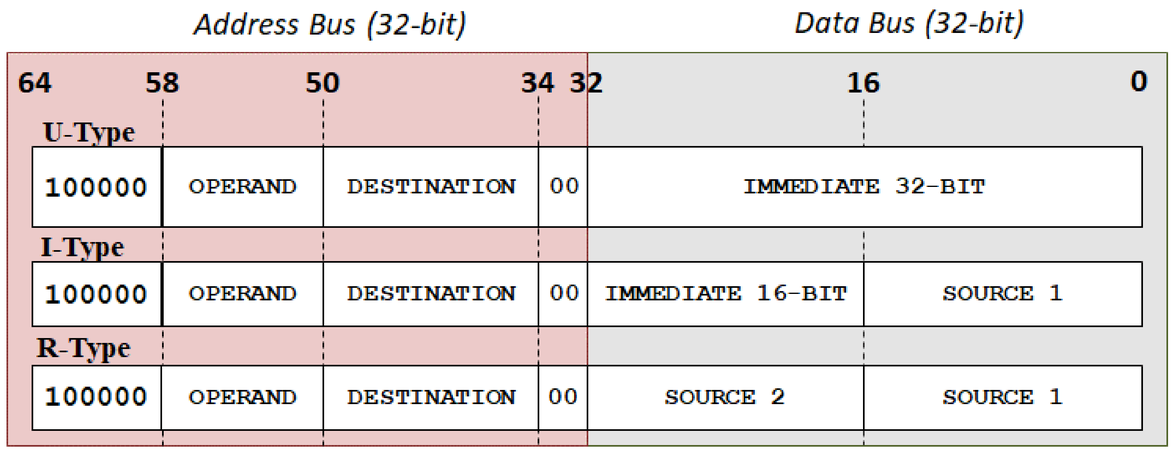
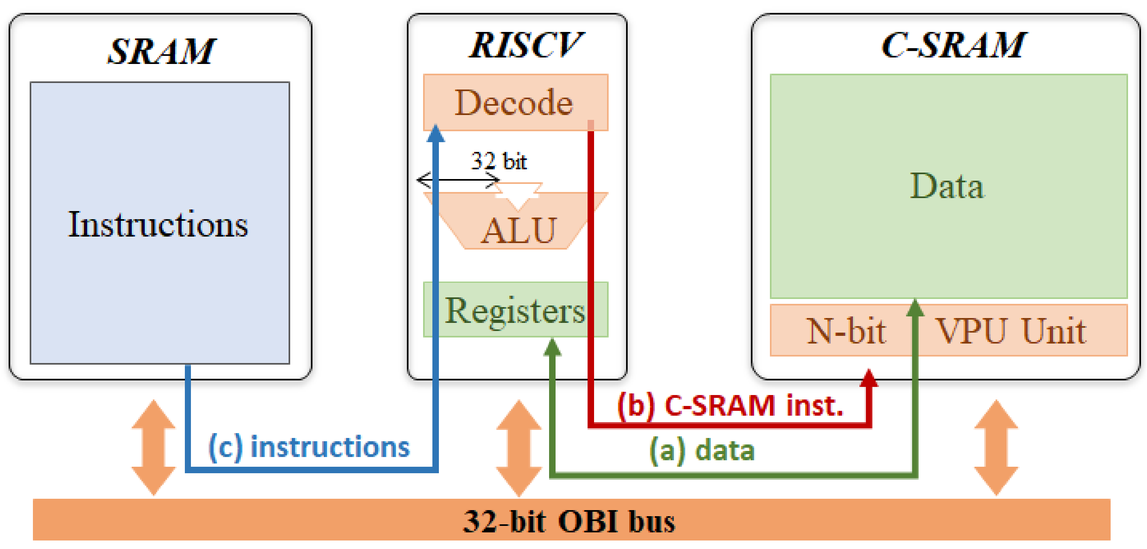


Fig 2. C-SRAM 64-bit Instruction Formats



(a) **Data Transfer:** *32-bit load/store conventional memory access*
(b) **C-SRAM instructions:** *64-bit **STORE** instruction encoding C-SRAM operation & operands*
(c) **Program Code:** *load/store, CPU scalar compute, C-SRAM vector compute, branch, etc*

Fig 4. C-SRAM System Communication Protocol

- The communication protocol that defines the interaction between the C-SRAM and the host processor, and manages the transfer of C-SRAM instructions, helps to integrate the C-SRAM circuit into an existing system without changing all its architecture
- The host processor runs the control part of the program, while the C-SRAM runs the main workload.
- We propose to use the '***STORE***' instruction to represent a C-SRAM instruction, where the C-SRAM operation and operands are encoded inside the registers of the '***STORE***' instruction,

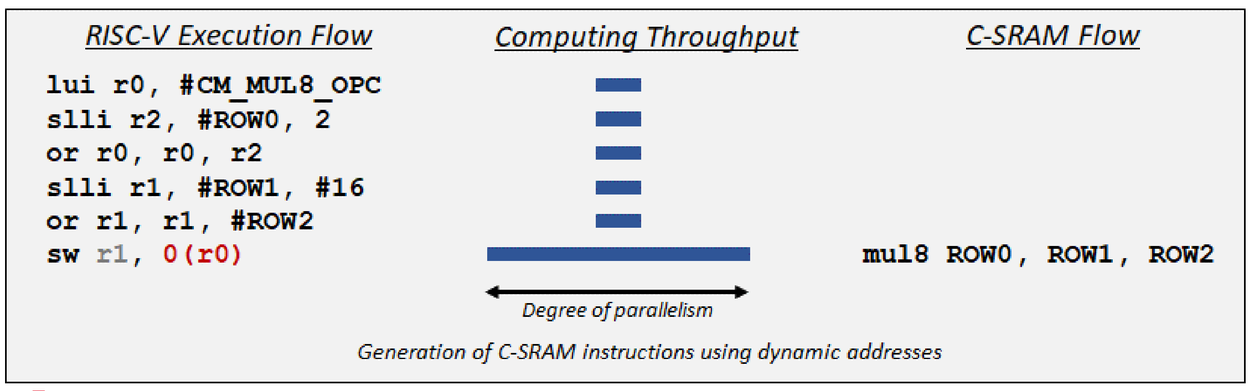


Fig 5. C-SRAM generated instruction

RISC-V based Software Tool Chain

To support the proposed programming model, we have developed a software stack:

- **A QEMU-based plugin emulator**
- **A RISC-V C cross-compiler and debugger**
- **A source-to-source compiler used to generate C-SRAM instructions**

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