CEA/LIST/DSCIN/LFIM

A tool for innovative interleaved execution and compilation scenarios : HybroGen

Why should we generate binary code at runtime ?

Computing architectures are complex

Complex memory hierarchy, deep pipelines,

Datasets are complex

Sparse data, indirect values, run-time values

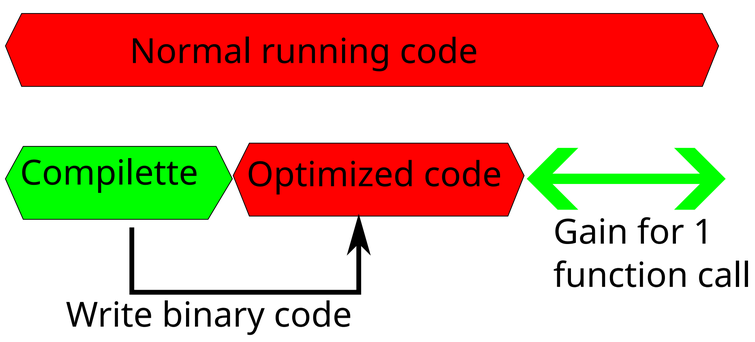
Static Compilers fail to reach peak performances

Binary codes should be adapted to run time conditions

How to modify functions ?

By using a **compilette** which will optimize the code at run-time

A **compilette** is a code generator that will :
- generate the binary code at run-time
- use data characteristics as optimizing parameter
- use the available accelerators



Technical informations

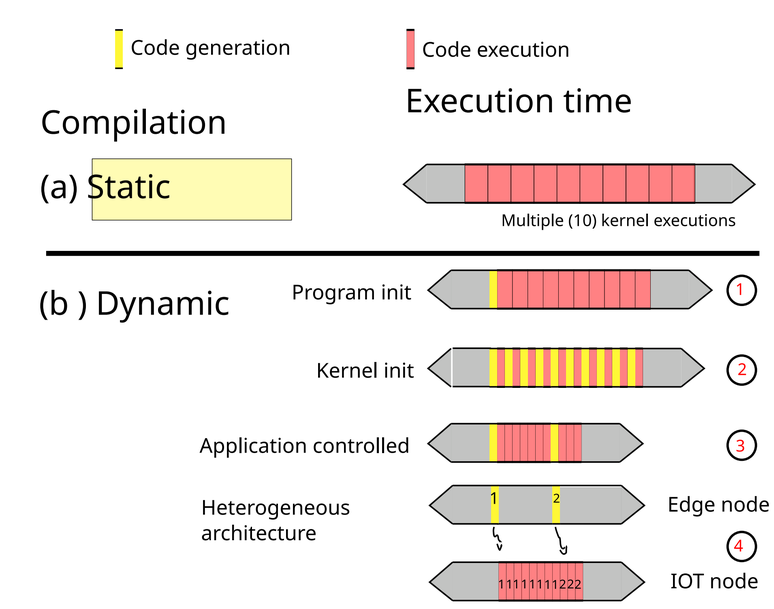
☐ **Supported architectures**

- IBM / Power
- ARM / aarch64
- RISCV /
- CEA / RISC-V + C-SRAM

☐ **Access**

https://github.com/CEA-LIST/HybroGen

Compilation Scenarios



Code generation scenarios:

at the top (a) part, the classical static compilation scheme.
The yellow bar represents the compilation time, the red blocs the kernel execution time.

On the (b) part we represent the interleaving code generation part and kernel execution part for multiple scenario we want to implement.

Demonstrators

At program initialization

Code specialization based on
- Program parameters
- Available accelerators
- Fixed data values

At kernel initialization

Code specialization based on
- Function parameters
- Fixed data values

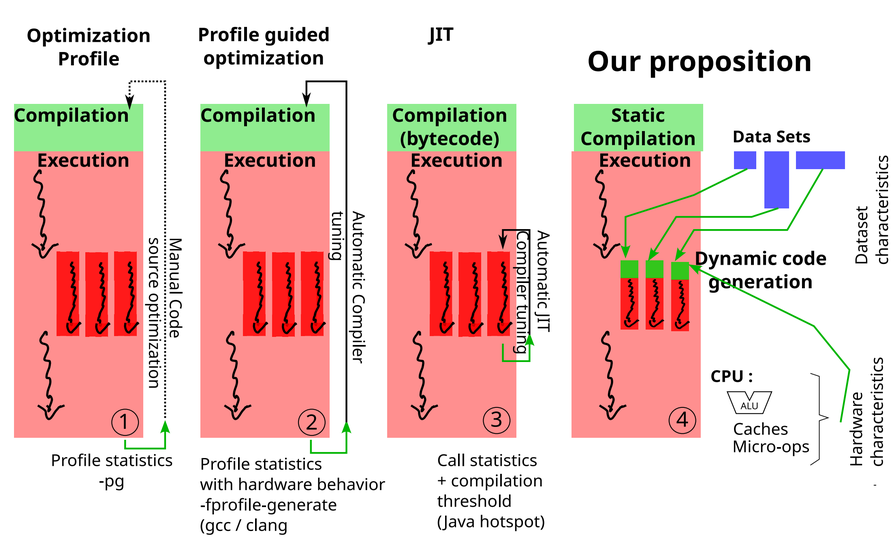
Controlled by program

Code specialization based on
- Program decision (variable precision)
- Security features

Heterogeneous architecture

Code specialization based on
- Multi ISA architectures
- Example on Computational SRAM

State of the art on compilation scenarios



Classical compilation scenarios using iterative profiling compared to our proposition.
- ○1 use static profile gathering and manual optimiation,
- ○ 2 use static profiling with automatic optimization,
- ○ 3 use dynamic profiling to guide JIT optimization.

Our solution use
- dataset characteristics
- and architecture description.

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