# Towards Full Time Protection of an Open-Source, Out-of-Order RISC-V Core

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**Abstract**

*Microarchitectural timing channels enable information transfer between security domains that are supposed to be isolated, bypassing the operating system's security boundaries. They result from shared microarchitectural state that depends on execution in one security domain and impacts timing in another. Since modern ISAs do not specify timing behaviour, they are insufficient to address these channels. The temporal fence instruction was recently proposed as a RISC-V extension that clears the processor's microarchitectural state and thus removes any timing dependence on execution history. It has been demonstrated to be extremely effective at low hardware overhead for in-order RV processors, such as CVA6 [1]. In this work-in-progress, we provide initial insight into the effectiveness and cost of the temporal fence on the open-source, 12-stage, out-of-order RV64GC core OpenC910. We highlight challenges that arise from the out-of-order microarchitecture of OpenC910 and propose an approach that leverages the custom Xthead extension of OpenC910 and minimises the required hardware modifications to enable time protection.*

## Introduction

Security schemes for application-class processors largely rely on memory protection, restricting the memory view of applications using abstractions such as address space virtualisation. However, as Ge et al. [2] argue, and the Spectre attacks have prominently demonstrated [3], this abstraction is insufficient for a principled isolation of applications. There exist timing dependencies between concurrently running applications through shared microarchitectural state, where one application's execution may impact another application's execution time. This timing dependency can be leveraged to bypass the system's security boundaries and covertly transfer information. We refer to such a communication channel as a *timing channel*.

In [4], the authors complement the existing notion of memory protection with *time protection*, a concept assumed at preventing timing channels. As they show, current instruction set architectures (ISAs) do not provide the means to enforce time protection. Hence, they propose to extend the existing ISA abstractions by adding control over shared microarchitectural state.

To address this need, Wistoff et al. [1] propose the temporal fence instruction (`fence.t`), which clears shared microarchitectural components that may constitute a timing channel. Furthermore, they propose a systematic approach for implementing `fence.t` by conservatively clearing all non-architectural state. They demonstrate this approach on CVA6, an in-order, 6-stage RV64GC core [5].

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In this work-in-progress, we prototype the `fence.t` instruction in OpenC910, an out-of-order (OoO) RISC-V core [6]. As we show, this core's high complexity and OoO architecture introduce new challenges that need to be addressed. We propose an approach that combines existing instructions in OpenC910 with an aggressive reset of microarchitectural state to enable time protection with minimal hardware modifications.

## fence.t in Large OoO Cores

### OpenC910

OpenC910 is an industrial, 64-bit, application-class, 12-stage, OoO RISC-V core by T-Head Semiconductor Co., Ltd., implementing the RV64GCXtheadc ISA. It was open-sourced in 2021 under the Apache License and features the custom Xtheadc extension [6].

In the following, we will introduce those elements of the extension that we leverage in this work.

**sync.i Instruction** The Instruction Stream Synchronisation (`sync.i`) instruction serves as a barrier in the instruction stream. It ensures that the instructions preceding it retire before those that follow it.

**dcache.call Instruction** The Data Cache Clear All (`dcache.call`) instruction clears the L1 data cache, writing back all dirty cache lines.

**mrvbr CSR** The Machine Mode Reset Vector Base Address Register (`mrvbr`) holds the address from which the core starts execution after coming out of reset.

## The Problem of Mixed State

OoO execution can introduce new challenges for temporal partitioning of shared microarchitectural state. On a simple in-order core, it is trivial to differentiate between architectural components that must be preserved on a temporal fence (the register files) and the non-architectural state that needs to be cleared (everything else). However, advanced microarchitectural optimisations, such as register renaming, obscure the boundary between architectural and non-architectural state. While the logical registers define the processor's architectural state, their allocation to physical registers constitutes non-architectural state with possible timing implications, harbouring the potential for timing channels. This raises the question of how to preserve the logical registers while bringing the re-namer and physical register file to a deterministic, history-independent state.

In the following, we propose an approach that is minimally intrusive to the hardware: software saves the architectural registers on the stack before `fence.t` conservatively resets the entire register file. Immediately afterwards, software restores the registers by loading them from the stack, resulting in a deterministic physical register layout.

## Hardware Modifications

The key hardware modification is the addition of the `fence.t` instruction, which, on this system, triggers a reset of the entire core except for the control and status registers (CSRs).

## Invocation of fence.t

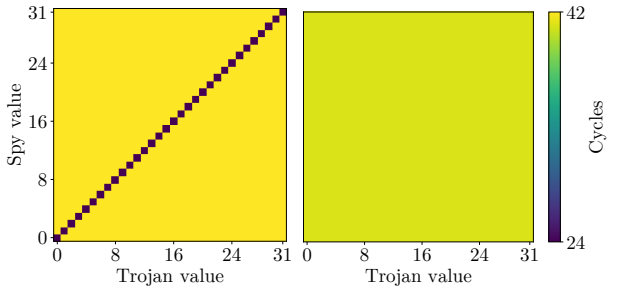
We aim to minimise the required hardware modifications for `fence.t` and reuse existing instructions as much as possible. As a result, a sequence of steps before and after `fence.t` is necessary to preserve computational and architectural correctness.

**Step 1: Save context.** Save the stack pointer (`sp`) at a known location that is not affected by `fence.t`, e.g. the `mscratch` CSR. Write the architectural registers onto the stack.

**Step 2: Define reset vector.** Write the address of the instruction following `fence.t` into the `mrvbr` CSR. Execution after `fence.t` will resume from here.

**Step 3: Clear L1 data cache.** Execute `dcache.call` to write back dirty cache lines.

**Step 4: Execute fence.t.** This resets the entire core except for the CSR files. We guard the `fence.t` instruction by `sync.i` instructions to ensure that all previous steps have been completed.




*a: Unmitigated.* *b: Using `fence.t`.*

**Figure 1:** *The L1 data cache channel on OpenC910.*

**Step 5: Restore context.** Restore the stack pointer and load the architectural registers from the stack.

# Preliminary Results

For initial validation of the proposed mechanism, we port the bare-metal timesec-bench [7] to OpenC910 and run it in RTL simulation. The resulting channel matrix in Figure 1 shows the time for the spy to access different cache lines given a particular value signalled by the Trojan, where any variation along a horizontal cut indicates a channel. Such a channel is clearly present in the unmitigated case, as the diagonal line in Figure 1a evinces. Conversely, invoking `fence.t` when switching between the Trojan and the spy removes all correlations, as shown in Figure 1b.

In future work, we will evaluate this approach's security and performance implications in the context of an operating system.

# References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