Enabling Design Space Exploration of RISC-V Accelerator-rich Computing Systems on gem5

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Motivation
- The slowdown of CMOS scaling has led to the widespread use of heterogeneous SoCs
- Need for tools that enable fast design space exploration and modeling of such designs containing RISC-V cores
- We achieve this goal by porting gem5-SALAM [MICRO’20], a cutting-edge Domain Specific Accelerator (DSA) simulator, to RISC-V
- gem5-SALAM is based on the widely-used gem5 microarchitectural simulator and works by instrumenting the LLVM of C descriptions of DSAs

Simulation Framework Architecture

Porting gem5-SALAM to RISC-V
1. The interrupt system used by gem5-SALAM hardware components employed the Arm General Interrupt Controller (GIC) for posting interrupts to the host CPU
   - We translate the GIC functionality to the RISC-V Platform Level Interrupt Controller (PLIC) implemented in gem5
2. The bare-metal software infrastructure included Arm specific boot code and interrupt handler support
   - We use SiFive’s Freedom-E SDK since the HiFive platform that gem5 supports is based on the SiFive U54 RISC-V SoC. The SDK provides device drivers and system calls that allow for easy configuration of interrupts, UART communication, HW timers

Execution Time of Different Configurations

Area Overhead of Different Configurations

By doing this we minimize the manual effort required for deploying bare-metal applications and have full bare-metal C library support in the form of Newlib
3. The automatic gem5 configuration script generator used an Arm gem5 configuration script as a template
   - To port the generator to RISC-V, we swapped the Arm-specific script template to an already existing RISC-V full-system configuration script
   - We also made modifications to initialize the gem5-SALAM components, and added the accelerator memory mapped addresses to the address ranges of the RISC-V platform

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