RISC-V as an enabler of heterogeneous compute

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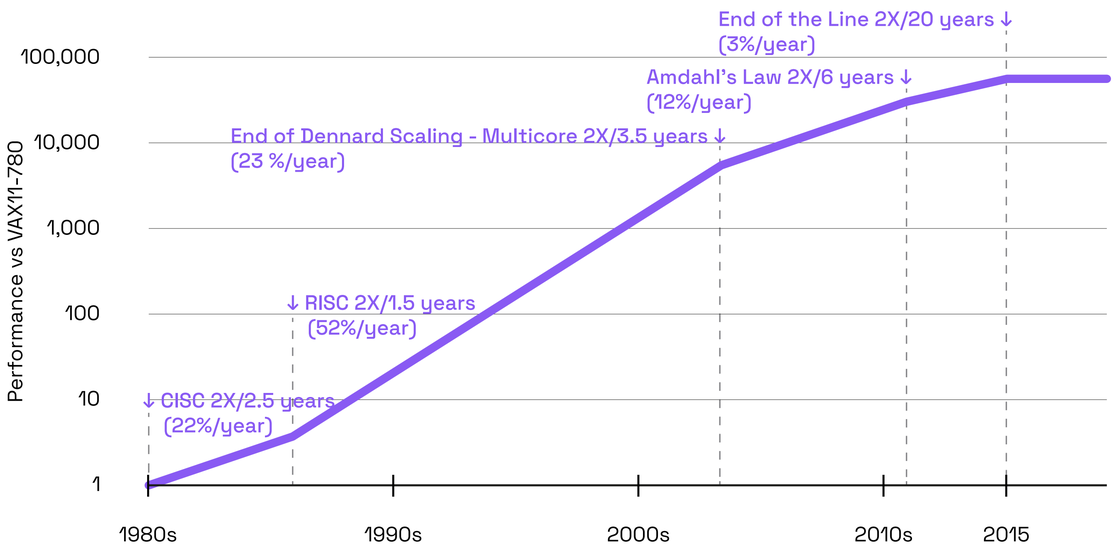
Codasip

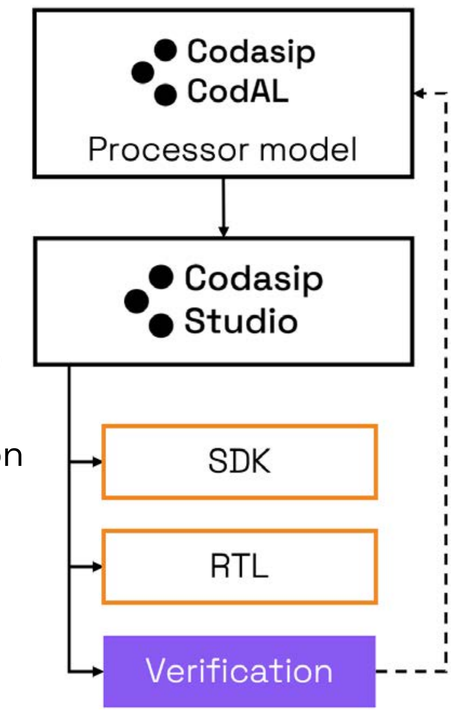
→ End of the road for traditional processor design

Scaling is failing and architectural innovation is the only way forward.



→ Unique processor design & customization tool

- Take existing RISC-V description in CodAL
- Profile software to identify hotspots
- Refine instruction set regenerate SDK and profile
- Tailor microarchitecture to achieve goals and generate RTL & TB
- User may use the instruction via the intrinsic or inline assembly



Verification → Design Space Exploration

Pre-verified RISC-V processors IPs are an essential enabler for a wide adoption of RISC-V in the heterogeneous compute.

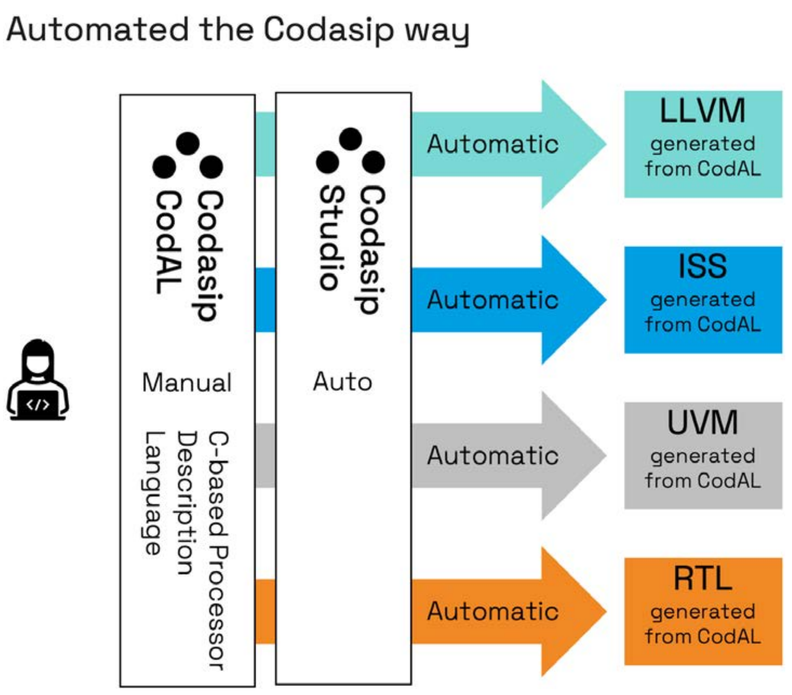
It solves a number of major problems, such as the need of a high-quality baseline that designers can build on, or the fact that the modular ISA removes the reinventing of the basic instructions that each processor must have.

→ RISC-V extensions offer flexibility

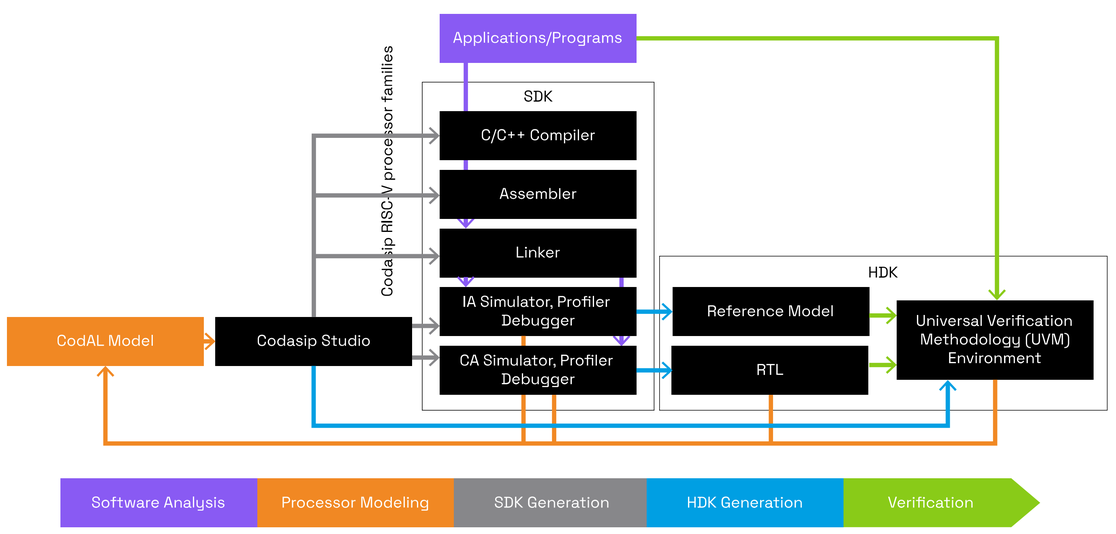
One of the unique features of RISC-V is the open instruction set specification with the rights to extend it.

This combination gives freedom to designers to control their destiny and it is a perfect fit for the needs of heterogeneous compute.

→ Automated the Codasip way



→ Architecture (instruction set) modelling



→ Conclusion

New techniques and methodologies are required to satisfy the growth of heterogeneous compute. The proposed solution automates the processor design and how the processor is customized for heterogeneous compute.

The customization is done on several levels allowing non-expert as well as expert designers to do it. The pre-verified RISC-V processors IP, that is designed for differentiation and innovation, is the key enabler and a baseline for further improvements.