

# Instrument Control & Data Processing

for high-reliable  
'New Space'  
instruments

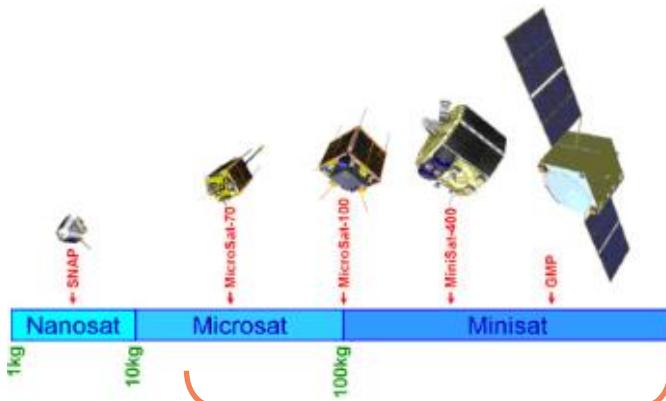
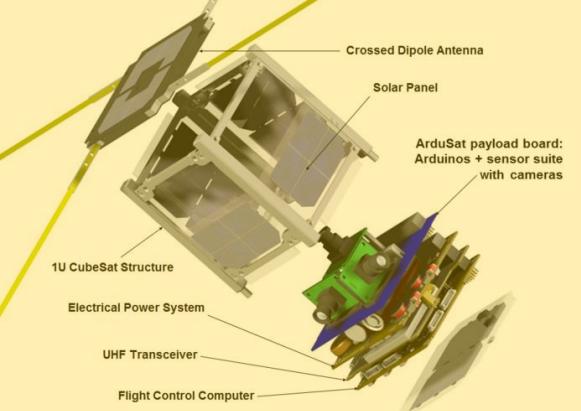
Dr. ir. Gerard Rauwerda

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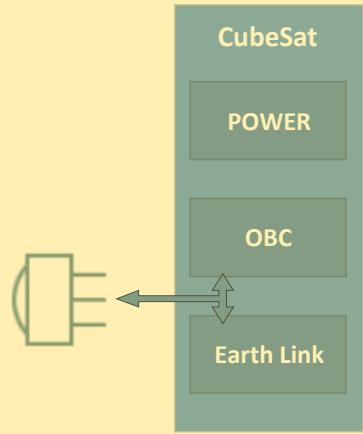


UNIVERSITY  
OF TWENTE.

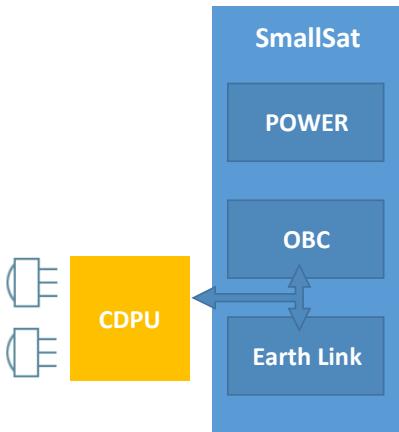




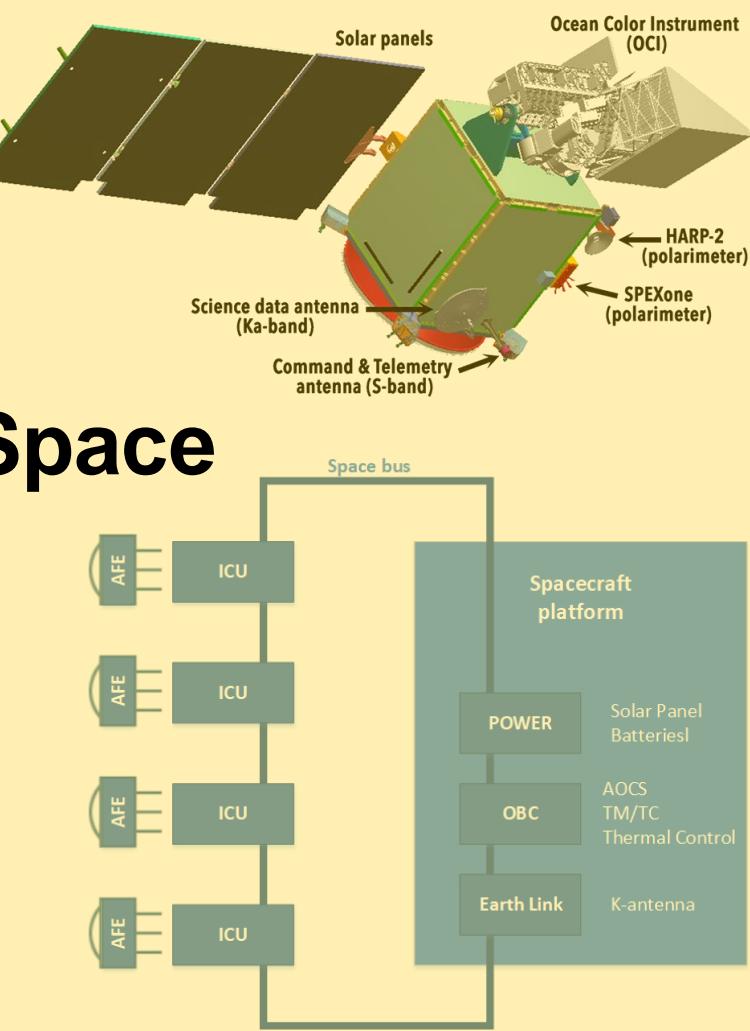
# New Space ↔ Traditional Space



**CubeSat**  
Single instrument  
Not Rad-Tolerant

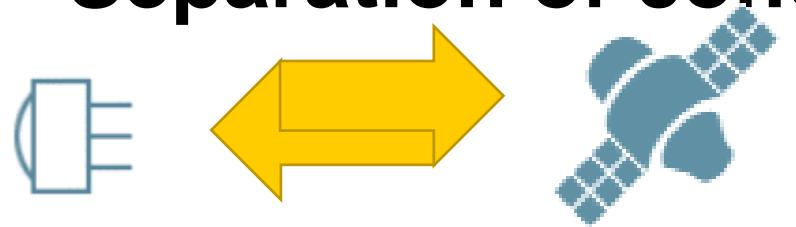


**SmallSat**  
Single or Multi instrument  
Instrument autonomy  
Rad-Tolerant

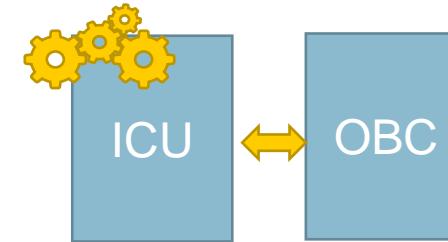


**Science satellite (conventional space)**  
Multi instrument  
Custom ICU developed  
Share Earth link with other instruments

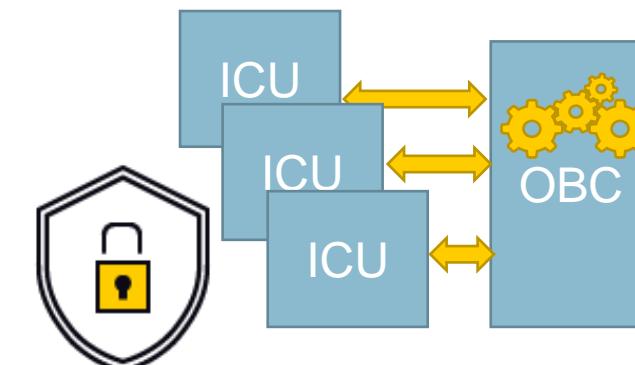
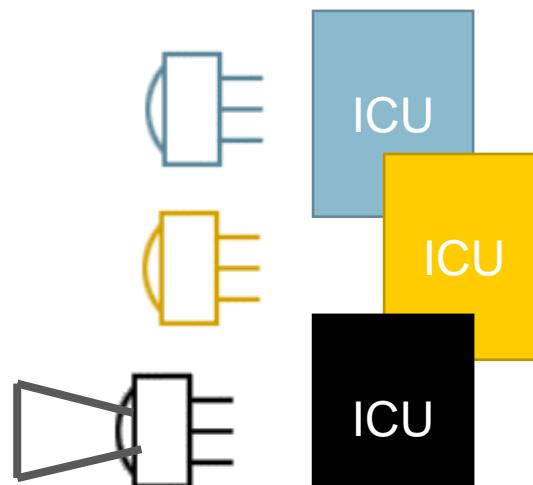
# Problem context: Separation of concerns and standardization in satellites



TTM – integration duration



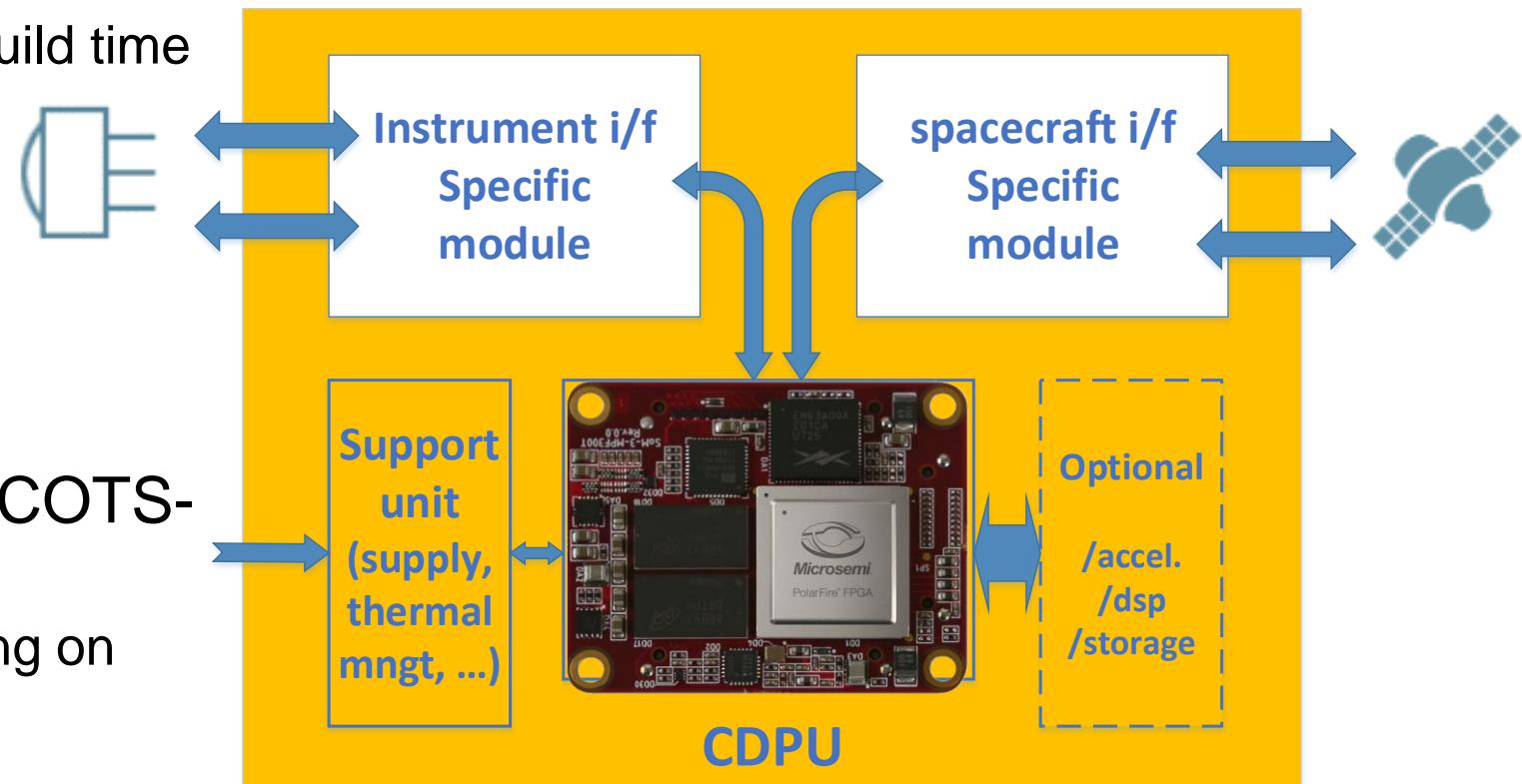
Data rate & Bandwidth



Separation of concerns

# Modular electronics to bridge sensor with satellite platform

- Enabling reuse of modules in new projects → NRE cost sharing
- Separation of concerns between satellite platform and instrument developers
  - Reducing overall satellite build time
  - Reducing instrument development and test time
- Rapid prototyping
- Design for rad.-hard (and COTS-equivalent) components
  - Reliability trade-off depending on mission needs



# CDPU: Control & Data Processing Unit for SmallSat instruments

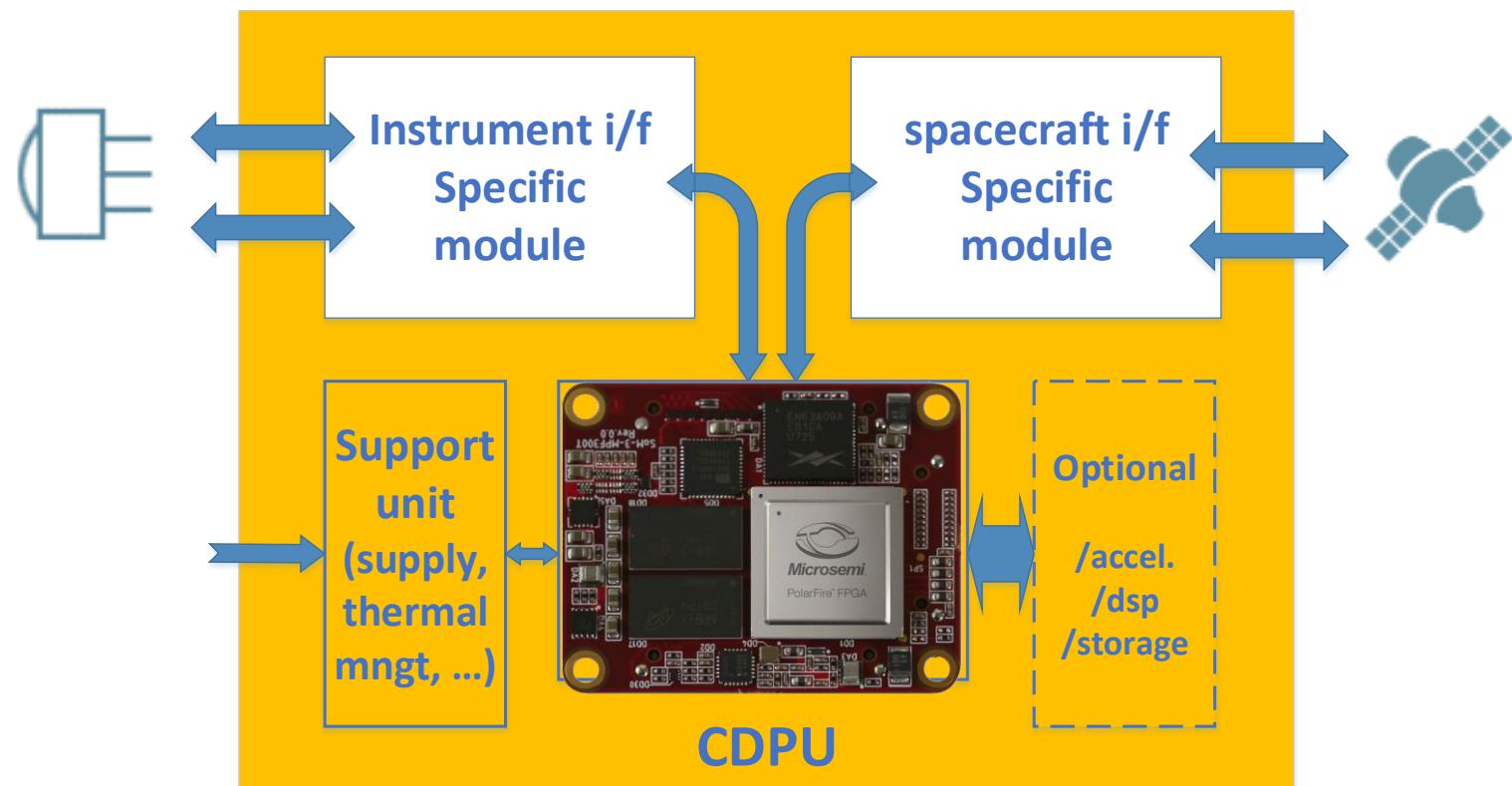
Netherlands  
Space  
Office



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**Technolution**



Flexible & reliable integration of sensor and platform



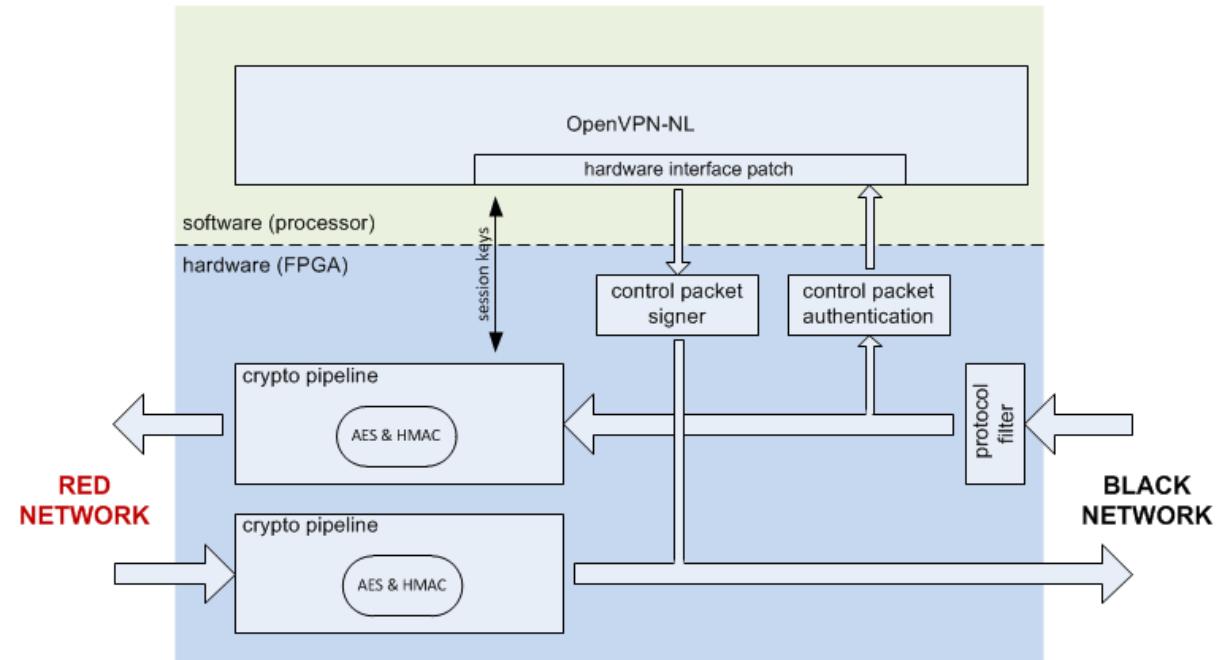
# RISC-V at Technolution

- We develop supplier-independent Programmable Logic designs
  - Implemented in    
- FreNox RISC-V IP
  - RISC-V processor family, 100% developed by Technolution
  - No dependencies on open-source implementations
  - Implemented in **NLD/NATO/EU** classified security



# Secure line encryption

- Hardware VPN solution (NLD/NATO/EU restricted)
  - Control flow in software /  RISC-V®
  - Data encryption in hardware logic



# Secure line encryption

- Hardware VPN solution (NLD/NATO/EU restricted)
    - Control flow in software /  RISC-V®
    - Data encryption in hardware logic
- ⇒ Full understanding of our custom implementation
- ⇒ Transparency for customer/evaluator
- ⇒ Lifecycle management (transparency & portability)





## Embedded processor

- hardware
  - RV32I(MA)
  - 32bits, mul/div
  - 5 stages - Harvard arch
  - cache or internal RAM
  - IO space
- software
  - Bare metal (C, embedded Rust)
  - FreeRTOS
  - ThreadX



## Application processor

- hardware
  - RV32IMA (S-mode)
  - 32bits, mul/div, atomic, supervisor
  - 5 stages - Harvard arch
  - iMMU, dMMU (1 - 128 entries)
  - 8 way associative cache (4 - 32k)
  - cache coherency (DMA)
  - IO space
- software
  - Linux
  - Buildroot

# CDPU: Control & Data Processing Unit

## for SmallSat instruments

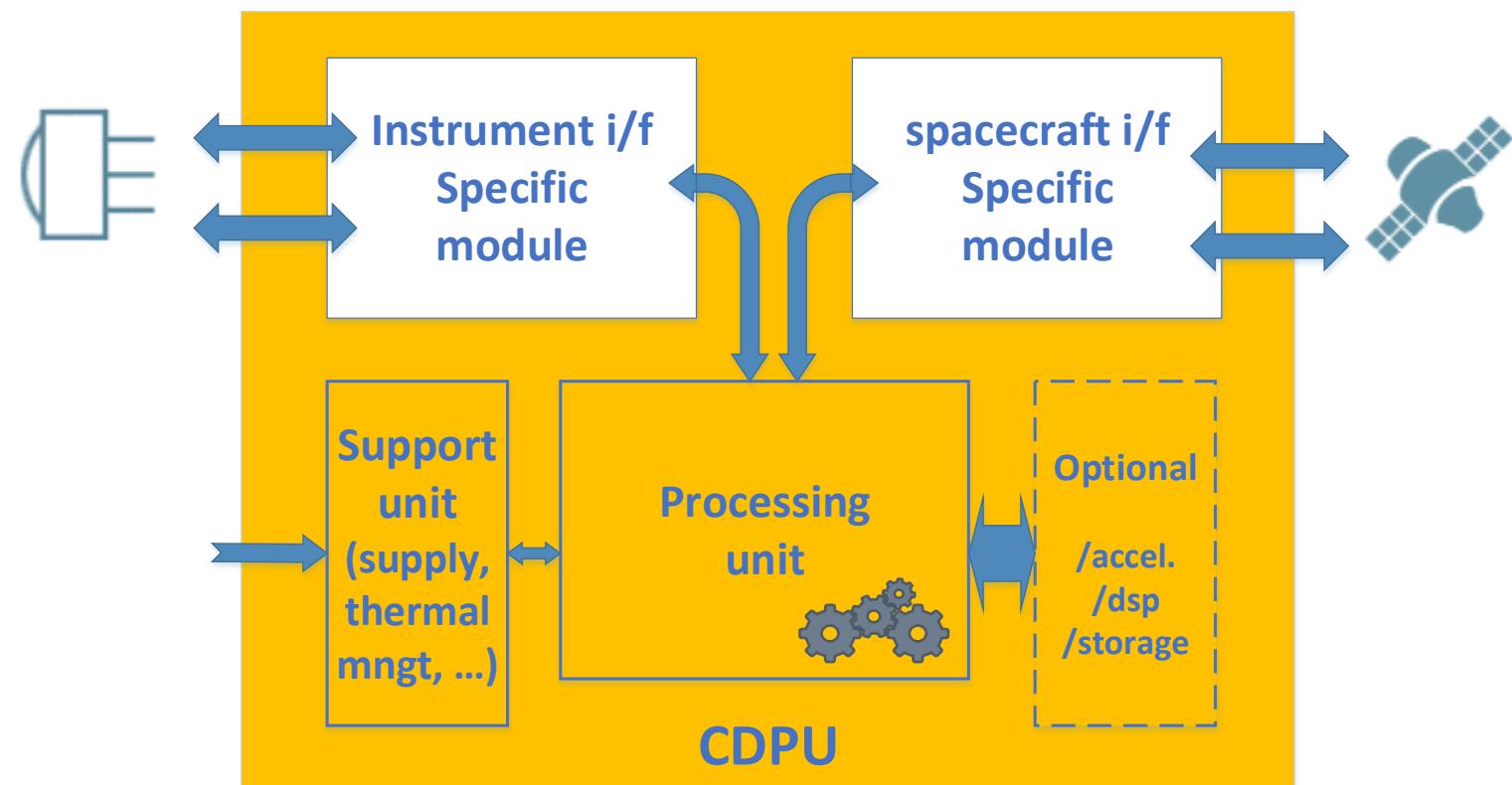
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**Space**  
Office



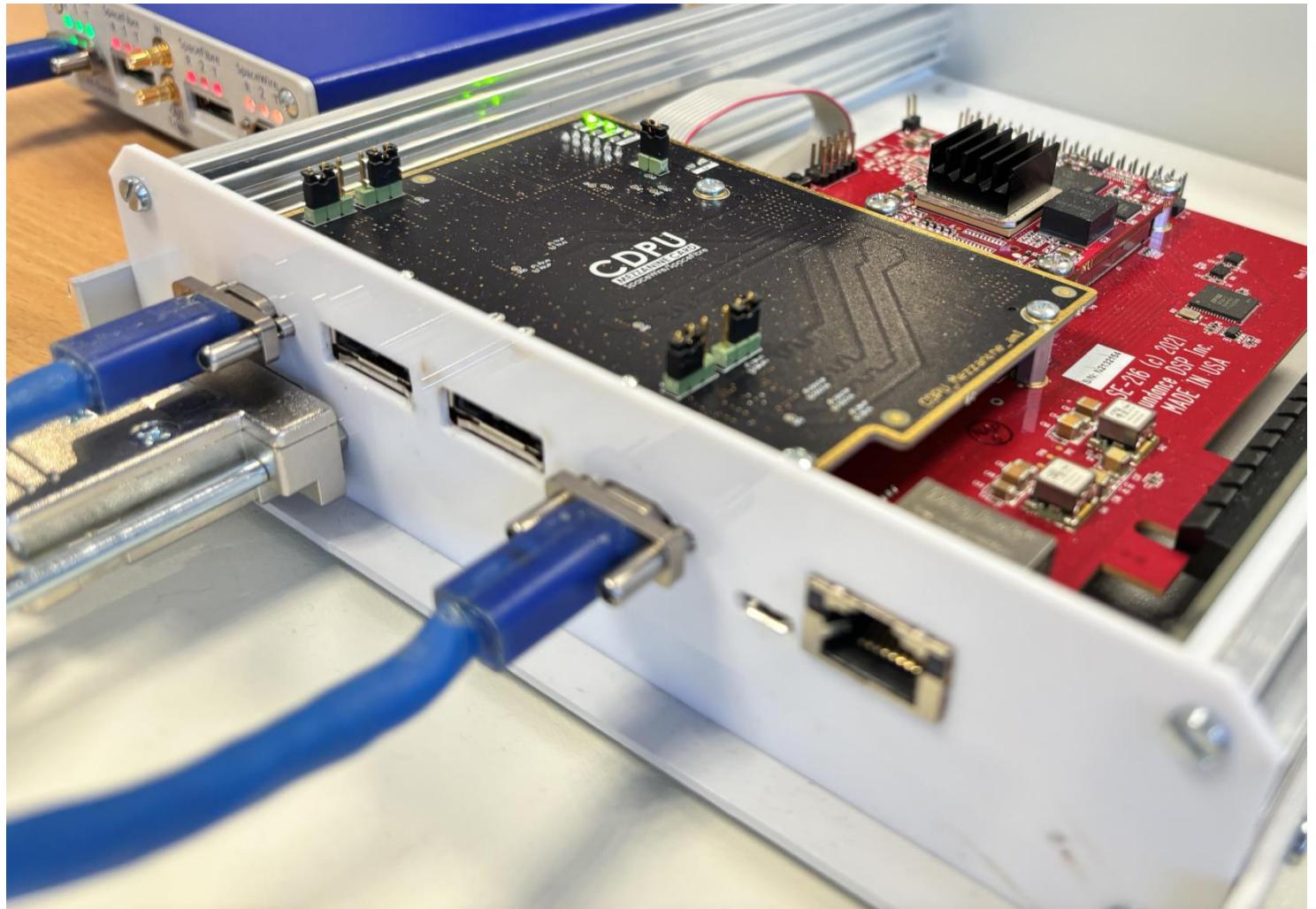
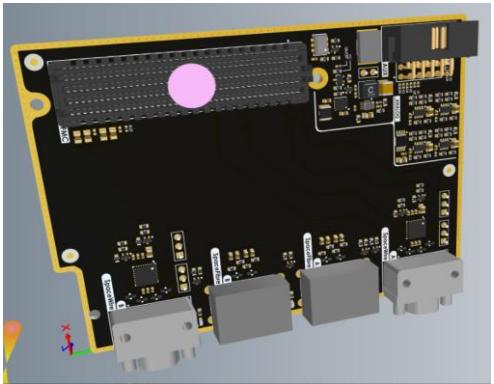
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Flexible & reliable integration of sensor and platform

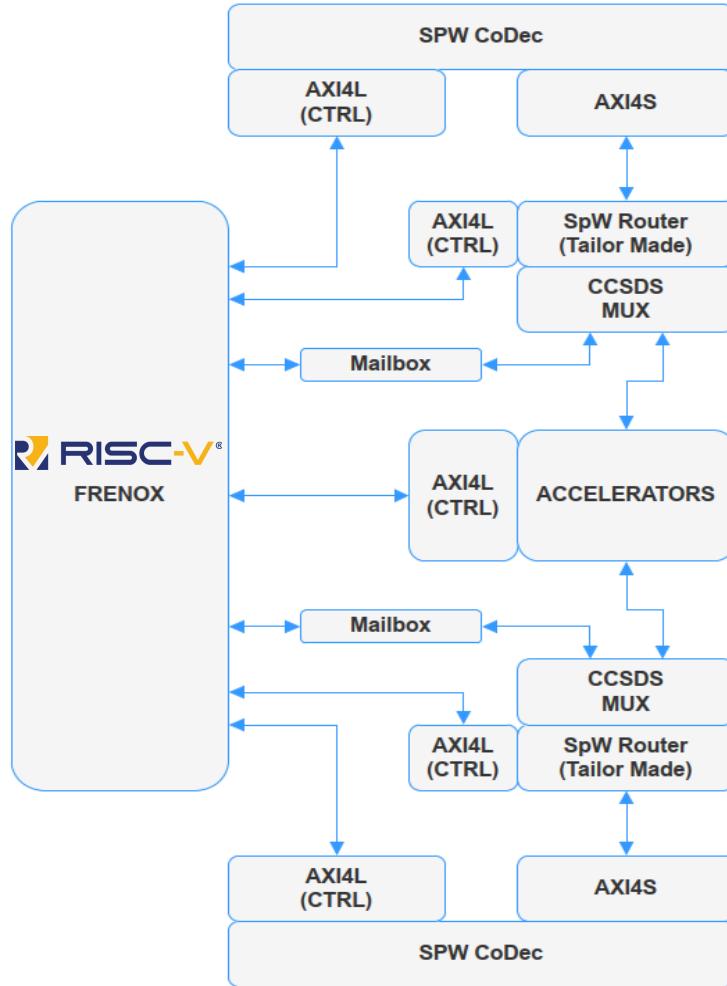


# CDPU Evaluation Kit

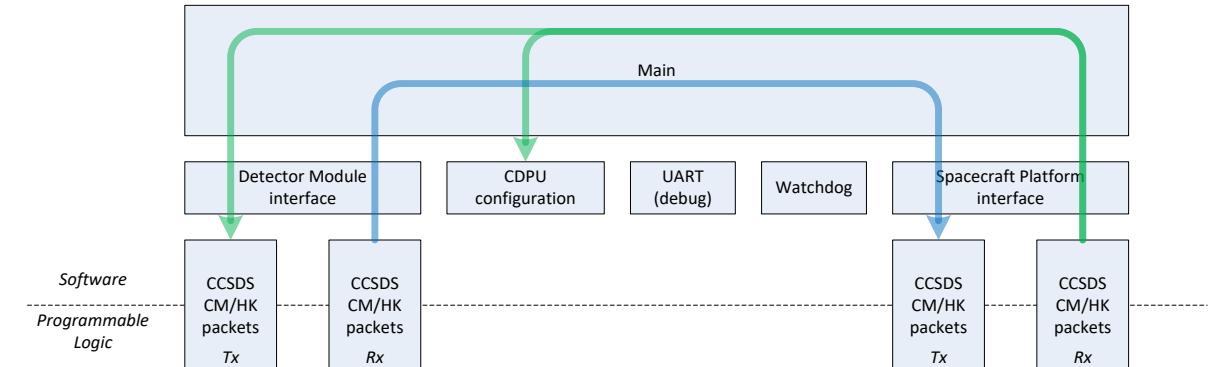


 RISC-V®

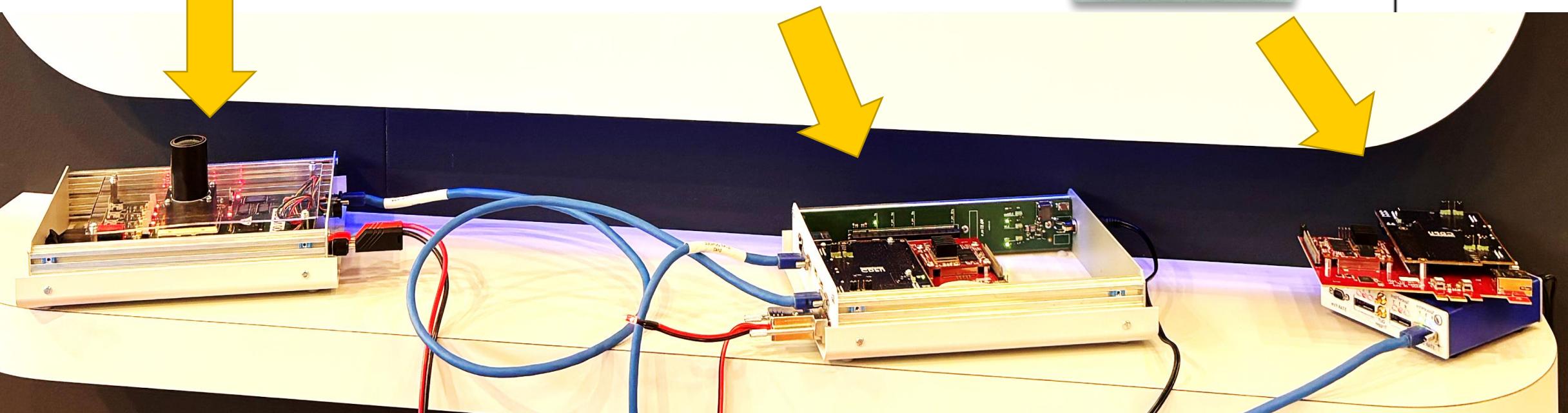
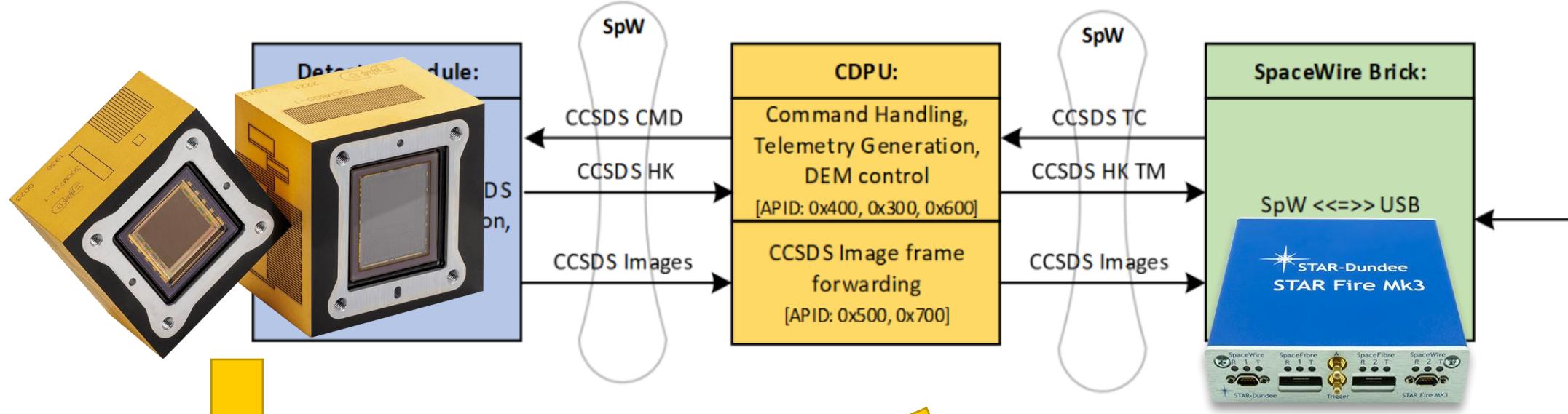
# CDPU FPGA Functional Design

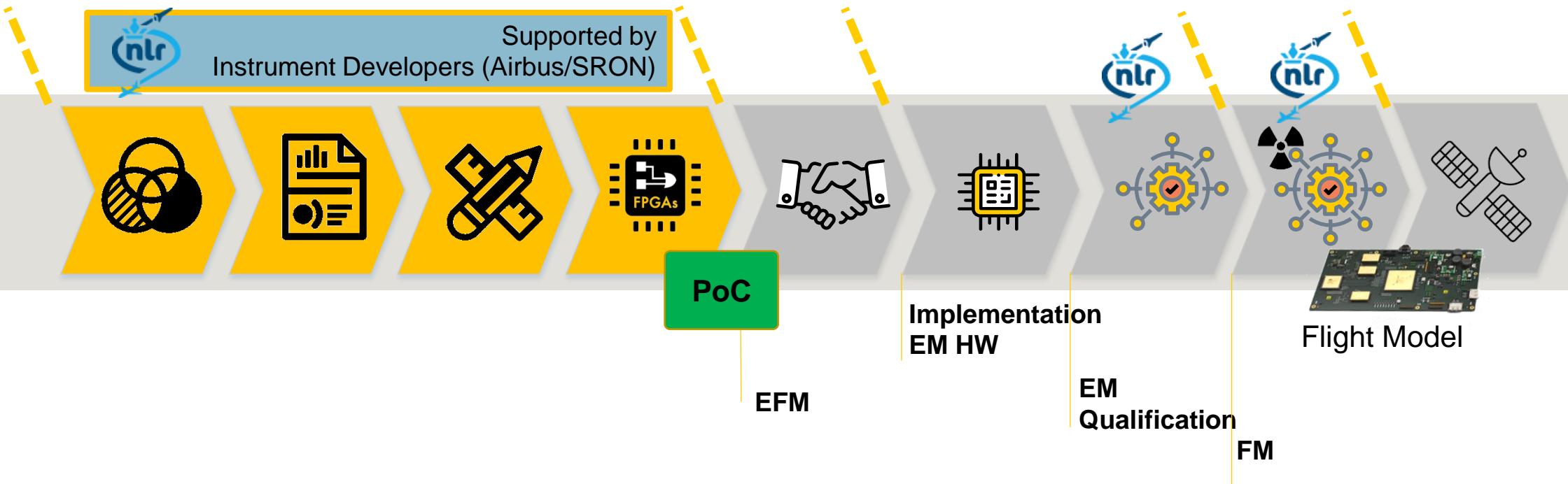
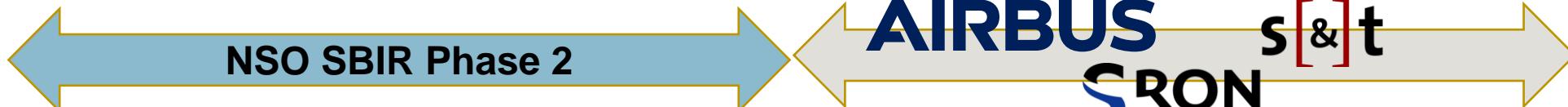


- Programmable logic design
  - FreNox RISC-V
  - SpW interface IP
  - SpFi interface IP
  - Interconnect infrastructure; accelerator extensions
- Embedded software design
  - TC/TM handling



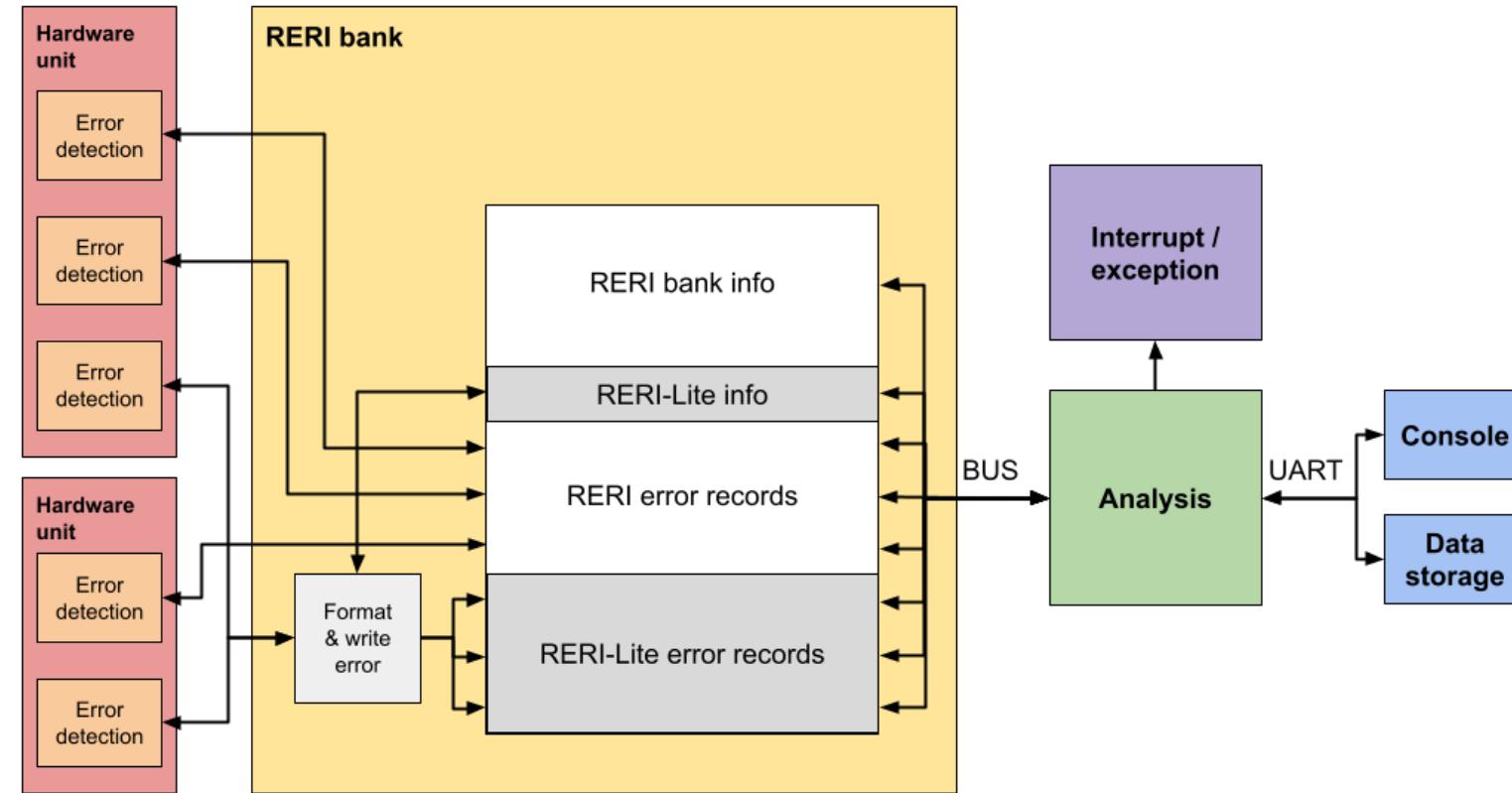
# CDPU Demo – Instrument Integration





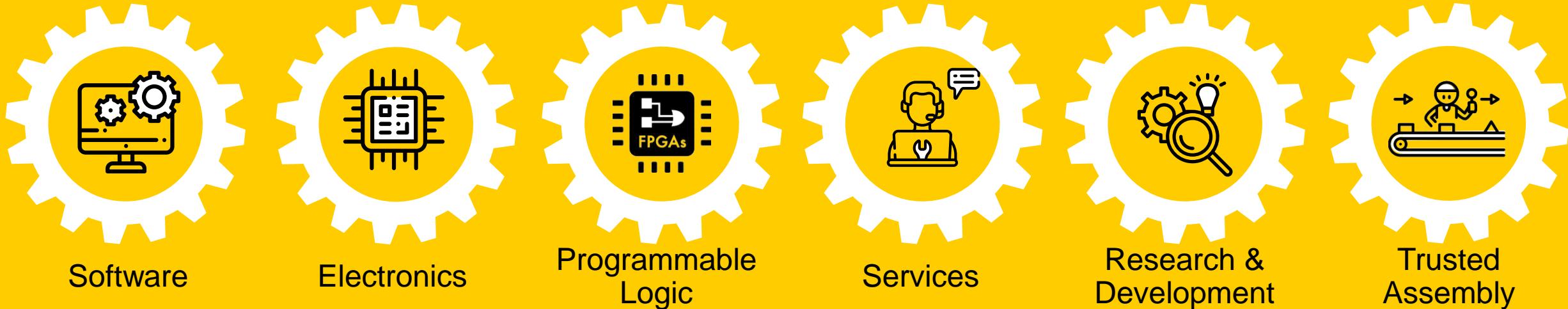
- FreNox-E SoC demonstrated in NG-Medium RH-FPGA
- FreNox-E SoC demonstrated in PolarFire FPGA

# Innovation & collaboration



- Joint research with University of Twente & European Space Agency on (reduced) RERI, checkers and radiation testing

# Conclusion: advanced electronics and embedded systems

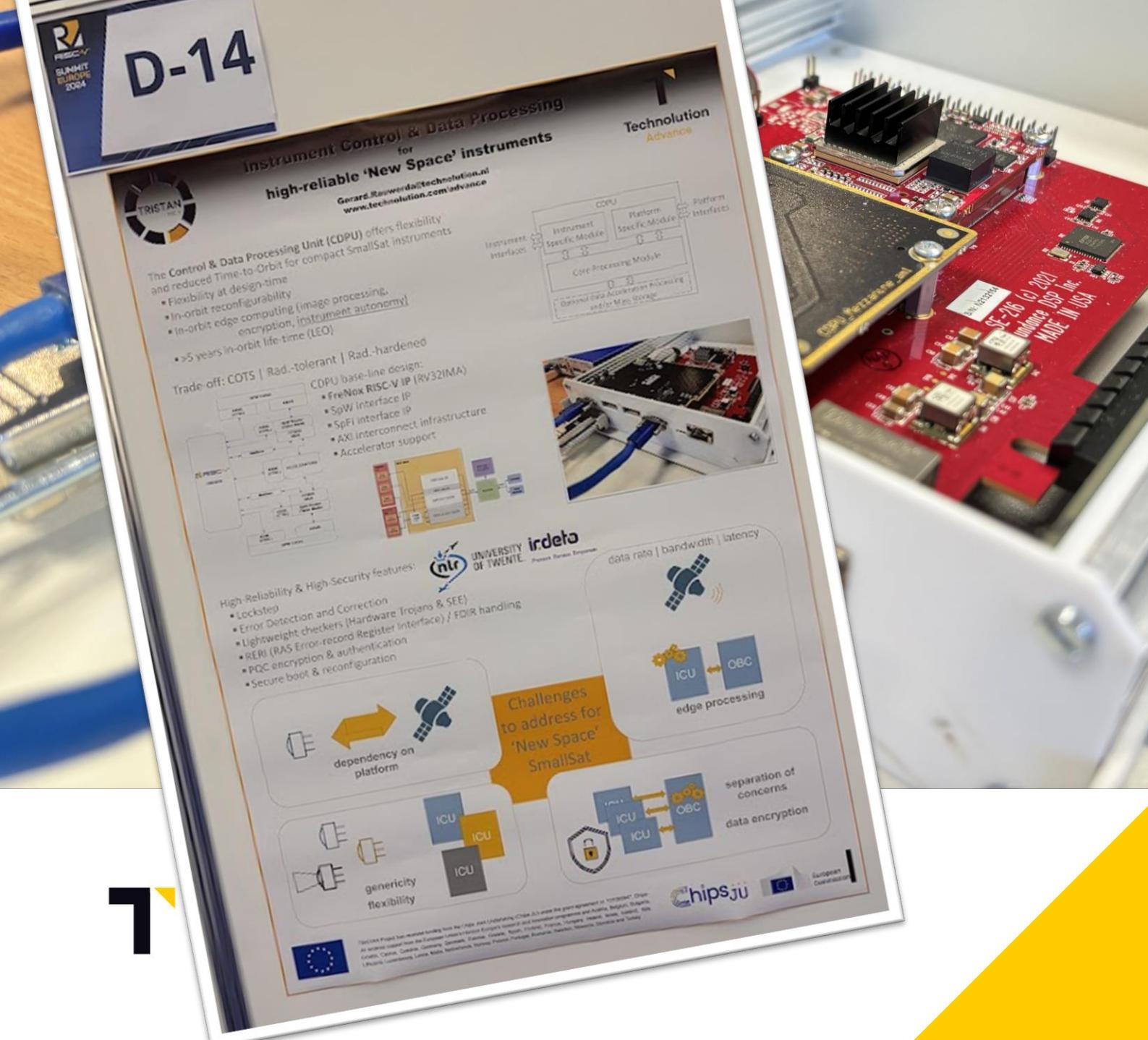


**Modular electronics enable re-use**

Modularity gives **reduced instrument development & test time**

**Benefit from standardization:** transparency, portability & flexibility

We build high-security & high-reliability systems using  **RISC-V**®(since 2014)



# Thanks for your attention!

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