Welcome to RISC-V Summit Europe 2024

Christian Fabre
CEA – RISC-V Summit Europe SC Co-Chair

About RISC-V Summit Europe

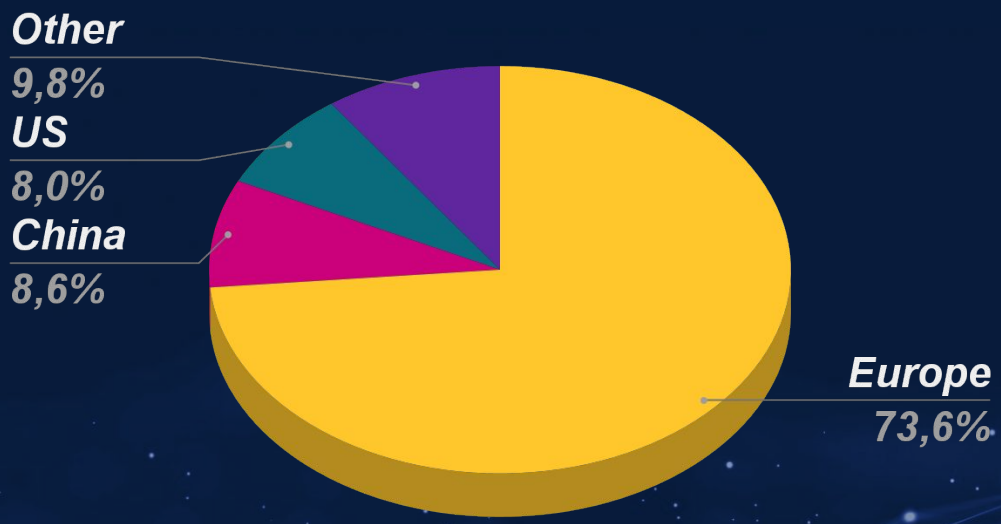
Joint effort of RISC-V International and three former events:

- RISC-V Activities Workshop (Germany)
- Red RISC-V (Spain)
- RISC-V Days/Week (France)

1st RISC-V Summit Europe in Barcelona on June 5-9, 2023.

2nd RISC-V Summit Europe in Munich on June 24-28, 2024.

Over 700 Attendees!



Armenia
Australia
Austria
Belgium
Brazil
Canada
China
Congo, The Democratic Republic of the
Croatia
Czech Republic
Finland
France
Germany
Greece
India
Ireland
Israel
Italy
Jordan
Korea, Republic of
Luxembourg
Netherlands
Norway
Pakistan
Poland
Portugal
Saudi Arabia
Serbia
Slovenia
Spain
Sweden
Switzerland
Taiwan, Province of China
Türkiye
United Arab Emirates
United Kingdom
United States
Viet Nam

Thanks to our Committees

Steering & Local Committee

Teresa Cervero (BSC)
Romain Dolbeau (SiPearl)
Wolfgang Ecker (Infineon)
Roger Espasa (Semidynamics)
Christian Fabre (CEA), General Chair
Frank K. Gürkaynak (ETH Zürich)
Andy Moore (RISC-V International)
Daniel Mueller-Gritschneder (TU Munich)
Grace Mutsengi (KIT)
Borja Pérez Pavon (Univ. de Cantabria)
Jérôme Quévremont (Thales R&T)
Anna Riverola (SiPearl)
Calista Redmond (RISC-V International)
Tiffany Sparks (RISC-V International)
Anja Schröter (KIT)
Olivier Sentieys (INRIA)
Philipp Tomsich (VRULL)
Stefan Wallentowitz (Hochschule München)
Anja Zeun (KIT)

Program Committee (39 Members)

Jan Andersson (Frontgrade Gaisler)
Jeremy Bennett (Embecosm)
Holger Blasum (Sysgo)
Alex Bradbury (Igalia)
Ramon Canal (UPC)
Marc Canel (Ventana)
Gregory Chadwick (LowRISC)
Samuel Chiang (Andes)
Fabio De Ambroggi (STMicroelectronics)
Denis Dutoit (CEA)
Angelo Garofalo (Univ. Bologna)
Michael Gielda (Antmicro)
Daniel Große (Uni Linz)
Timo Hämäläinen (Tampere Uni)
Frederic Heitzmann (Tiempo)
Eyck Jentzsch (MINRES)
Nick Kossifidis (FORTH)
Larry Lapides (Synopsys)
Nathan Ma (Nuclei)
Fabrizio Magugliani (E4CE)
Andreas Mauderer (Bosch)
Andy Moore (RISC-V International)
Daniel Mueller-Gritschneder (TU Wien), co-chair
Rihards Novickis (EDI)
Katzalin Olcoz Herrero (UCM)
Arthur Perais (TIMA, CNRS)
Borja Pérez Pavon (Univ. de Cantabria), co-chair
Sandro Pinto (University of Minho)
Shawn Prestridge (IAR)
Jérôme Quévremont (Thales)
Victoria Rege (Imagination)
Thomas Roecker (Infineon)
Davide Rossi (University of Bologna)
Olivier Savry (CEA)
Olivier Sentieys (INRIA), chair
Davide Schiavone (OpenHW Group)
Georg Sigl (TU Munich)
Sharad Sinha (IIT Goa)
Gabriel L. Somlo (CMU)
Tiffany Sparks (RISC-V International)
Philipp Tomsich (VRULL)
Stefan Wallentowitz (HM)
Jonathan Woodruff (Uni Cambridge)
An Xu (BOSC)
Itai Yarom (MIPS)
Florian Zaruba (Axelera)

Program Overview of the RISC-V Summit Europe 2024

Olivier Sentieys
INRIA/University of Rennes – RISC-V Summit Europe PC Chair

Daniel Mueller-Gritschneder *(TU Wien), PC Co-Chair*
Borja Pérez Pavon *(Univ. de Cantabria), PC Co-Chair*

Thanks to Our Presenters

27 Technical Presentations

138 Poster Presentations

128 for the R&D track
57 for the Industry track

RISC-V®

Program Highlights

2 **Keynotes**

Krste Asanovic, RISC-V
Thomas Böhm, Infineon

27 **Technical Talks**

Technology and market advancements of last year

6 **Sponsor Keynotes**

Learn about exciting commercial advantages

2 **Panels**

“RISC-V and AI” and “How can Europe Engage in RISC-V?”

8 **Invited Talks**

Invited technology leaders

Collaboration Breakfast

Discuss community collaboration with fellow

RISC-V®

Demo Theatre

Technical in-depth presentation

10-minute presentations during breaks

Limited seating available, be on time!

Thursday: Hackathon results and University demos

Sponsored by Quintauris

Posters

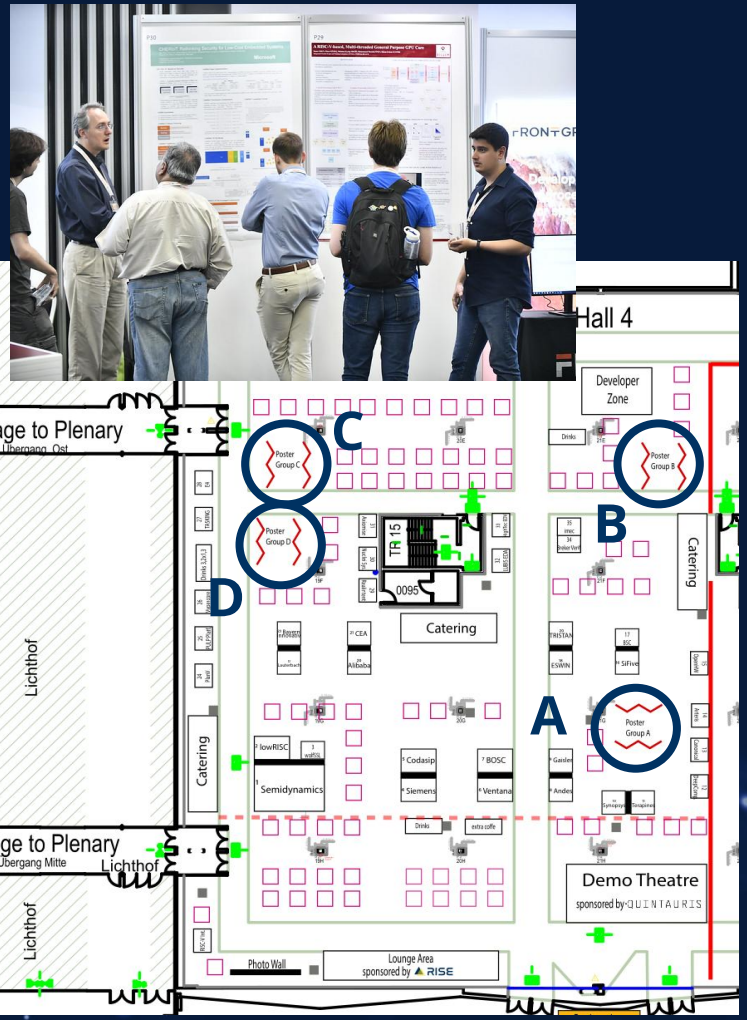
Meet the community at their posters

Posters rotate daily, so check back!

Find posters on website with their location

4 islands in the expo hall, during breaks

Presenters: Be sure to be at your poster to maximize engagement



Enjoy RISC-V Summit Europe 2024!