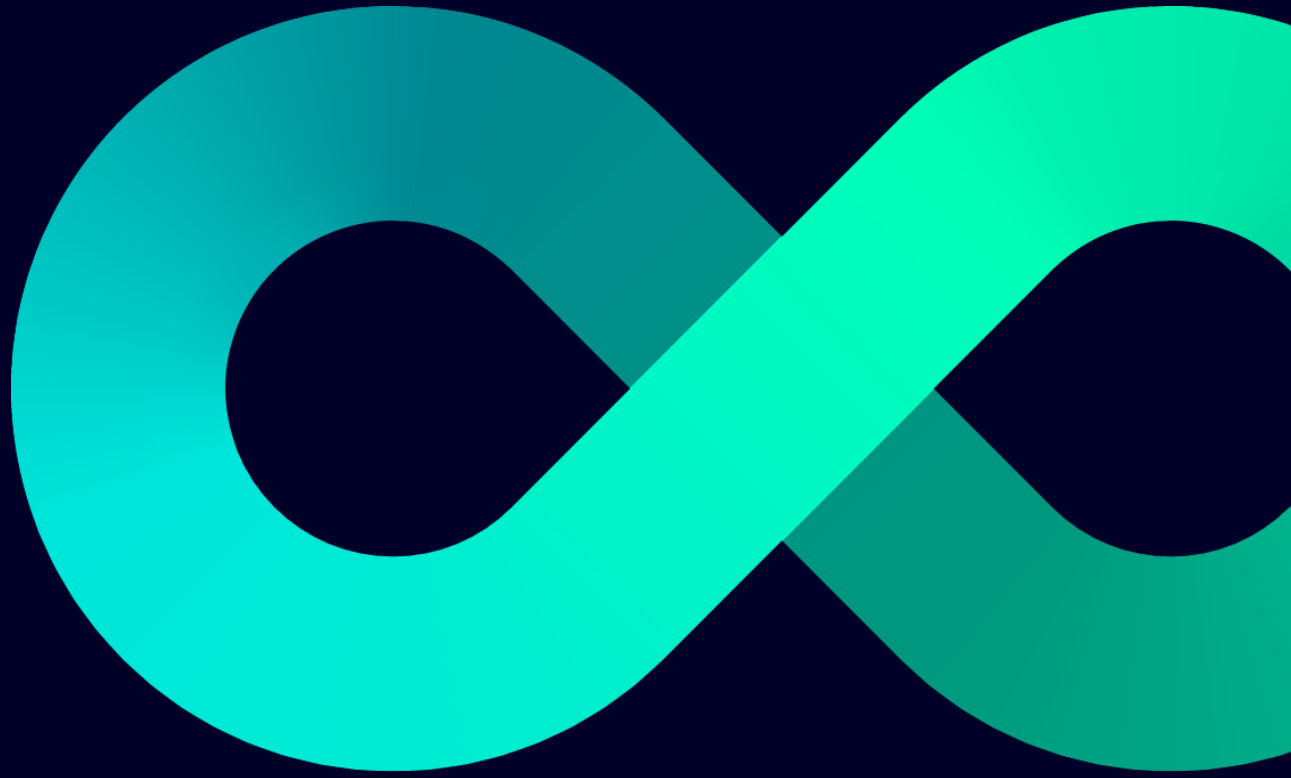
Taking the risk out of RISC-V

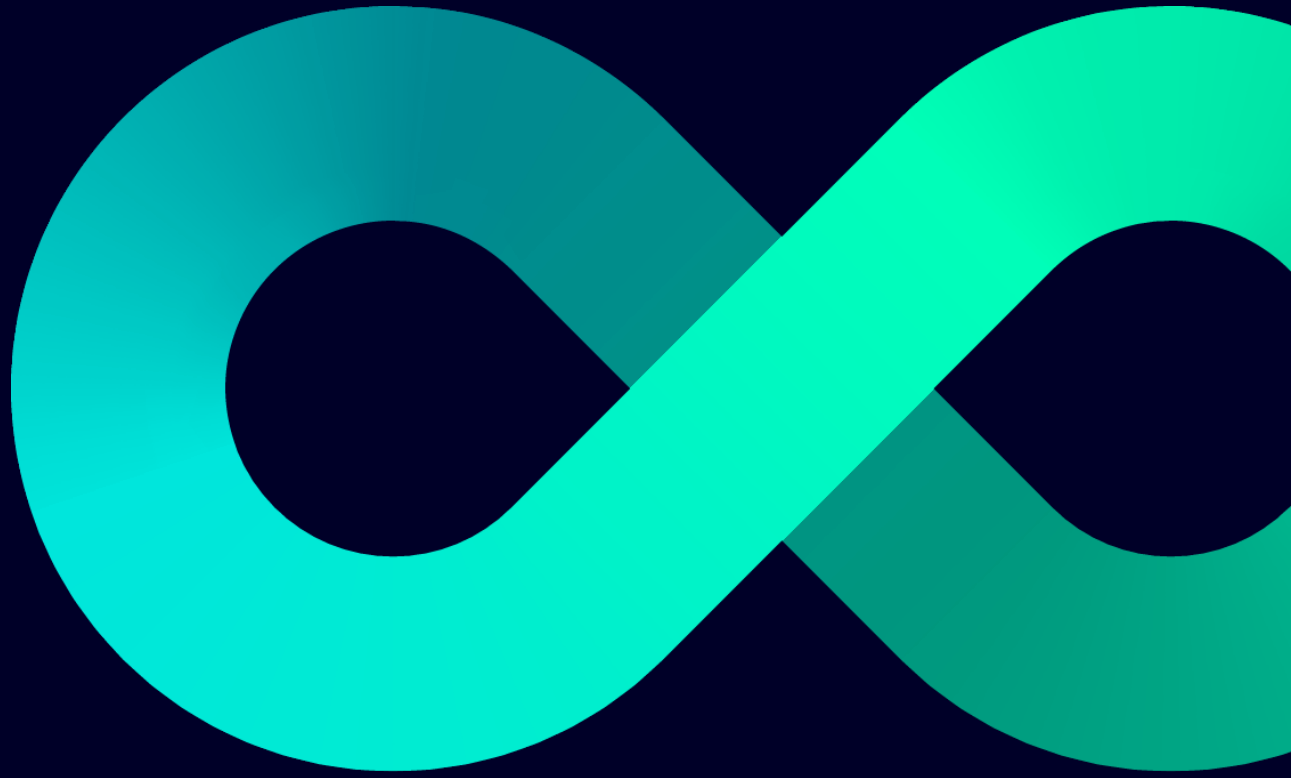
Take advantage of RISC-V without adding risk to your next-generation SoC and system design



SIEMENS

Taking the risk out of RISC-V

Take advantage of RISC-V without adding risk to your next-generation SoC and system design



SIEMENS

RISC-V creates opportunities and challenges

Pros	Cons
Open architecture specification independent of implementation	Does not define an implementation so specification can be open to interpretation
Wide selection of IP implementations optimized for use-cases	Need a way to validate suitability of the IP for an application
Ability to create bespoke and optimized solution based on application	Need a way to effectively verify processor changes
Common software ecosystem	Need to port and validate existing software

SIEMENS

With great flexibility, comes great responsibility

Non infringing paraphrase, of a totally non-licensed quote…

SIEMENS

The challenge isn’t in building a new processor

Hard

Designing a new processor is relatively achievable for even a small team

It’s the reason there were previously so many processor IPs

SIEMENS

The challenge isn’t in building a new processor

Hard

Designing a new processor is relatively achievable for even a small team

It’s the reason there were previously so many processor IPs

Harder

Verifying it works in a specific configuration and for a fixed task

Verification doesn’t scale linearly with complexity

Hardest

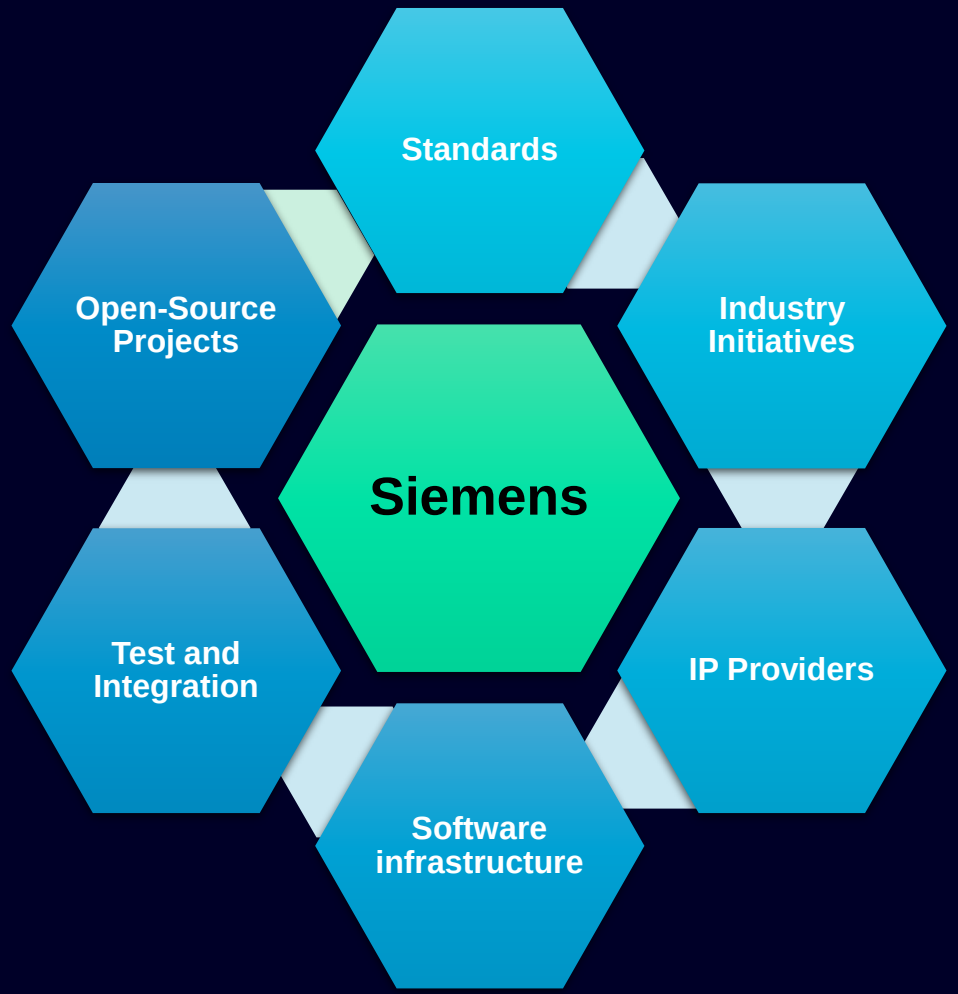
Scaling to work under a variety of conditions and building a robust software infrastructures

Requires specialized tools, teams and lots of resources

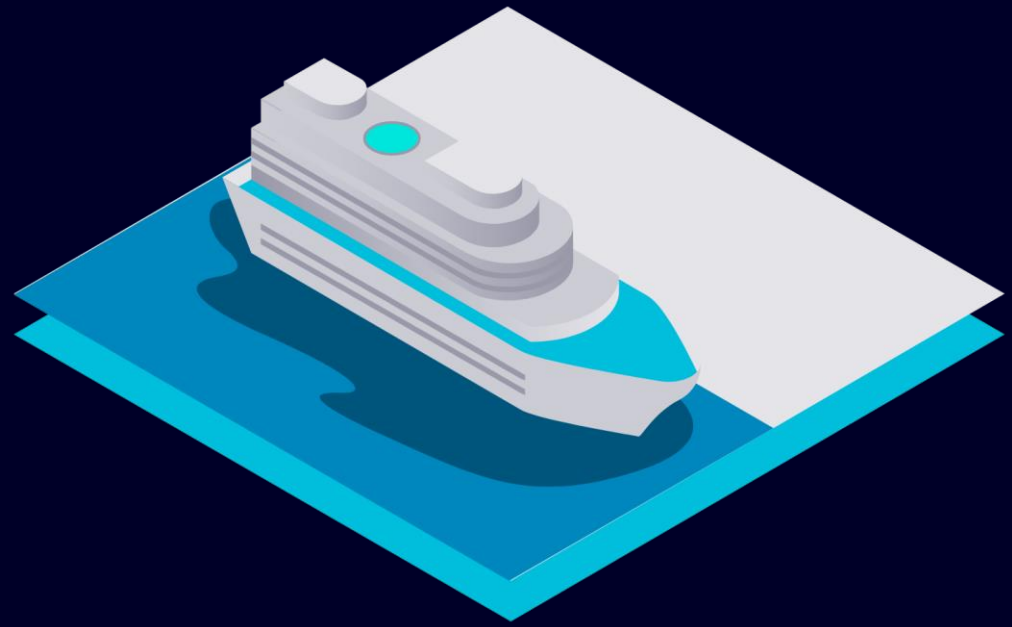
End-to-end verification and validation is key to scalable success in any SoC design even when using “proven” IP

SIEMENS

Siemens supports the RISC-V ecosystem



A rising tide lifts all boats

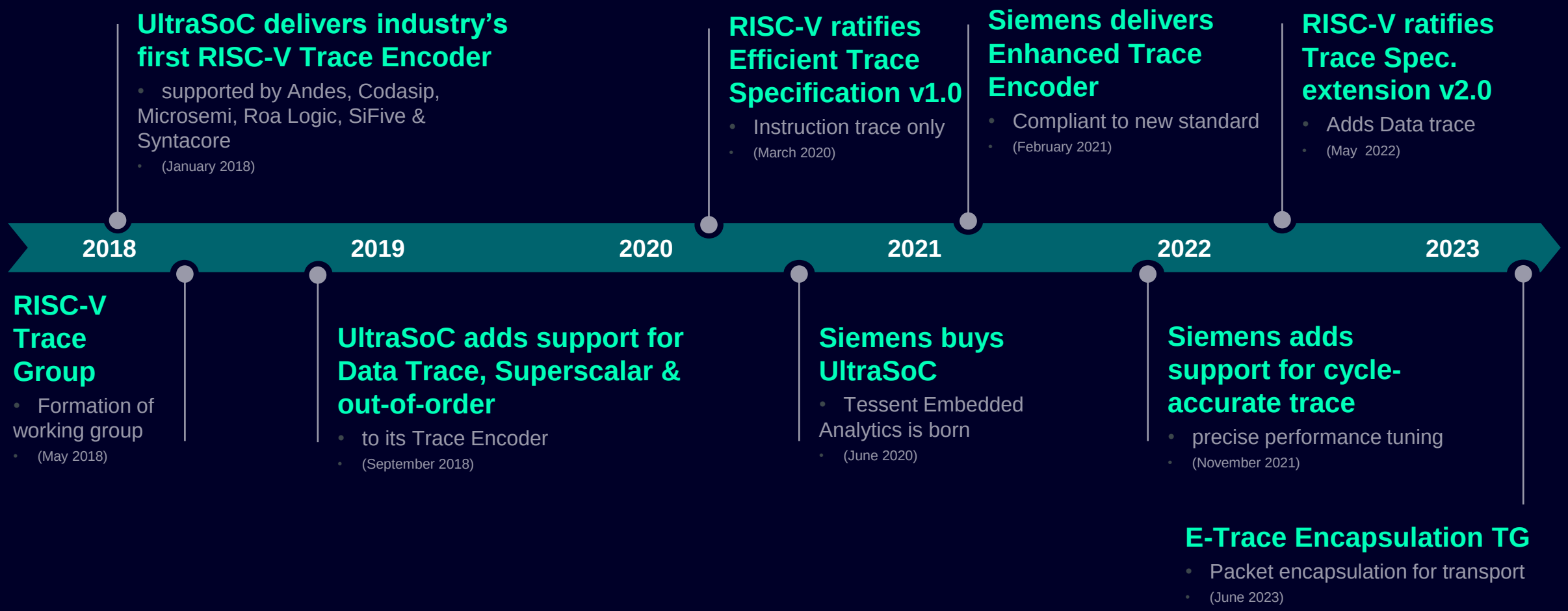


Siemens is not an IP provider;
we believe enabling the RISC-V ecosystem grows the market for all

SIEMENS

Long term support for RISC-V core standards

an E-Trace Timeline



Enabling high-quality processors

Technology

Processor Verification

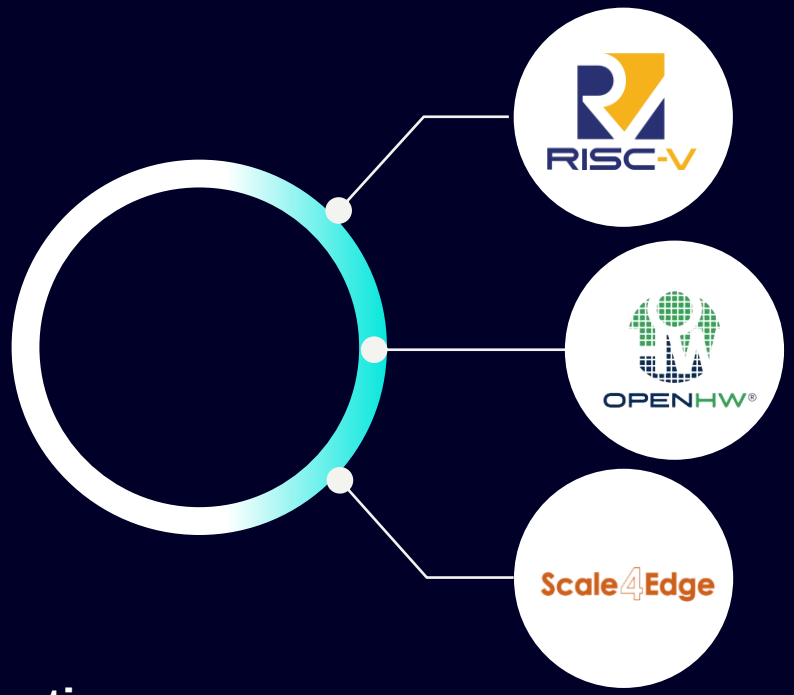
- Core verification
- Integration verification

Industry involvement

RISC-V International

OpenHW Group

Scale4Edge project



User community

Commercial solution adoption

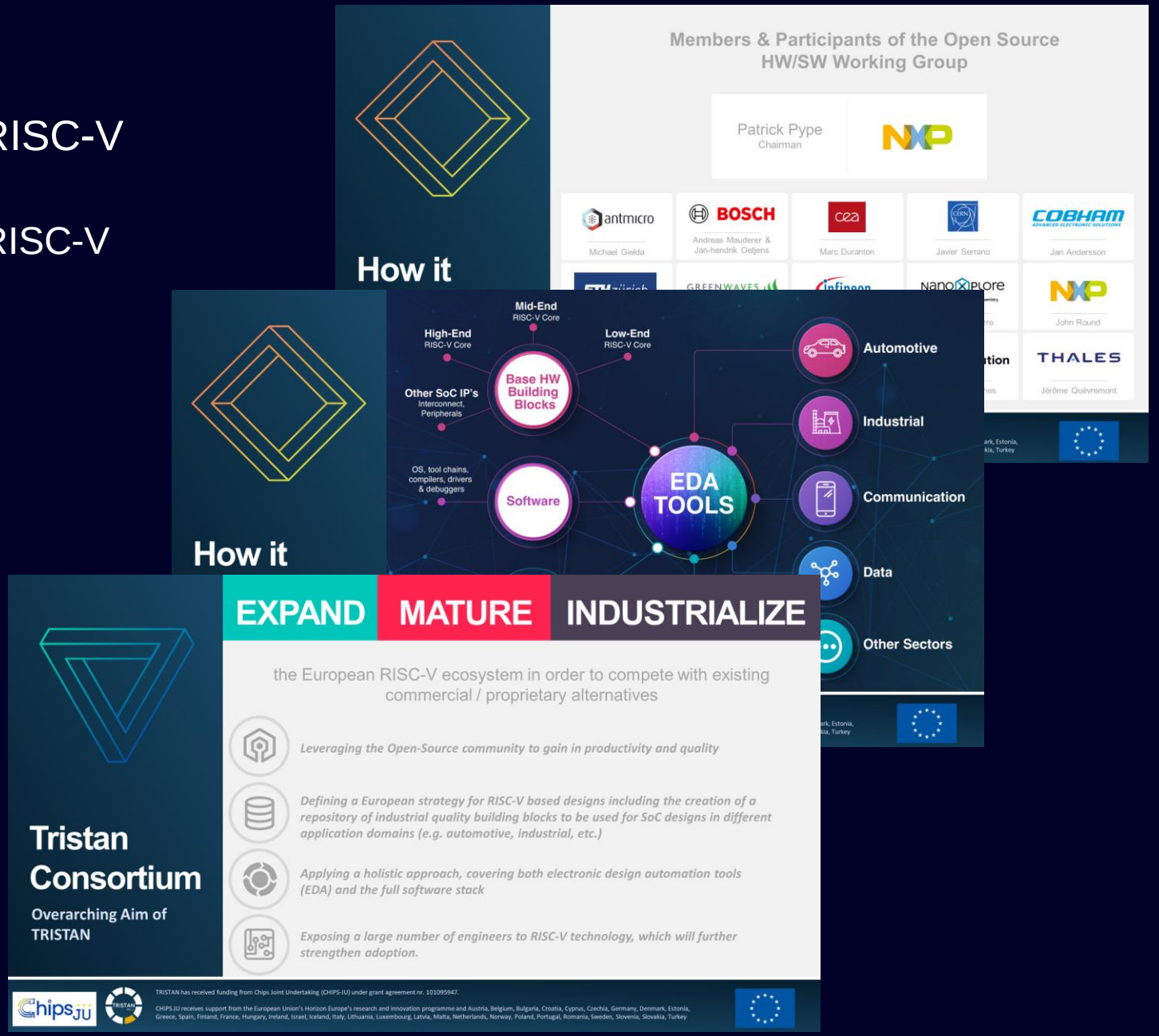
SIEMENS

TRISTAN Consortium overview

Siemens partnering with industry to drive RISC-V

Expand, Mature, Industrialize the European RISC-V ecosystem to compete with commercial and/or proprietary alternatives

- Broad industry partnership
- Predictable solutions for RISC-V Adoption
- Broad applicability



SIEMENS

tristan-project.eu

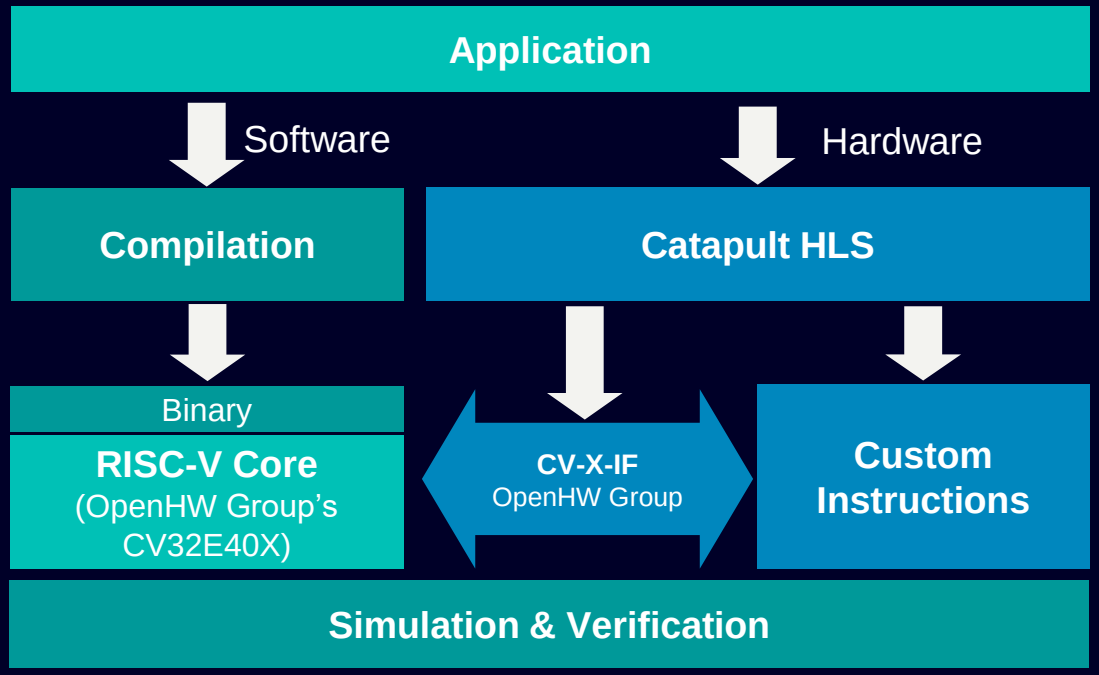
TRISTAN

SIEMENS Contributions

-> Please visit the Siemens colleagues at the Tristan booth

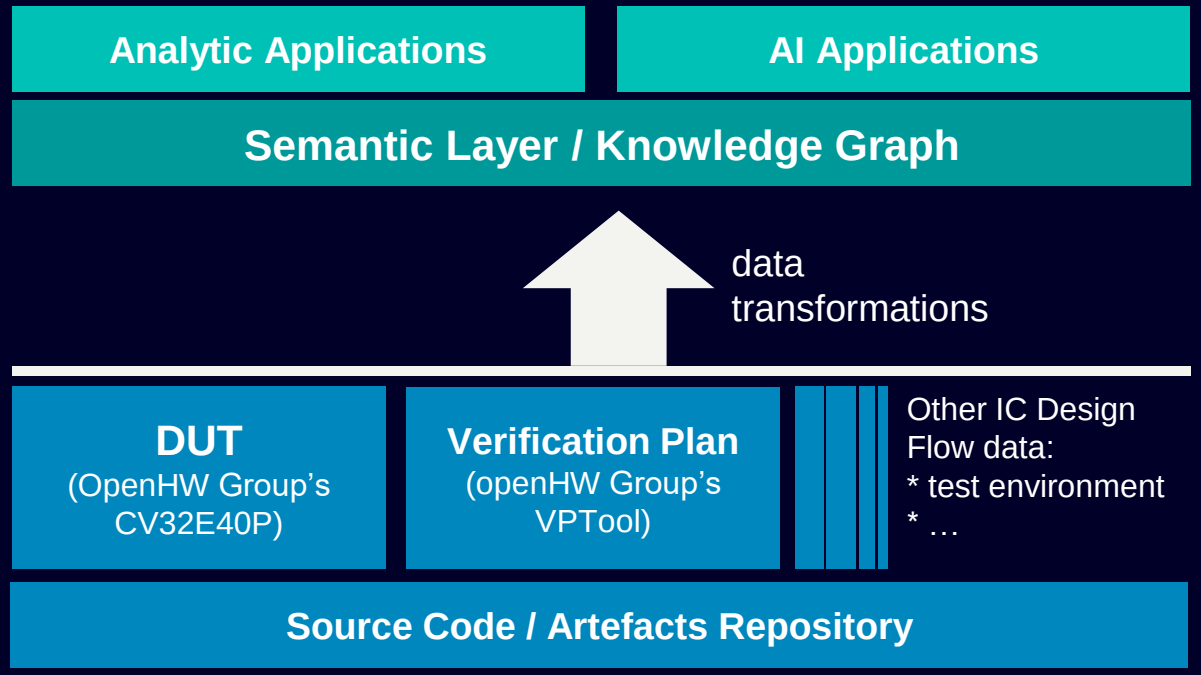
A flexible High-Level Synthesis Flow for RISC-V Custom Instructions

Speed-up applications by customizing instructions for existing processors supporting CV-X-IF.



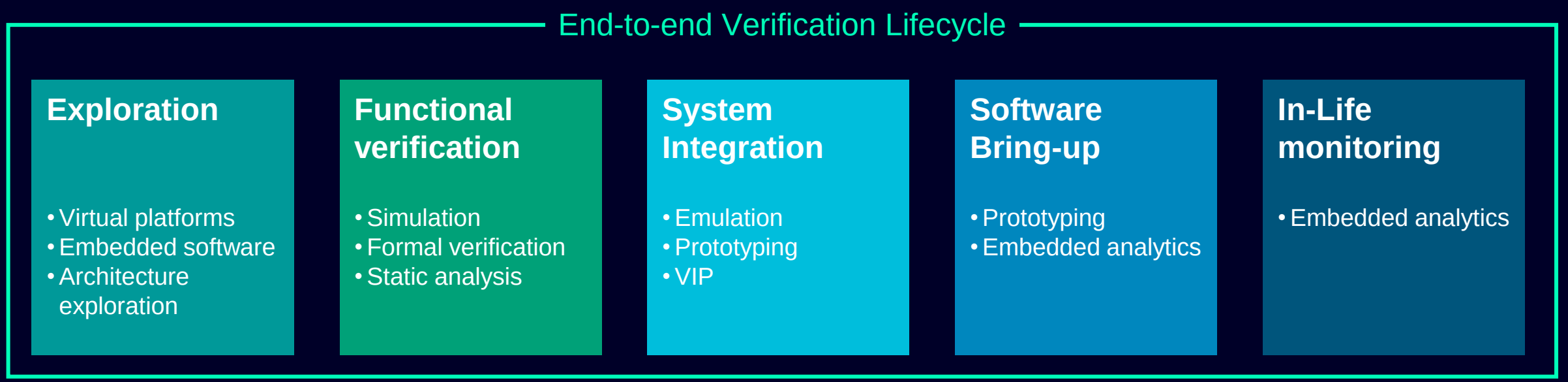
AI-Enhanced Verification Framework for RISC-V

Integrating all diverse data and hosting analytical and AI-enabled verification apps.



SIEMENS

The lifecycle of verification for RISC-V



Any change to a production-proven processor requires users to revalidate not only the new capabilities but original functionality to avoid **unintended consequences**

The combination of **multiple approaches drastically increases confidence** of correctness and performance through the complete lifecycle of a RISC-V based design

SIEMENS

A multiprong approach to improving functional verification

1 Verification speed-up

- Optimized engines
- Find RTL issues earlier than in UVM flow
- Accelerate coverage closure
- Pinpoint bugs – quick fix check

2 High degree of automation

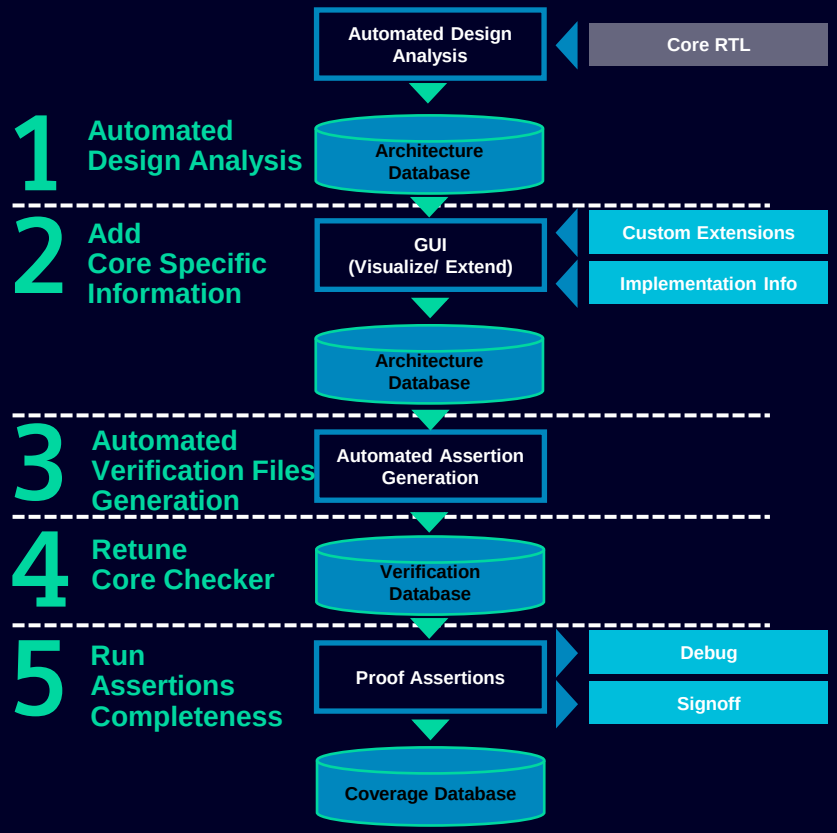
- No writing of functional coverage model
- Automate microarchitecture details extraction
- Automated assertion generation
- Built-in disassembler annotation

3 Exhaustive and complete verification

- 100% functional coverage
- Unbounded proofs
- No undocumented RTL
- Support custom extensions
- ISA and privileged ISA compliance
- Essential for state-of-the-art processor DV

SIEMENS

From automated formal compliance to leading edge software shift-left



VISTA Virtual Platform

A complete system level modelling environment

Veloce Codelink

SW debug and correlation to power profiles, performance, and HW debug

Veloce HYCON

SW enabled validation with preconfigured HYBRID emulation environment

Veloce vProbe

SW development & debug setup consistent with post-silicon methodology

Integrations Between Veloce & 3rd Party SW Development Frameworks
T32, Arm DS, OpenOCD (RISC-V)

Detect issues that would otherwise be impossible to find early in the design process

Software Shift-left built on the industry's most advanced hardware platforms

SIEMENS

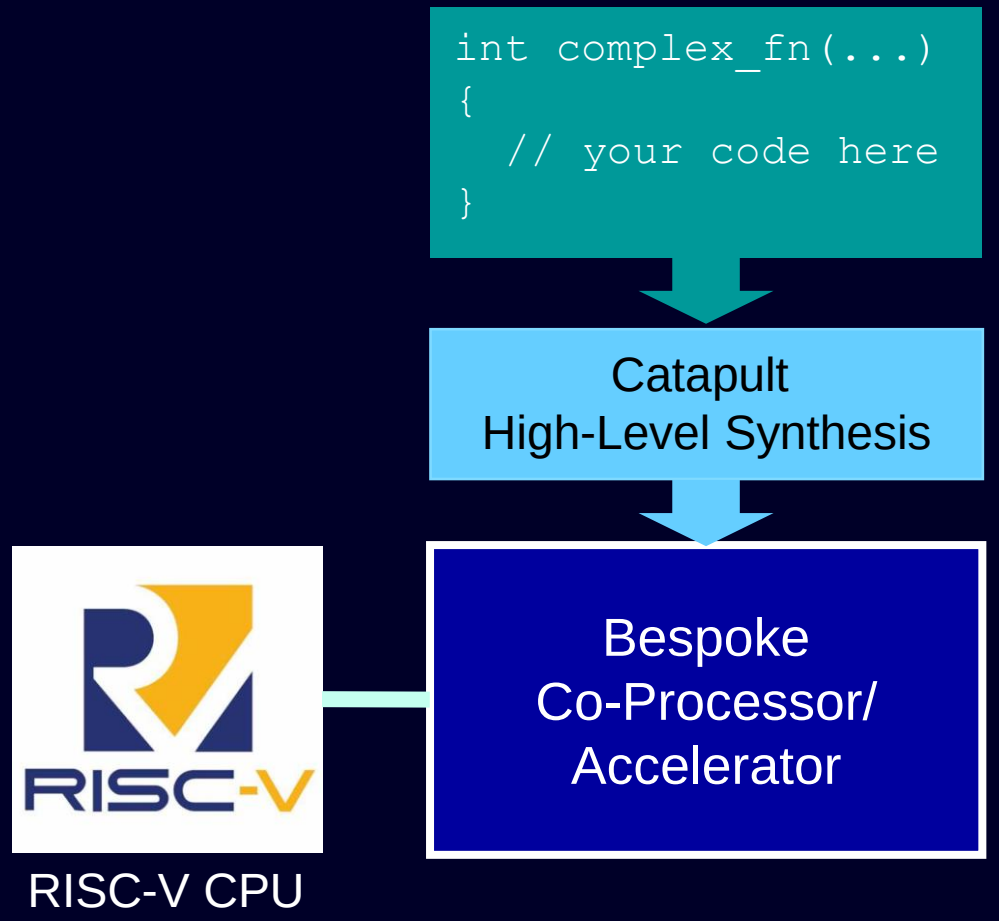
Higher performance, greater efficiency

Go beyond ISA changes

- Augment compute capabilities with co-processors and accelerators

High-level algorithmic synthesis can covert a software functions into an RTL co-processor or accelerator

- Off-load compute intensive functions from software to hardware
- Greater parallelism, higher performance
- Reduced energy consumption
- Enables true "Domain Specific Computing"



Offloading compute intensive operations delivers greater performance and efficiency than possible with instruction set modifications

SIEMENS

Verification that extends into system bring-up and in-life operation

Tessent Embedded Analytics ensures your commitment to verification extends through the product lifecycle

Smart, configurable, silicon IP monitors

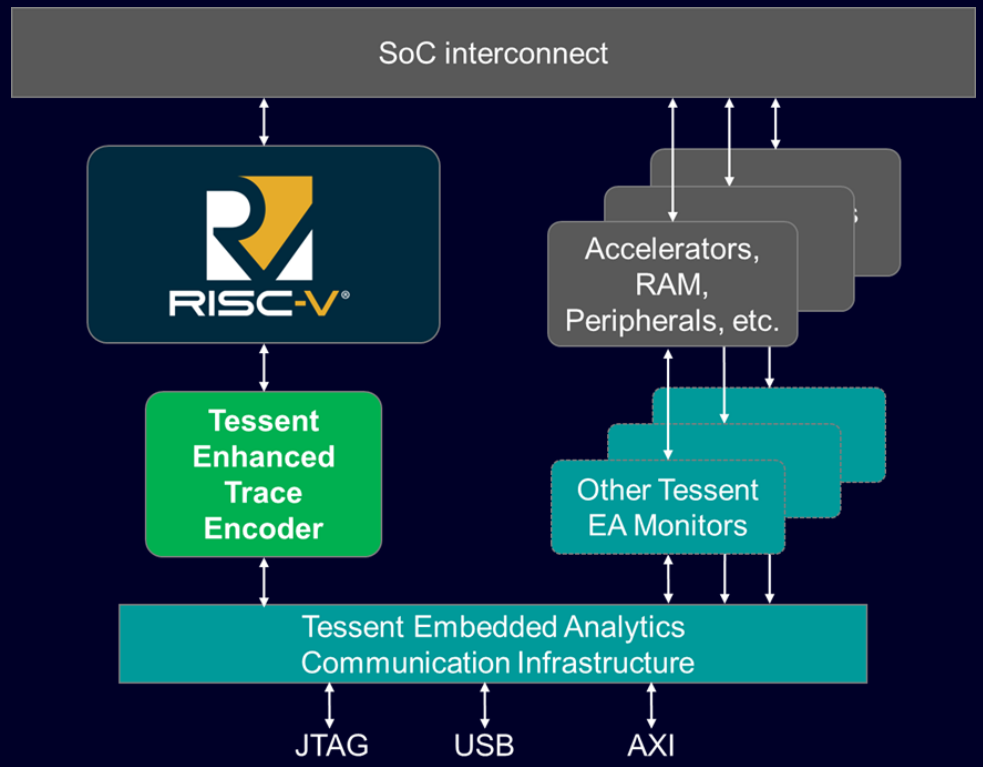
- Programmable collection and filtering of functional data
- Run-time cross-triggering

Analysis and monitoring of complete system behaviour

- Processors, buses, memories, custom logic, software
- Insights into HW-SW interactions
- Heterogeneous/multicore embedded software debug & trace

Optimize embedded system, pre- and post-deployment

- Identify and fix bottlenecks and bugs
- Root-cause system performance issues
- Detect anomalies for security and safety applications



RISC-V trace and debug as part of a complete SoC debug and analytics system

SIEMENS

The design productivity gap is a real and growing problem

1 Trillion

Transistors in chiplet based processors by 2030

How We'll Reach a 1 Trillion Transistor GPU - IEEE Spectrum

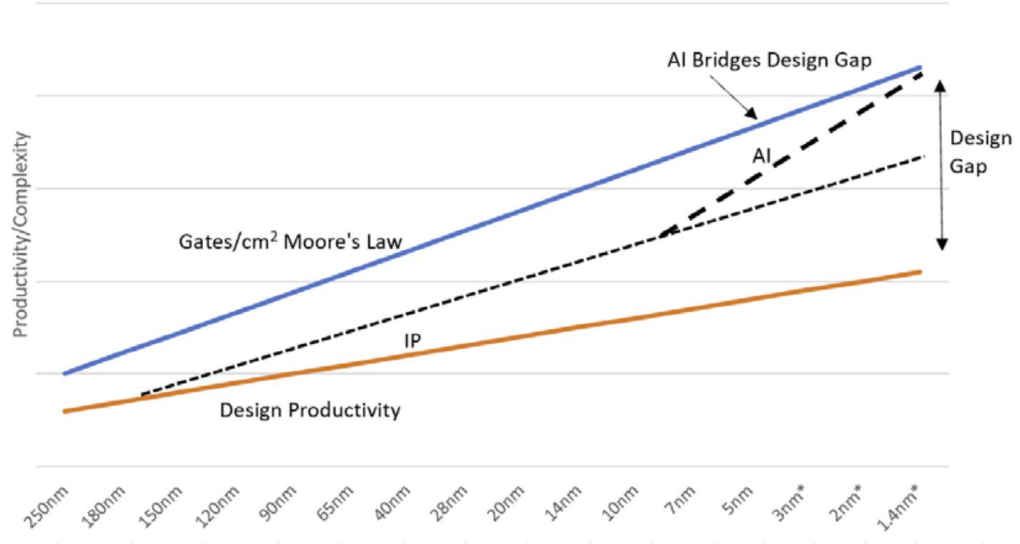
27.3K

Shortage of engineers in the US workforce by 2030

Shortage of Tech Workers - Semiconductor Industry Association (semiconductors.org)

The capability and complexity of a system is directly proportional to the number of transistors integrated into it

Figure 1: Altering the Design Productivity Gap



Advanced EDA tools, new methodologies such as "shift left", and SIP blocks (internal or 3rd party) have made it possible to close the gap somewhat … **IT'S NOT ENOUGH**

SIEMENS

Siemens EDA AI Customer Testimonials

"Saved 13hr Veloce compile time by optimizing memory usage based on prior compilations"

-Large Mobile Semiconductor Vendor

"Aprisa Macro Placement saved us about **3-4 weeks of floor planning with AI-driven approach"**

-Maxlinear, U2U India

"6-sigma verification for standard cells**, 1,000+ times faster with greater accuracy** and coverage using Solido"

-Arm, AWS and Siemens

"5x Production test time improvement with SSN Adaptive intelligence"

-Amazon, ITC 2022

"50% CPU time reduction, 40% reduction in setup time, 60% debugging time reduction for .lib verification with Solido Analytics"

-Samsung, U2U 2022

"100,000X faster design space exploration & optimization for signal integrity with HyperLynx"

"Up to **15x faster DRC iterations** on dirty designs"

-Calibre nmDRC Recon User

"With Questa VIQ Block level coverage closure has been reduced by nearly 70% **reducing weeks off of total schedule"**

-Processor Vendor

"ML-DRC+ delivers a **21% improvement in hotspot accuracy** using Calibre Embedded Machine Learning"

-GlobalFoundries, U2U 2024

"10x productivity improvement for DFT architecture"

-Intel, ITC 2021

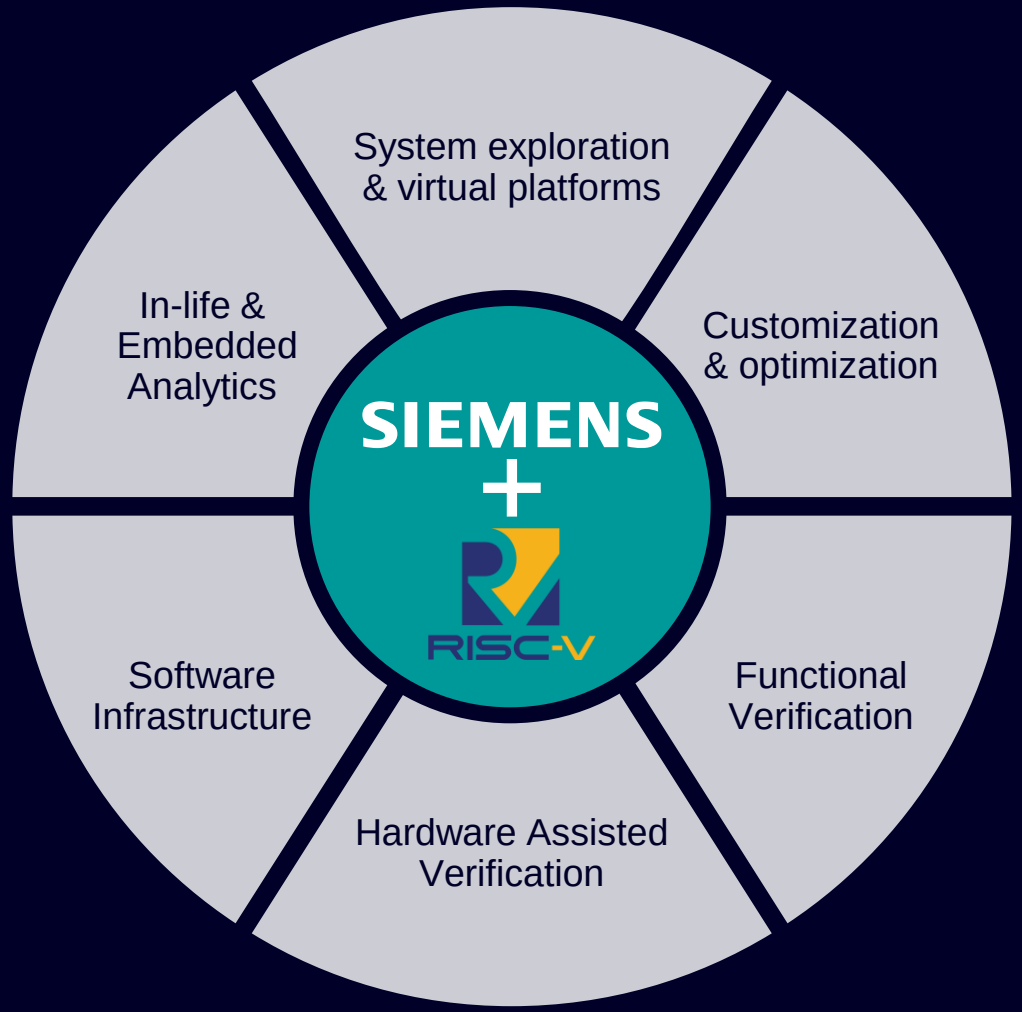
SIEMENS

Siemens and RISC-V

Siemens is not an IP vendor so is a **trustworthy independent voice** in the RISC-V world

There is **great opportunity in the flexibility RISC-V** provides, but be aware of the challenges

From design concept through the end-product lifecycle
Siemens EDA has you covered

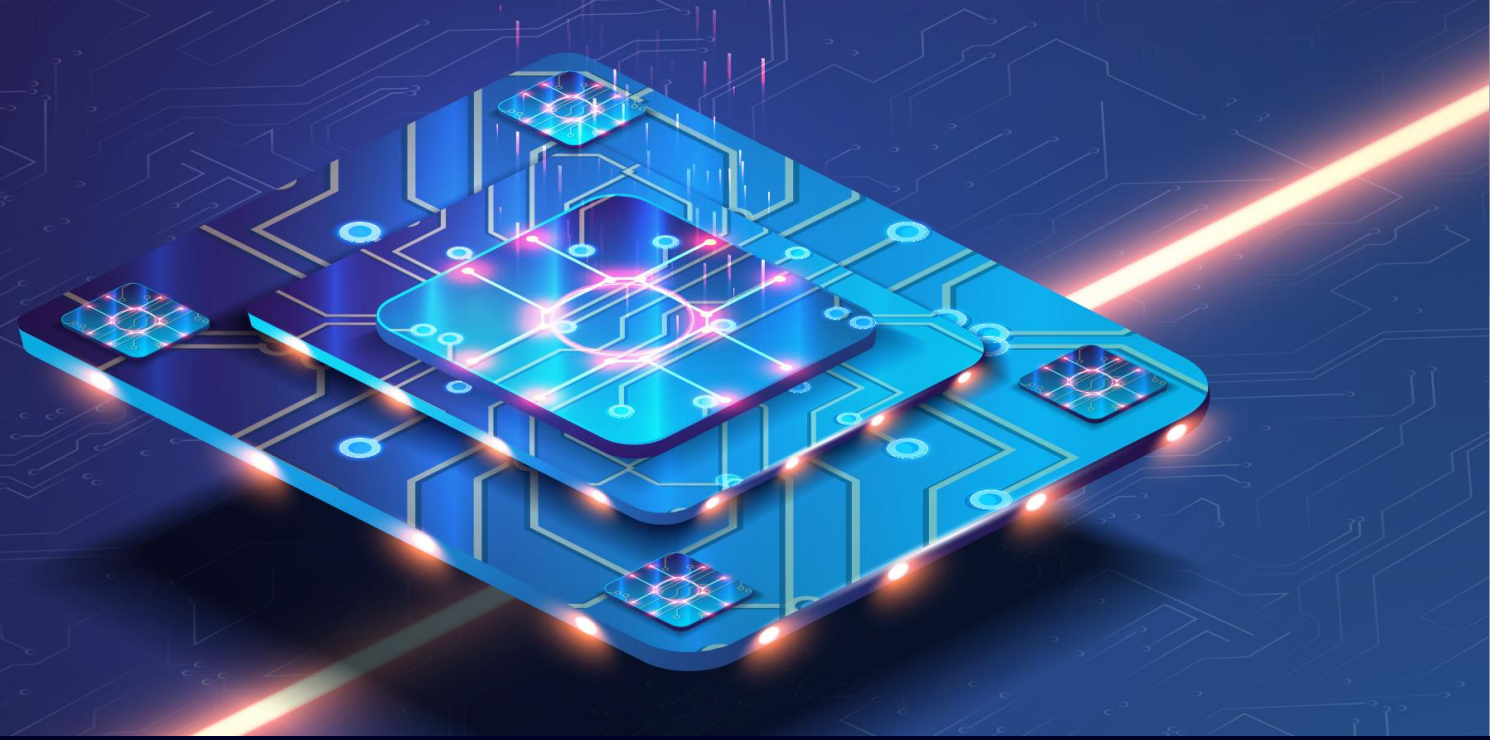


SIEMENS

SIEMENS

+

RISC-V



Thank You

SIEMENS

Contact

Published by Siemens EDA

Thomas Heurung
Technical Director EMEA

Arnulfstraße 201
80634 Munich
Germany
Mobile +49 172 8176300

E-mail thomas.heurung@siemens.com

SIEMENS